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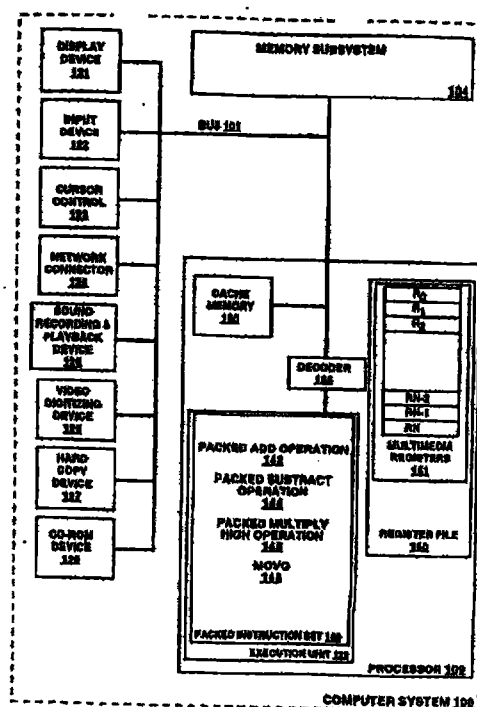
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| (21) International Application Number: PCT/US96/20315<br>(22) International Filing Date: 18 December 1996 (18.12.96)<br>(30) Priority Data:<br>08/574,932 19 December 1995 (19.12.95) US<br>(71) Applicant (for all designated States except US): INTEL CORPORATION [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).<br>(72) Inventors; and<br>(75) Inventors/Applicants (for US only): MENNEMEIER, Larry, M. [US/US]; P.O. Box 587, Boulder Creek, CA 95006 (US). PELEG, Alexander, D. [IL/IL]; 38 Hannah Street, Carmelia, 31015 Haifa (IL). MITTAL, Millind [US/US]; 1149 Hillside Boulevard, South San Francisco, CA 94080 (US). BITAN, Benny [IL/IL]; 25 Stephen Wise, 31015 Haifa (IL). DULONG, Carole [FR/US]; 18983 Harleigh Drive, Saratoga, CA 95070 (US). KOWASHI, Eiichi [JP/JP]; 2-8-10, Kubodai, Ryugasaki 301 (JP).<br>(74) Agents: TAYLOR, Edwin, H. et al.; Blakely, Sokoloff, Taylor & Zafman L.L.P., 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US). |  |                                                                 |
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(54) Title: A COMPUTER SYSTEM PERFORMING A TWO-DIMENSIONAL ROTATION OF PACKED DATA REPRESENTING MULTIMEDIA INFORMATION

## (57) Abstract

A computer system (100) for processing multimedia data, wherein the data is transformed from a first domain to a second domain by performing two dimensional rotation on the data. The computer system (100) includes a memory (104) having stored therein a set of packed data sequences having data elements representing the digital data, and a sequence of instructions for transforming the digital data from a first domain to a second domain. The instructions, when executed, cause the processor (109) to generate a first set of intermediate results in response to the execution of a first instruction which multiplies data elements of a first packed data sequence with corresponding elements of the third packed data sequence, wherein the data of the third packed data sequence represent either a sine or cosine function. The instructions then cause the processor (109) to generate a second set of intermediate results in response to the execution of a second instruction which multiplies the data elements of a second packed data sequence with corresponding data elements of a fourth packed data sequence, wherein the data elements of the fourth packed data sequence representing either a sine or cosine function. A set of first set of final results is generated in response to the execution of a third instruction which performs an arithmetic operation between corresponding data elements of the first and second sets of the intermediate results. The final results represent the digital data transformed into the second domain.



\* (Referred to in PCT Gazette No.44/1997, Section II)

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