

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:
a semiconductor chip comprising an insulative protective layer and a plurality of
5 conductive chip pads exposed through openings in the insulative protective layer; and
a redistribution layer including:
a plurality of insulating layers each comprising an organic film, and
a plurality of conductive redistribution patterns, each of the conductive
redistribution patterns comprising a conductive interconnection portion formed
10 on a surface of a corresponding one of the insulating layers,
wherein at least a first organic film of one of the plurality of insulating layers
comprises a filler comprising a plurality of ion trapping particles formed of an inorganic
material which is chemically reactive with at least one of the following ions: Cl⁻, K⁺,
Na⁺, OH⁻ and H⁺,
15 wherein the first organic film is a first upper polymer film comprising a polymer
material in which the ion trapping particles of the filler are dispersed,
wherein the plurality of insulating layers comprise a first lower polymer film
directly on the first upper polymer film, and
wherein the first upper polymer film has a thickness less than 70% of the
20 thickness of the first lower polymer film.
2. The semiconductor package of claim 1, wherein the first organic film
comprises a photosensitive polymer film having the ion trapping particles of the filler
dispersed therein.

3. The semiconductor package of claim 1 or claim 2, wherein at least some of the plurality of ion trapping particles of the filler are chemically combined with a chlorine ion.

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4. The semiconductor package of any one of claims 1 to 3, wherein the inorganic material of the filler comprises at least one of a magnesium (Mg) compound, an alabamine (Ab) compound and a bismuth (Bi) compound.

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5. The semiconductor package of claim 1,
wherein the first organic film comprises a polymer film formed of a first polymer material and having the ion trapping particles of the filler dispersed therein,
wherein the ion trapping particles have a thermal conductivity higher than that of the first polymer material.

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6. The semiconductor package of claim 1,
wherein the first organic film comprises a polymer film formed of a first polymer material and having the ion trapping particles of the filler dispersed therein,
wherein the ion trapping particles have a coefficient of thermal expansion less
20 than that of the first polymer material.

7. The semiconductor package of any one of claims 1 to 6,
wherein the plurality of redistribution patterns comprise a first redistribution pattern in contact with a first chip pad of the chip pads of the semiconductor pattern.

8. The semiconductor package of claim 7, wherein the first organic film is in contact with the first chip pad.

5 9. The semiconductor package of claim 8, wherein the first chip pad has a surface exposed with respect to the insulative protection layer by a first hole in the insulative protection layer, and the exposed surface of the first chip pad is fully covered by the first organic film and the first redistribution pattern formed within the first hole.

10 10. The semiconductor package of any one of claims 7 to 9, wherein the first redistribution pattern comprises a conductive via and a conductive interconnection integrally formed with the conductive via, wherein the conductive via is formed within the first hole of the insulative protection layer and in contact with the first chip pad and wherein the conductive interconnection is formed on the first organic film.

15 11. The semiconductor package of claim 1,
wherein the plurality of redistribution patterns comprise a first redistribution pattern in contact with a first chip pad of the chip pads of the semiconductor pattern and formed directly on the first lower polymer film, and

20 wherein the first lower polymer film is a photosensitive polymer film.

12. A semiconductor package comprising:
a semiconductor chip comprising an insulative protective layer and a plurality of conductive chip pads exposed through openings in the insulative protective layer; and

a redistribution layer including:

a plurality of insulating layers each comprising an organic film, and

a plurality of conductive redistribution patterns, each of the conductive redistribution patterns comprising a conductive interconnection portion formed on a surface of a corresponding one of the insulating layers,

wherein at least one organic film of one of the plurality of insulating layers comprises a filler comprising a plurality of ion trapping particles formed of an inorganic material dispersed in the at least one organic film, the plurality of ion trapping particles comprised of a material that combines with a reactive material corrosive to the chip pads,

wherein the at least one organic film comprises a first upper polymer film comprising a polymer material in which the ion trapping particles of the filler are dispersed and a first lower polymer film directly on the first upper polymer film,

wherein the first upper polymer film has a thickness less than 70% of the thickness of the first lower polymer film,

wherein the conductive redistribution patterns comprise a first conductive redistribution pattern disposed in an opening, the opening penetrating the first upper polymer film and the first lower polymer film, and

wherein the first conductive redistribution pattern comprises:

a seed pattern covering a bottom of the opening, a sidewall of the first upper polymer film, and a sidewall of the first lower polymer film exposed by the opening; and a conductive pattern disposed on the seed pattern and filling the opening.

13. The semiconductor package of claim 12,

wherein the ion trapping particles have a thermal conductivity higher than that of

the first polymer material, and

wherein the first lower polymer film does not comprise an ion trapping agent.

14. The semiconductor package of claim 12 or claim 13,

5 wherein the plurality of redistribution patterns comprise a first redistribution pattern in contact with a first chip pad of the chip pads of the semiconductor pattern and formed directly on the first lower polymer film.

15. The semiconductor package of claim 14,

10 wherein the first redistribution pattern comprises a conductive via and a conductive interconnection integrally formed with the conductive via,

wherein the conductive via is formed within a hole penetrating the first upper polymer film and first lower polymer film, and the conductive via is in contact with the first chip pad, and

15 wherein the conductive interconnection is formed on the first lower polymer film.

16. The semiconductor package of claim 15, wherein the conductive via has a tapered shape to have a width at the first chip pad that is smaller than a width at the conductive interconnection.

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17. The semiconductor package of claim 15, wherein the conductive via and the conductive interconnection are formed of copper.

18. A method of manufacturing comprising:

forming at least one first insulating layer on a first surface of a semiconductor chip, the first surface of the semiconductor chip comprising a plurality of metal chip pads to provide signals and power to the semiconductor chip, the plurality of metal chip pads including a first chip pad;

- 5 patterning the at least one first insulating layer to expose the chip pads of the semiconductor chip through corresponding openings in the at least one first insulating layer; and

- forming a first redistribution pattern on the first insulating layer, the first redistribution pattern comprising a first via contacting the first chip pad and a first
10 interconnection portion connected to the first via extending horizontally on the at least one first insulating layer,

 wherein the at least one first insulating layer comprises an organic film including a plurality of ion trapping particles dispersed therein, the ion trapping particles comprising an inorganic material,

- 15 wherein the step of forming the at least one first insulating layer on the first surface of the semiconductor chip comprises forming a first upper insulating layer on the first surface of the semiconductor chip and forming a first lower insulating layer of the first upper insulating layer, and

- wherein the first upper insulating layer is the organic film including the plurality
20 of ion trapping particles dispersed therein,

 wherein the first upper insulating layer has a thickness less than 70% of the thickness of the first lower insulating layer.

19. The method of claim 18, wherein the first lower insulating layer comprises

a photosensitive polymer film.

20. The method of any one of claims 18 to 19, wherein the first upper insulating layer is not a photosensitive film.

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