

CLAIMS

We claim:

1. A memory device, comprising:

a base die; and

a plurality of memory dies stacked on the base die and electrically connected to the base die through a plurality of through substrate vias,

wherein the base die includes:

a plurality of first terminals configured to receive channel signals, or channel data from an outside of the memory device during a first operation mode,

a monitoring unit configured to generate monitored data from at least a portion of the received channel signals or the channel data during the first operation mode, and

a plurality of second terminals configured to receive test signals or test data from the outside of the memory device during a second operation mode, and configured to receive the monitored data from the monitoring unit to generate the monitored data to the outside of the memory device during the first operation mode.

2. The memory device of claim 1, wherein:

the second operation mode is a direct access mode in which the test signals and the test data are transmitted through the plurality of second terminals, which are direct access terminals, to the plurality of memory dies for testing of the plurality of memory dies, and

the first operation mode is a system level test mode or normal mode in which the channel signals and the channel data are transmitted through the plurality of first terminals to the plurality of memory dies for accessing the plurality of memory dies, while the at least a portion of the channel signals or the channel data is also transmitted through the monitoring unit and a plurality of first output buffers to be output from the base die at the

plurality of second terminals.

3. The memory device of claim 2, wherein:

the direct access terminals are used for a direct access test operation during the second operation mode, and are used for a monitoring operation during the first operation mode,

wherein the buffer die further includes:

a plurality of first input buffers configured to receive the channel signals or the channel data from the plurality of first terminals to generate the at least a portion of the received channel signals or the channel data to the monitoring unit during the first operation mode,

a plurality of second input buffers configured to receive the test signals or the test data from the plurality of second terminals during the second operation mode, and

the plurality of first output buffers configured to receive the monitored data from the monitoring unit to generate the monitored data to the plurality of second terminals during the first operation mode.

4. The memory device of claim 3, wherein:

during the first operation mode, the at least a portion of the channel signals and the channel data received at the plurality of first input buffers are transmitted to the plurality of memory dies while they are transmitted to the monitoring unit.

5. The memory device of any one of claims 1 to 4, wherein:

the test signals and the test data includes test information, and all of the plurality of second terminals are used to receive test information during the second operation mode

and to receive the monitored data during the first operation mode.

6. The memory device of any one of claims 2 to 5, wherein:

the memory device is configured to output channel data, received from the plurality of memory dies, through a plurality of second output buffers during the first operation mode and to output test data, received from the plurality of memory dies, through the plurality of first output buffers during the second operation mode.

7. The memory device of any one of claims 2 to 6,

wherein each of the plurality of memory dies includes at least one memory channel, and the plurality of through substrate vias connected to a plurality of signal terminals and a plurality of data terminals, and is configured to receive corresponding signals or corresponding data transmitted from the base die through the plurality of through substrate vias.

8. The memory device of any one of claims 1 to 7,

wherein the channel signals includes channel clock signals and channel command/addresses, and

the monitoring unit is configured to receive at least a portion of the channel command/addresses and the channel data applied in a double data rate (DDR), and to generate the monitored data in a single data rate (SDR) or DDR, in response to the channel clock signals.

9. The memory device of claim 8, wherein the monitoring unit is configured to receive the channel command/addresses, and generate at least a portion of row

command/addresses and column command/addresses included in the channel command/addresses as the monitored data, in response to the channel clock signals.

10. The memory device of claim 9, wherein the monitoring unit includes a channel monitoring unit for each of the plurality of memory dies, and

the channel monitoring unit includes a row monitoring unit configured to receive the row command/addresses and generate at least a portion of an odd row command/address and an even row command/address included in the row command/address as a row output signal, in response to the channel clock signal, and a column monitoring unit configured to receive the column command/address and generate at least a portion of an odd column command/address and an even column command/address included in the column command/address as a column output signal, in response to the channel clock signal.

11. The memory device of claim 10, wherein the row monitoring unit includes a first flip-flop configured to receive and output the row command/address, in response to the channel clock signal, a second flip-flop configured to generate an output signal of the first flip-flop as the odd row command/address in response to an inverted channel clock signal generated by inverting the channel clock signal, and a third flip-flop configured to generate the row command and address as the even row command/address in response to the inverted channel clock signal, and

the column monitoring unit includes a fourth flip-flop configured to receive and output the column command/address, in response to the channel clock signal, a fifth flip-flop configured to generate an output signal of the fourth flip-flop as the odd column command/address, in response to the inverted channel clock signal, and a sixth flip-flop configured to generate the column command/address as the even column command and

address, in response to the inverted channel clock signal, and

wherein the odd row command/address includes a first odd row command/address and a second odd row command/address which are sequentially generated, and the even row command/address includes a first even row command/address and a second even row command/address which are sequentially generated.

12. The memory device of claim 11, wherein the row monitoring unit further includes a first selector configured to generate the odd row command/address or the even row command/address as the row output signal, in response to a first selection signal, and

the column monitoring unit further includes a second selector configured to generate the odd column command/address or the even column command/address as the column output signal, in response to the first selection signal.

13. The memory device of claim 12, wherein the channel monitoring unit further includes a third selector configured to generate the row output signal or the column output signal as a channel output signal, in response to a second selection signal, and

the monitoring unit further includes a fourth selector configured to select and output one of the channel output signals output from the channel monitoring units, in response to a third selection signal.

14. The memory device of claim 10, wherein the row monitoring unit includes:

a first flip-flop configured to generate the row command/address as the odd row command/address, in response to the channel clock signal, and

a second flip-flop configured to generate the row command/address as the even row command/address, in response to an inverted channel clock signal generated by inverting

the channel clock signal, and

wherein the column monitoring unit includes:

a third flip-flop configured to generate the column command/address as the odd column command/address, in response to the channel clock signal, and

a fourth flip-flop configured to generate the column command/address as the even column command/address, in response to the inverted channel clock signal.

15. The memory device of claim 14, wherein the row monitoring unit further includes a first selector configured to generate the odd row command/address as the row output signal in response to the channel clock signal or generate the even row command/address as the row output signal in response to the channel clock signal, and

the column monitoring unit further includes a second selector configured to generate the odd column command/address as the column output signal in response to the channel clock signal or the even column command/address as the column output signal, in response to the channel clock signal in response to the channel clock signal, and

wherein the odd row command and address includes a first odd row command/address and a second odd row command/address which are sequentially generated, the even row command/address includes a first even row command/address and a second even row command/address which are sequentially generated, the row output signal includes the first odd row command/address, the first even row command/address, the second odd row command/address, and the second even row command/address which are sequentially generated, and the column output signal includes the odd column command/address and the even column command/address which are sequentially generated.

16. The memory device of claim 15, wherein the channel monitoring unit further includes a third selector configured to generate the row output signal or the column output signal as a channel output signal, in response to a second selection signal, and

the monitoring unit further includes a fourth selector configured to select and output one of the channel output signals output from the channel monitoring units, in response to a third selection signal.

17. The memory device of claim 8, wherein the monitoring unit includes a channel monitoring unit for each of the plurality of memory dies, and

the channel monitoring unit includes a first flip-flop configured to receive and output the channel data in response to the channel clock signal, a second flip-flop configured to generate an output signal of the first flip-flop as odd data, in response to an inverted channel clock signal generated by inverting the channel clock signal, a third flip-flop configured to generate the channel data as even data, in response to the inverted channel clock signal, and a storage unit configured to store the odd data and the even data in parallel in response to the channel clock signal, and sequentially generate the odd data and the even data as monitoring data.

18. A memory system device, comprising:

a system device substrate;

a memory device including a base die and a set of memory dies stacked on the system device substrate, the base die electrically connected to the set of memory dies by through substrate vias;

a controller; and

an interposer mounted on the system device substrate and on which the memory

device and controller are mounted, wherein the interposer electrically connects the memory device to the controller, wherein:

the controller is configured to receive, as input to the memory system device, control signals and data signals, and based on the input, to output channel clock signals, channel command/addresses, and channel data to the memory device; and

the base die is configured to:

receive the channel clock signals, channel command/addresses, and channel data from the controller at a first set of input/output (i/o) terminals of the base die;

transmit the channel clock signals, channel command/addresses, and channel data to the set of memory dies; and

transmit at least a portion of one or more of the channel clock signals, channel command/addresses, and channel data through a monitoring unit to a second set of i/o terminals of the base die.

19. The memory system device of claim 18, wherein:

the base die further includes:

a first set of buffers connected to the first set of i/o terminals and connected to receive the channel clock signals, channel command/addresses, and channel data from the first set of i/o terminals; and

a second set of buffers connected to the second set of i/o terminals and connected to transmit the at least a portion of one or more of the channel clock signals, channel command/addresses, and channel data to the second set of i/o terminals.

20. The memory system device of claim 19, wherein:

the monitoring unit is connected between the first set of buffers and the second set of

buffers, and is configured to transmit signals output from the first set of buffers to the second set of buffers during a first operation mode of the memory device and to prevent transmission of the signals output from the first set of buffers to the second set of buffers during a second operation mode of the memory device.