CLAIMS

1. A method, comprising:

depositing a first portion of a first material layer on a semiconductor structure;

performing a first run of a post-treatment process for modifying at least said first portion of said first material layer;

after said first run of said post-treatment process, depositing a second portion of said first material layer, said second portion being formed of substantially the same material as said first portion; and

after said deposition of said second portion of said first material layer, performing a second run of said post-treatment process for modifying at least said second portion of said first material layer.

2. A method according to claim 1, further comprising:

after said second run of said post-treatment process, depositing at least one further portion of said first material layer on said semiconductor structure, each further portion of said first material layer being formed of substantially the same material as said first and second portion of said first material layer and, after each deposition of one of the at least one further portion of said first material layer, performing a run of said post-treatment process.

3. A method according to claim 1, wherein each of said deposition of said first portion of said first material layer and said deposition of said second portion of said first material layer comprises performing a run of a deposition process.

4. A method according to claim 3, wherein said deposition process is a chemical vapor deposition process.

5. A method according to claim 4, wherein a material of said first and second portion of said first material layer comprises silicon dioxide, and a reactant gas comprising silane and nitrous oxide is used in said chemical vapor deposition process.

6. A method according to claim 4, wherein said post-treatment process comprises exposing said semiconductor structure to a plasma, wherein said plasma is formed by an electric discharge in

a gas having a different composition than a reactant gas used in said chemical vapor deposition process.

7. A method according to claim 6, wherein said plasma is formed by an electric discharge in a gas comprising oxygen.

8. A method according to claim 7, wherein said plasma is formed by means of a decoupled plasma source.

9. A method according to claim 1, further comprising forming a second material layer on said first material layer, said second material layer being formed of a material having a greater dielectric constant than a material of said first material layer.

10. A method according to claim 9, wherein said material of said first material layer comprises silicon dioxide and said material of said second material layer has a dielectric constant of about 10 or more.

11. A method according to claim 10, wherein said material of said second material layer comprises at least one of hafnium oxide, zirconium oxide, hafnium silicate and zirconium silicate.

12. A method according to claim 1, further comprising forming a gate electrode of a field effect transistor above said first material layer, said first material layer being located between a channel region of said field effect transistor and said gate electrode for providing electrical insulation between said gate electrode and said channel region.

13. A method according to claim 12, wherein said channel region comprises at least one of silicon and germanium.

14. A method according to claim 1, wherein said post-treatment process comprises exposing said semiconductor structure to an oxidizing ambient, wherein a portion of said semiconductor structure adjacent said first material layer is oxidized during said first run of said post-treatment process.

15. A method according to claim 14, wherein said oxidized portion adjacent said first material layer has a thickness in a range from about 2 angstroms to about 6 angstroms.

16. A method according to claim 9, wherein a total thickness of said first material layer and said second material layer is greater than about 30 angstroms.

17. A method according to claim 9, wherein a total thickness of said first material layer and said second material layer is in a range from about 30 angstroms to about 80 angstroms.

18. A method of forming a field effect transistor, comprising:

providing a semiconductor structure comprising a semiconductor material;

forming a gate insulation layer on said semiconductor material, wherein forming said gate insulation layer comprises:

performing a first run of a chemical vapor deposition process to deposit a first portion of a silicon dioxide layer on said semiconductor material;

after said first run of said chemical vapor deposition process, performing a first run of a plasma oxidation process wherein a portion of said semiconductor material adjacent said first portion of said silicon dioxide layer is oxidized;

after said first run of said plasma oxidation process, performing a second run of said chemical vapor deposition process to deposit a second portion of said silicon dioxide layer on said first portion of said silicon dioxide layer; and

after said second run of said chemical vapor deposition process, performing a second run of said plasma oxidation process;

the method further comprising:

forming a gate electrode above said gate insulation layer.

19. A method of forming a field effect transistor according to claim 18, wherein forming said gate insulation layer further comprises forming a layer of a material having a greater dielectric constant than silicon dioxide on said silicon dioxide layer.

20. A method of forming a field effect transistor according to claim 19, wherein forming the gate insulation layer further comprises:

after said second run of said plasma oxidation process, performing one or more runs of said chemical vapor deposition process to deposit one or more further portions of said silicon dioxide layer, wherein a run of said plasma oxidation process is performed after each run of said chemical vapor deposition process.

CLAIMS

1. A method, comprising:

depositing a first portion of a first material layer on a semiconductor structure;

performing a first run of a post-treatment process for modifying at least said first portion of said first material layer, wherein said post-treatment process comprises exposing said semiconductor structure to an oxidizing ambient, wherein a portion of said semiconductor structure adjacent said first material layer is oxidized during said first run of said post-treatment process;

after said first run of said post-treatment process, depositing a second portion of said first material layer, said second portion being formed of substantially the same material as said first portion;

after said deposition of said second portion of said first material layer, performing a second run of said post-treatment process for modifying at least said second portion of said first material layer; and

forming a gate electrode of a field effect transistor above said first material layer, said first material layer being located between a channel region of said field effect transistor and said gate electrode for providing electrical insulation between said gate electrode and said channel region.

2. The method of claim 1, further comprising, after said second run of said post-treatment process, depositing at least one further portion of said first material layer on said semiconductor structure, each further portion of said first material layer being formed of substantially the same material as said first and second portion of said first material layer and, after each deposition of one of the at least one further portion of said first material layer, performing a run of said post-treatment process.

3. The method of claim 1, wherein each of said deposition of said first portion of said first material layer and said deposition of said second portion of said first material layer comprises performing a run of a deposition process.

4. The method of claim 3, wherein said deposition process is a chemical vapor deposition process.

5. The method of claim 4, wherein a material of said first and second portion of said first material layer comprises silicon dioxide, and a reactant gas comprising silane and nitrous oxide is used in said chemical vapor deposition process.

6. The method of claim 4, wherein said post-treatment process comprises exposing said semiconductor structure to a plasma, wherein said plasma is formed by an electric discharge in a gas having a different composition than a reactant gas used in said chemical vapor deposition process.

7. The method of claim 6, wherein said plasma is formed by an electric discharge in a gas comprising oxygen.

8. The method of claim 7, wherein said plasma is formed by means of a decoupled plasma source.

9. The method of claim 1, further comprising forming a second material layer on said first material layer, said second material layer being formed of a material having a greater dielectric constant than a material of said first material layer.

10. The method of claim 9, wherein said material of said first material layer comprises silicon dioxide and said material of said second material layer has a dielectric constant of about 10 or more.

11. The method of claim 1, wherein said channel region comprises at least one of silicon and germanium.

12. The method of claim 1, wherein said oxidized portion adjacent said first material layer has a thickness in a range from about 2-6 Å.

13. The method of claim 9, wherein a total thickness of said first material layer and said second material layer is greater than about 30 Å.

14. The method of claim 9, wherein a total thickness of said first material layer and said second material layer is in a range from about 30-80 Å.

15. A method of forming a field effect transistor, comprising:

providing a semiconductor structure comprising a semiconductor material;

forming a gate insulation layer on said semiconductor material, wherein forming said gate insulation layer comprises:

performing a first run of a chemical vapor deposition process to deposit a first portion of a silicon dioxide layer on said semiconductor material;

after said first run of said chemical vapor deposition process, performing a first run of a plasma oxidation process wherein a portion of said semiconductor material adjacent said first portion of said silicon dioxide layer is oxidized;

after said first run of said plasma oxidation process, performing a second run of said chemical vapor deposition process to deposit a second portion of said silicon dioxide layer on said first portion of said silicon dioxide layer; and

after said second run of said chemical vapor deposition process, performing a second run of said plasma oxidation process;

the method further comprising: forming a gate electrode above said gate insulation layer.

16. The method of claim 15, wherein forming said gate insulation layer further comprises forming a layer of a material having a greater dielectric constant than silicon dioxide on said silicon dioxide layer.

17. The method of claim 16, wherein forming the gate insulation layer further comprises, after said second run of said plasma oxidation process, performing one or more runs of said chemical vapor deposition process to deposit one or

more further portions of said silicon dioxide layer, wherein a run of said plasma oxidation process is performed after each run of said chemical vapor deposition process.

18. A semiconductor device having a semiconductor structure treated in accordance with any one of the preceding claims.