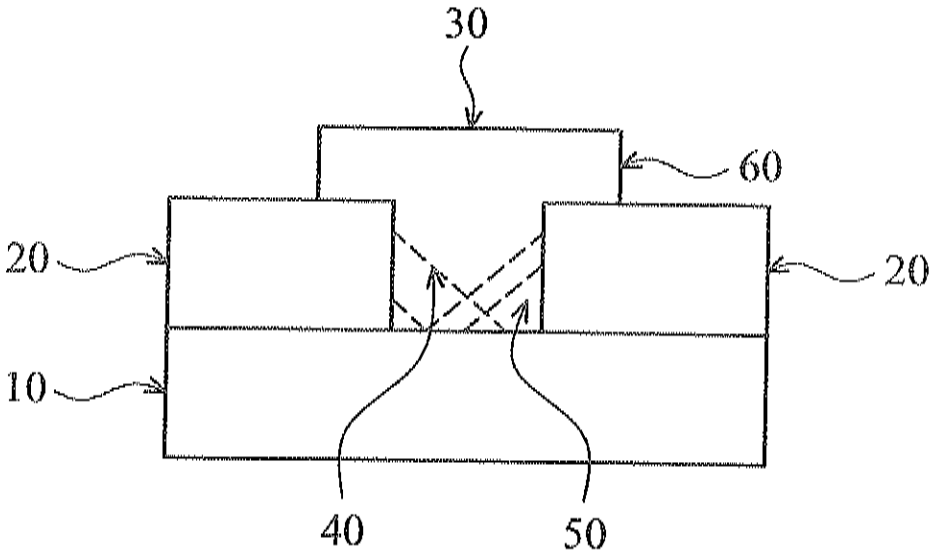


Figure 1

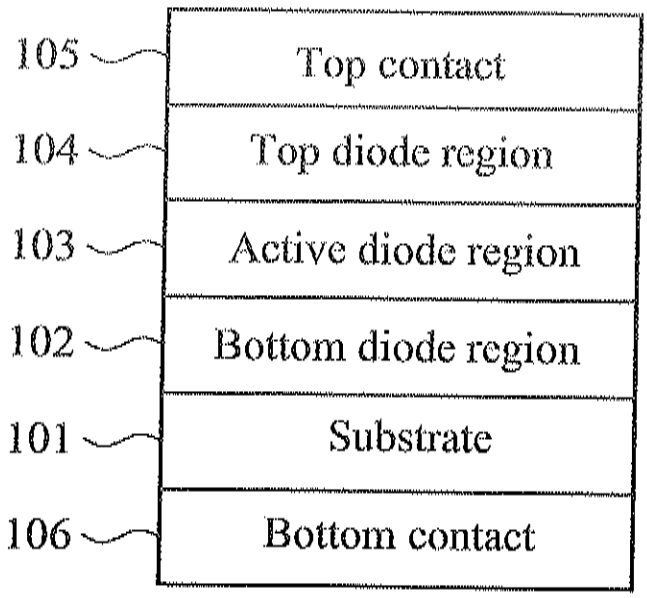


Figure 2

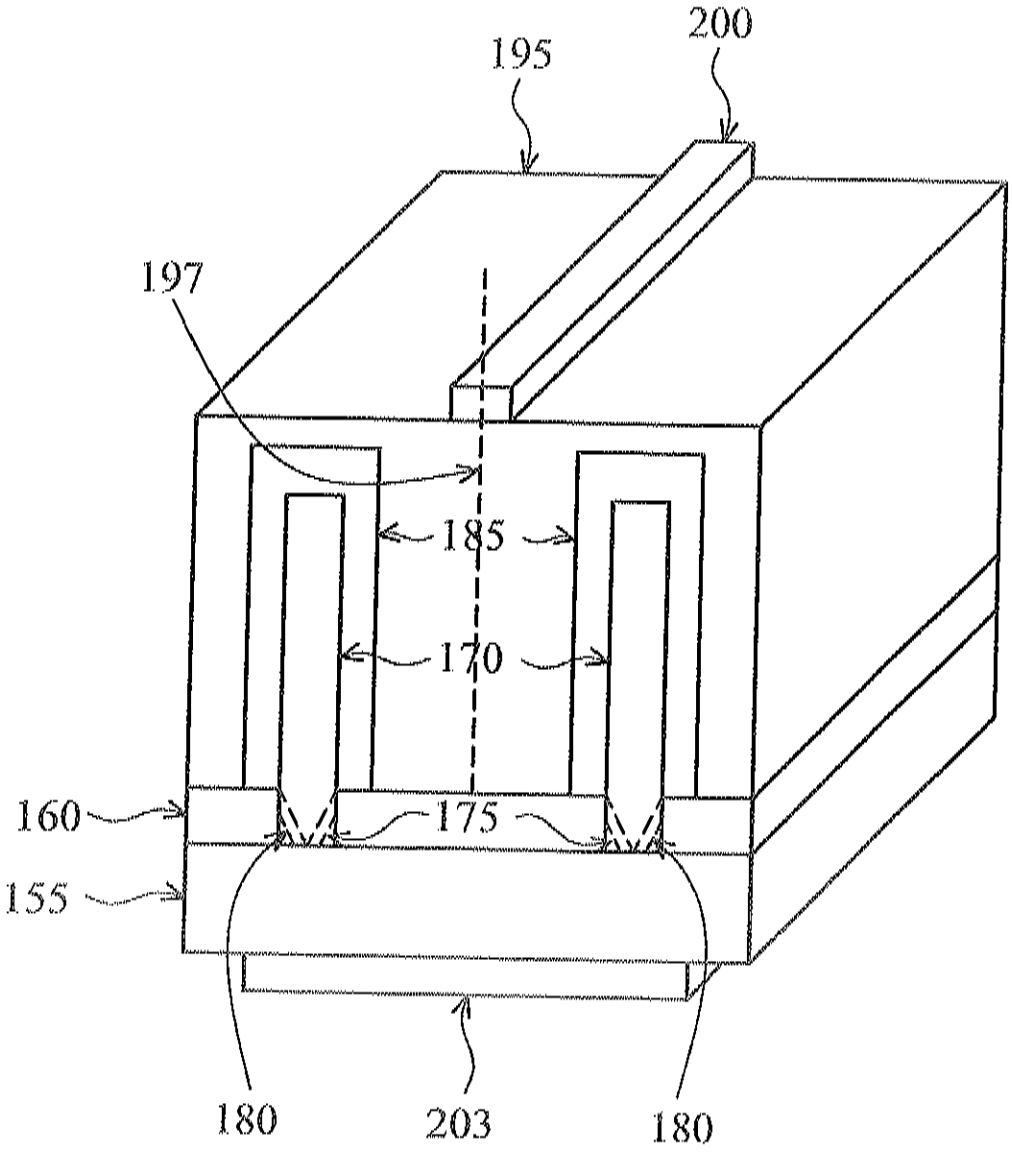


Figure 3

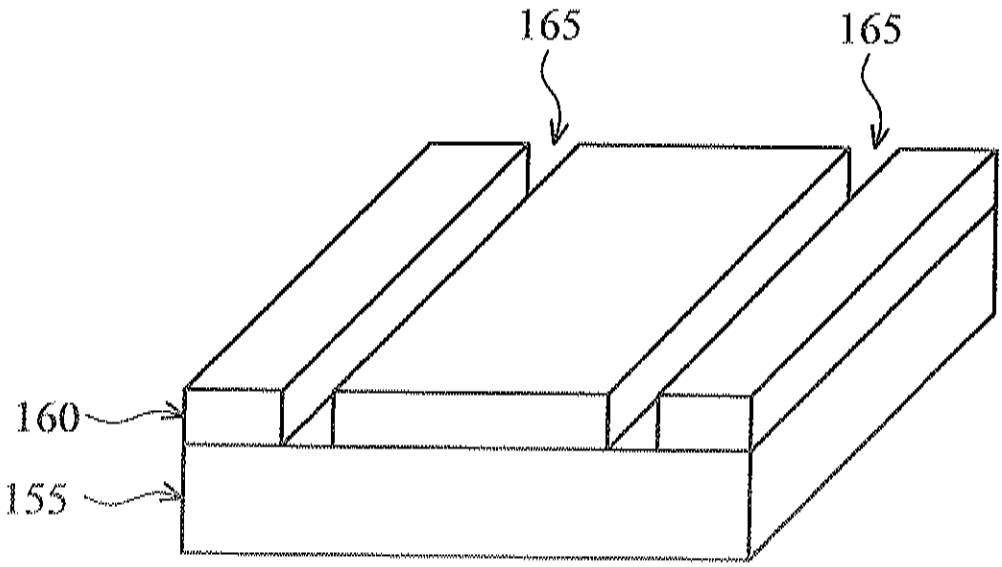


Figure 4

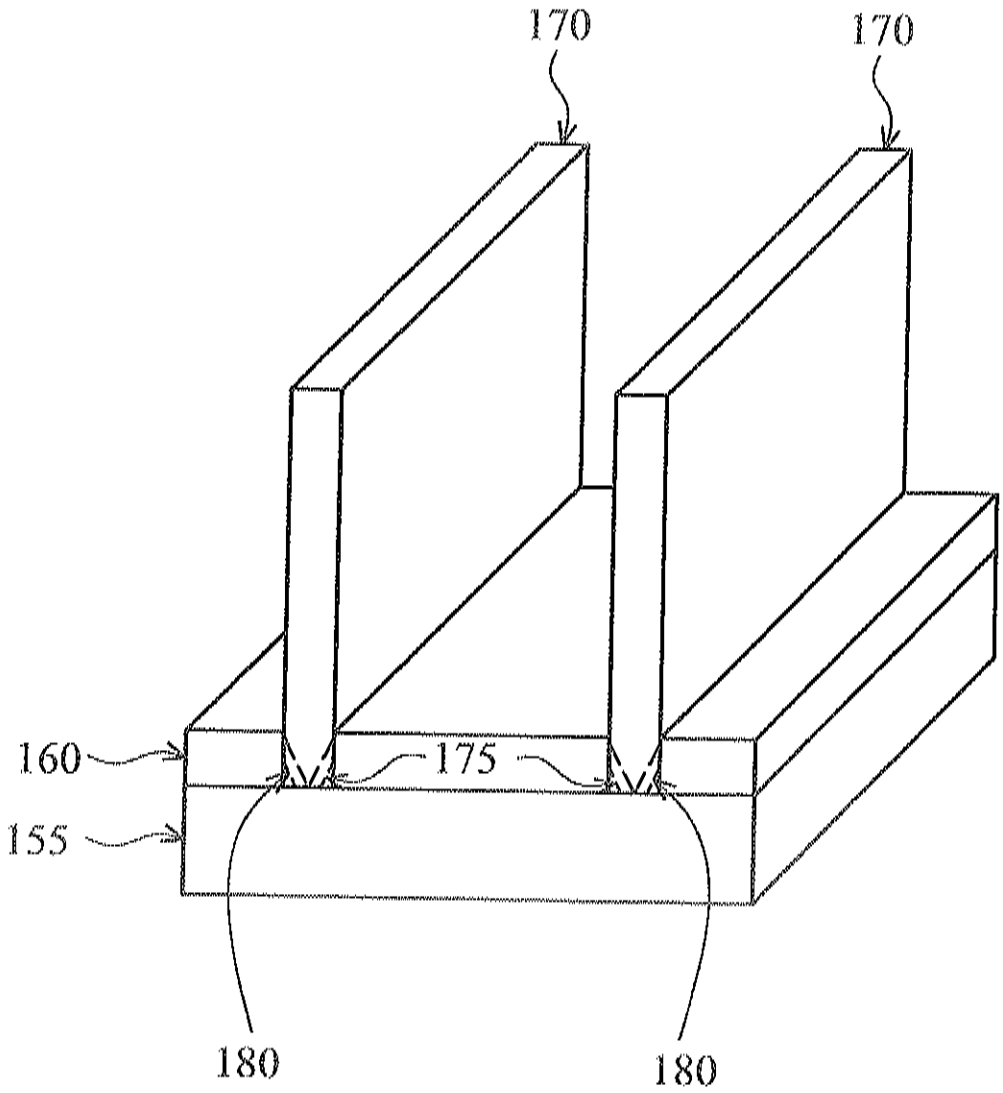


Figure 5

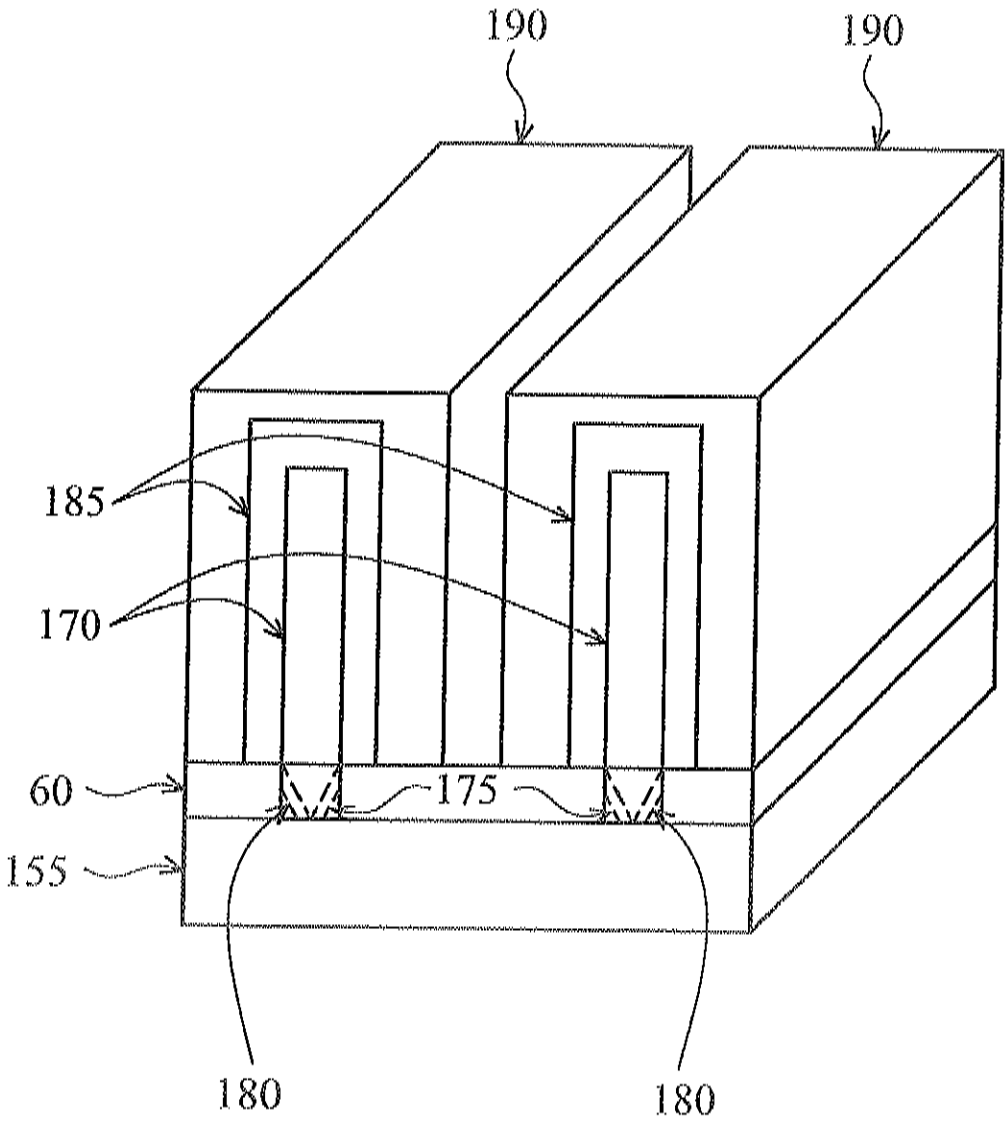


Figure 6

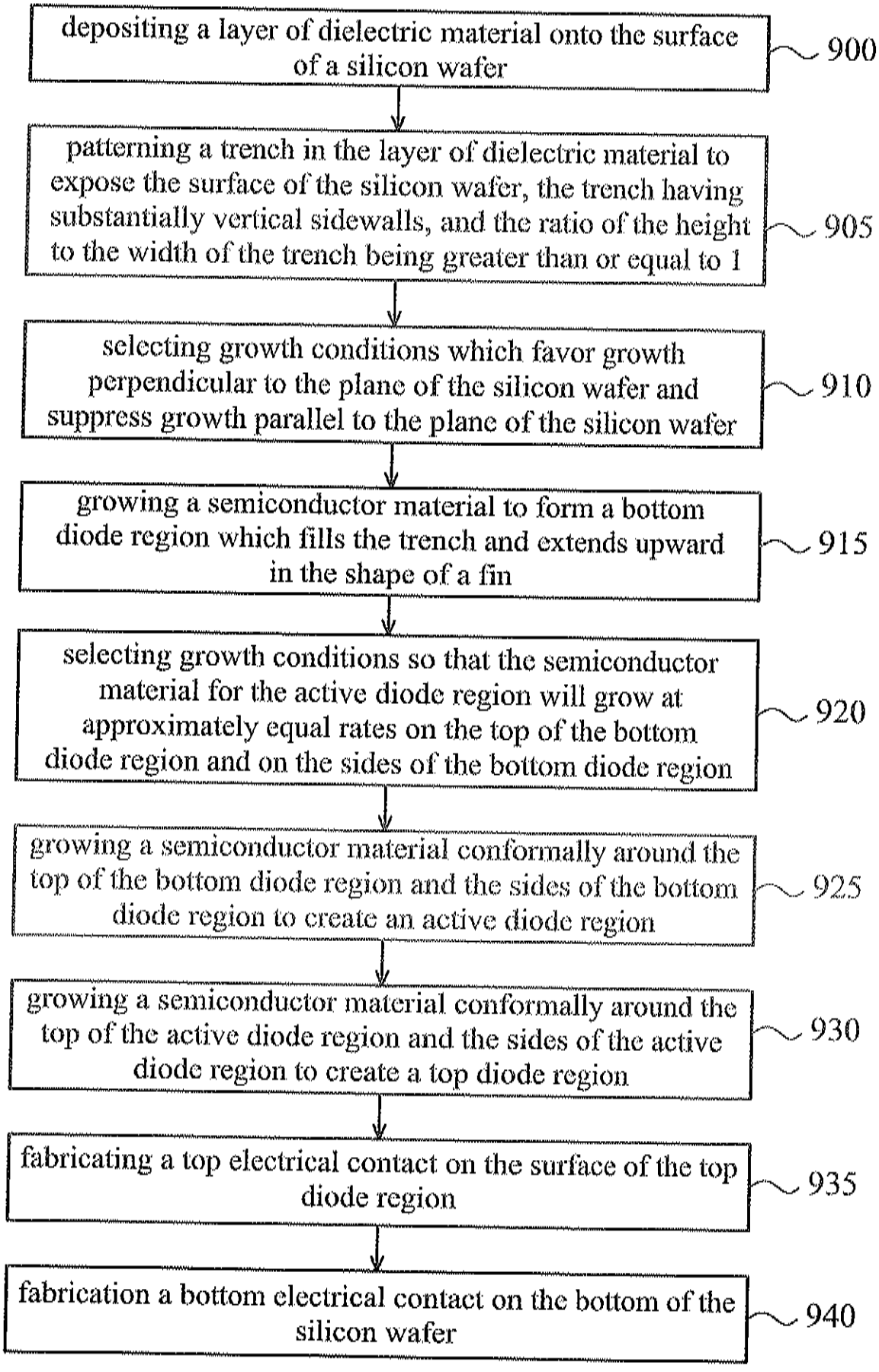

depositing a layer of dielectric material onto the surface of a silicon wafer
900
patterning a trench in the layer of dielectric material to expose the surface of the silicon wafer, the trench having substantially vertical sidewalls, and the ratio of the height to the width of the trench being greater than or equal to 1
905
selecting growth conditions which favor growth perpendicular to the plane of the silicon wafer and suppress growth parallel to the plane of the silicon wafer
910
growing a semiconductor material to form a bottom diode region which fills the trench and extends upward in the shape of a fin
915
selecting growth conditions so that the semiconductor material for the active diode region will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region
920
growing a semiconductor material conformally around the top of the bottom diode region and the sides of the bottom diode region to create an active diode region
925
growing a semiconductor material conformally around the top of the active diode region and the sides of the active diode region to create a top diode region
930
fabricating a top electrical contact on the surface of the top diode region
935
fabrication a bottom electrical contact on the bottom of the silicon wafer
940

Figure 7

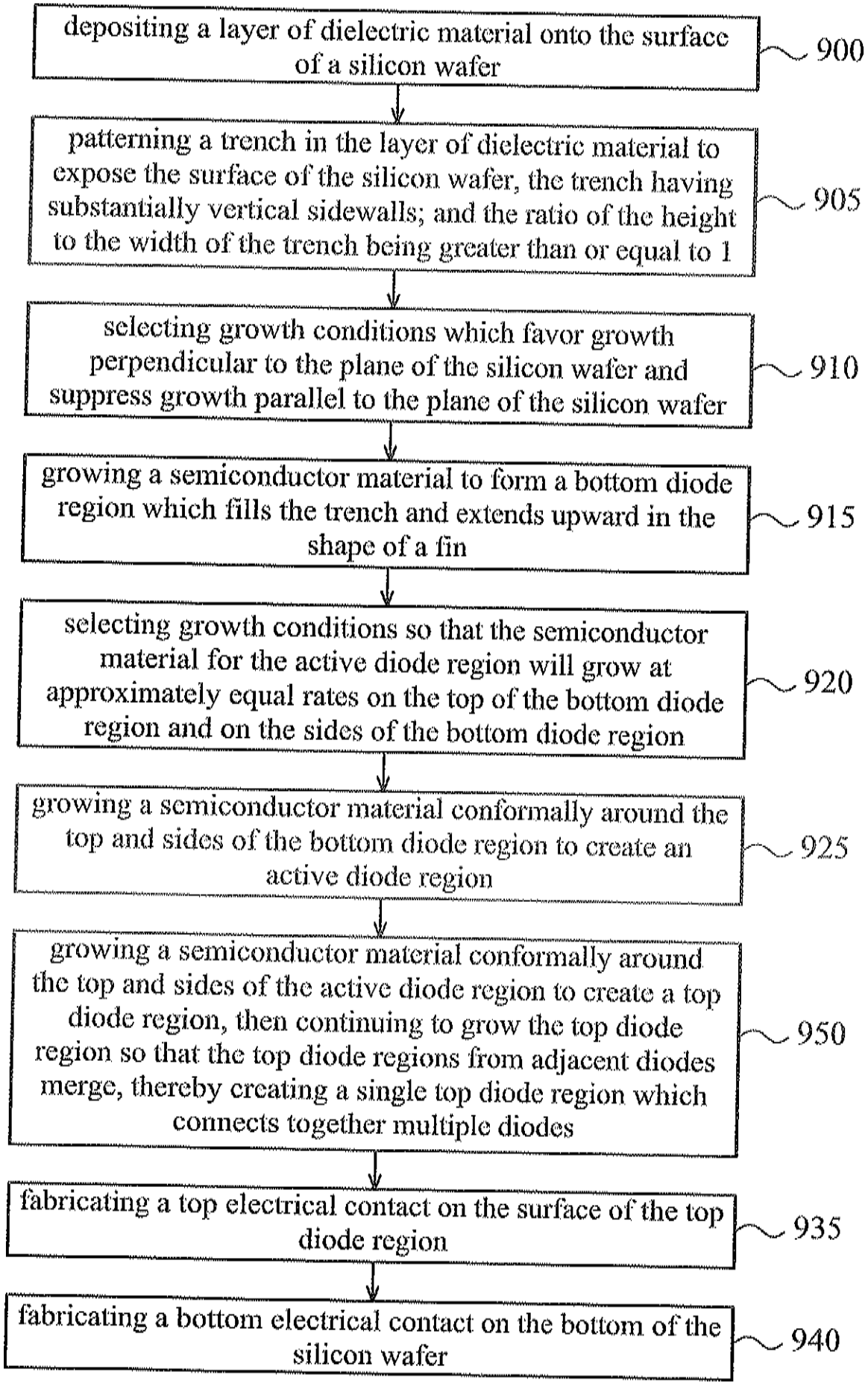

depositing a layer of dielectric material onto the surface of a silicon wafer
900
patterning a trench in the layer of dielectric material to expose the surface of the silicon wafer, the trench having substantially vertical sidewalls; and the ratio of the height to the width of the trench being greater than or equal to 1
905
selecting growth conditions which favor growth perpendicular to the plane of the silicon wafer and suppress growth parallel to the plane of the silicon wafer
910
growing a semiconductor material to form a bottom diode region which fills the trench and extends upward in the shape of a fin
915
selecting growth conditions so that the semiconductor material for the active diode region will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region
920
growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region
925
growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region, then continuing to grow the top diode region so that the top diode regions from adjacent diodes merge, thereby creating a single top diode region which connects together multiple diodes
950
fabricating a top electrical contact on the surface of the top diode region
935
fabricating a bottom electrical contact on the bottom of the silicon wafer
940

Figure 8

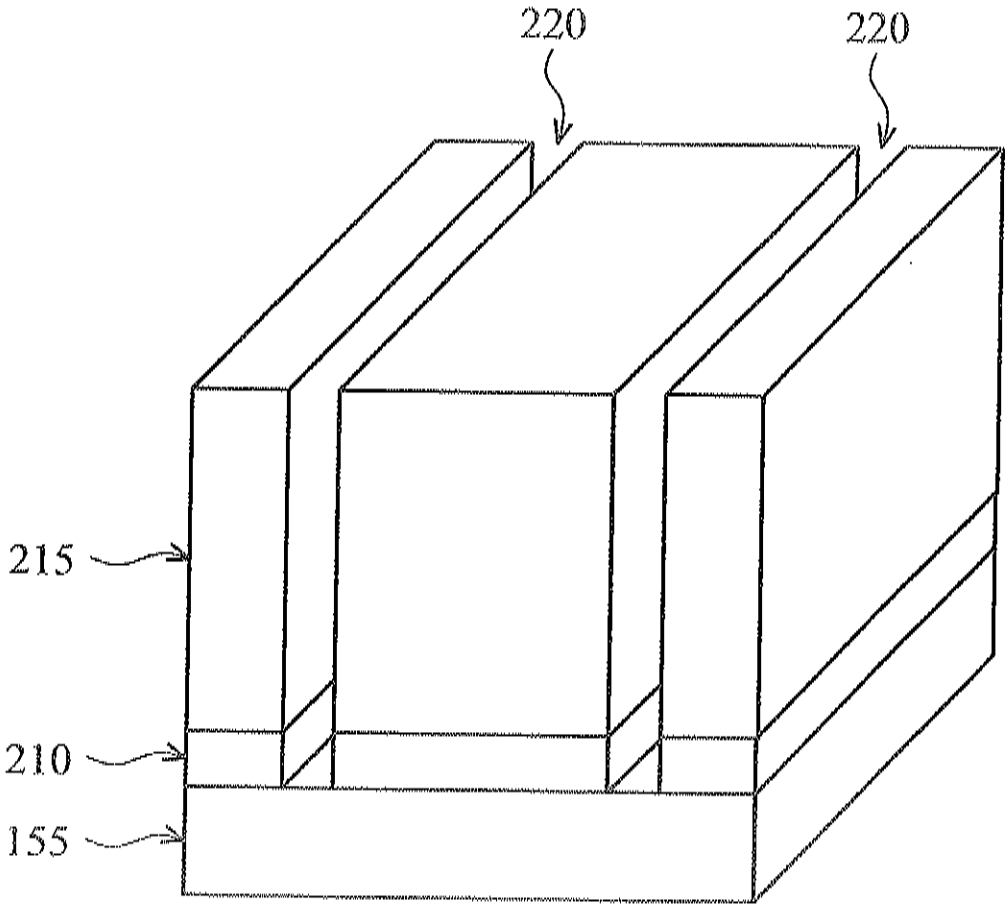


Figure 9

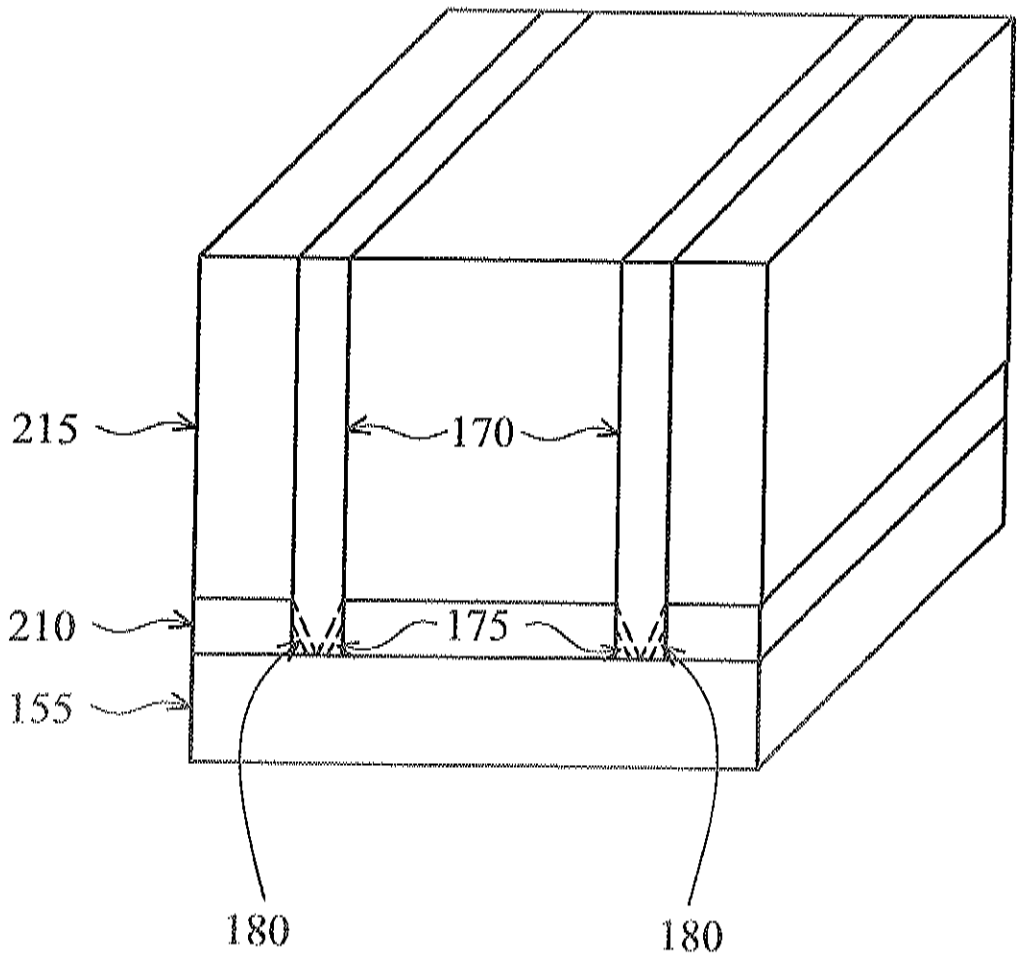


Figure 10

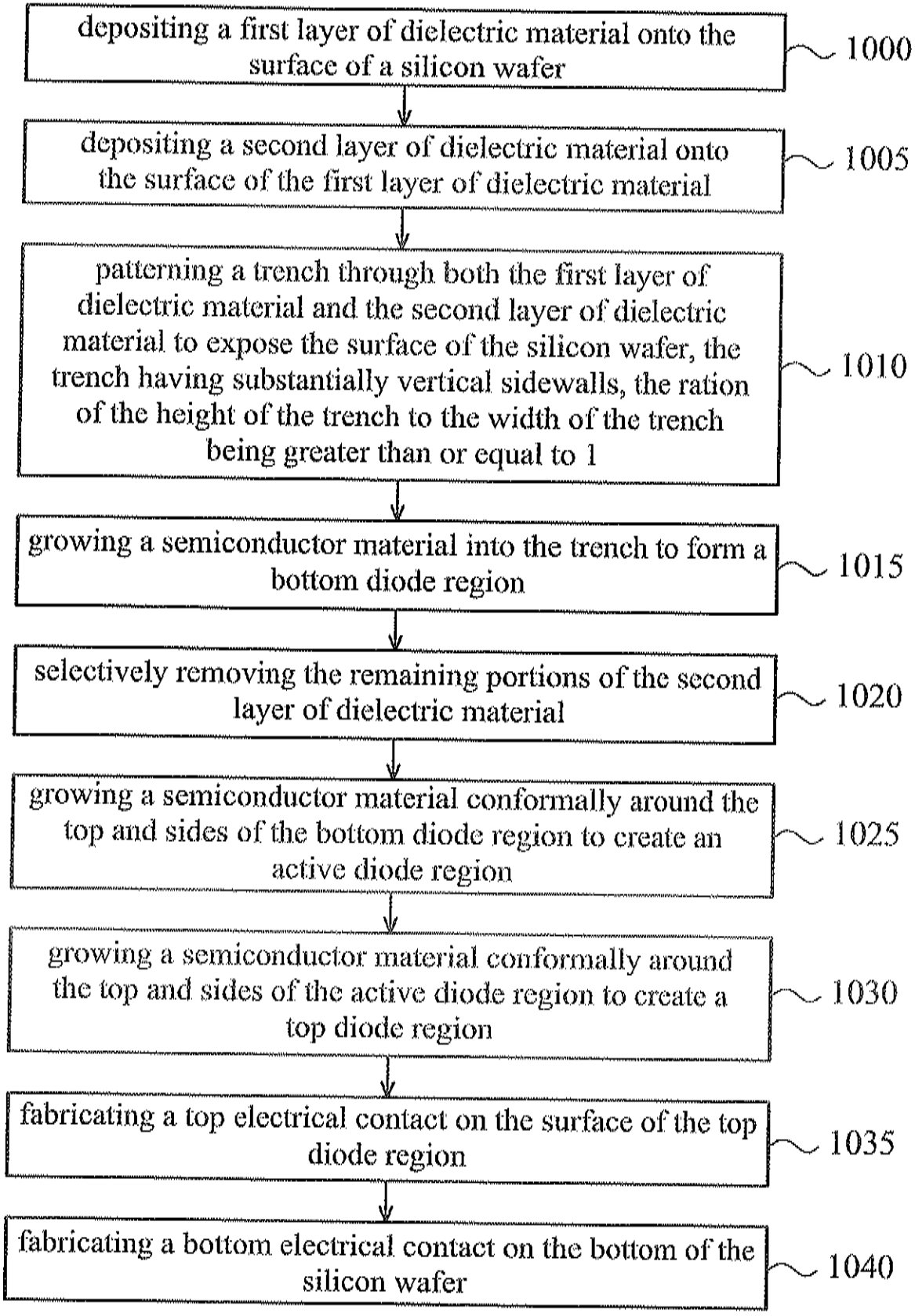

depositing a first layer of dielectric material onto the surface of a silicon wafer
1000
depositing a second layer of dielectric material onto the surface of the first layer of dielectric material
1005
patterning a trench through both the first layer of dielectric material and the second layer of dielectric material to expose the surface of the silicon wafer, the trench having substantially vertical sidewalls, the ration of the height of the trench to the width of the trench being greater than or equal to 1
1010
growing a semiconductor material into the trench to form a bottom diode region
1015
selectively removing the remaining portions of the second layer of dielectric material
1020
growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region
1025
growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region
1030
fabricating a top electrical contact on the surface of the top diode region
1035
fabricating a bottom electrical contact on the bottom of the silicon wafer
1040

Figure 11

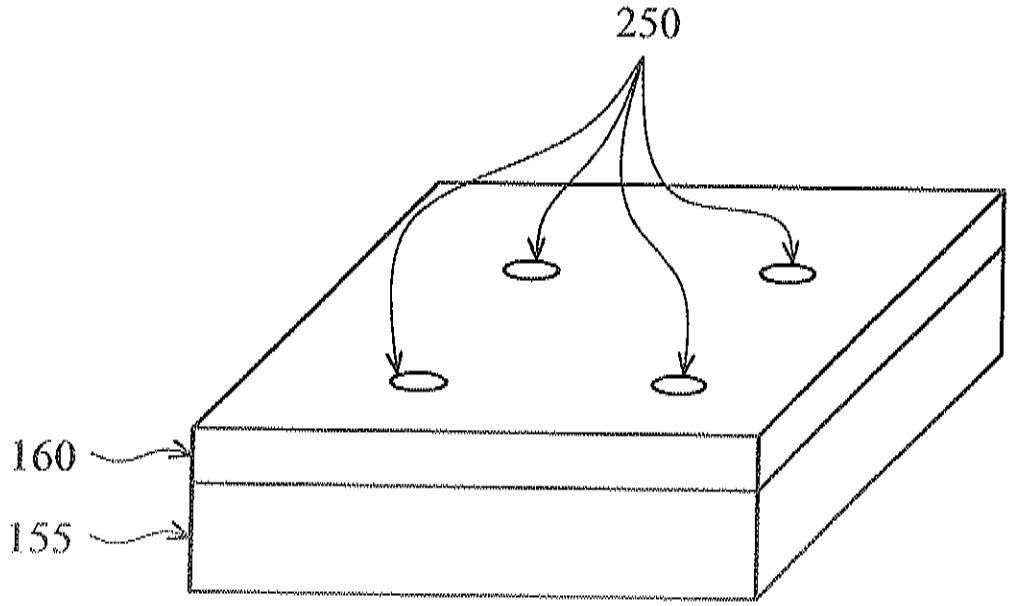


Figure 12

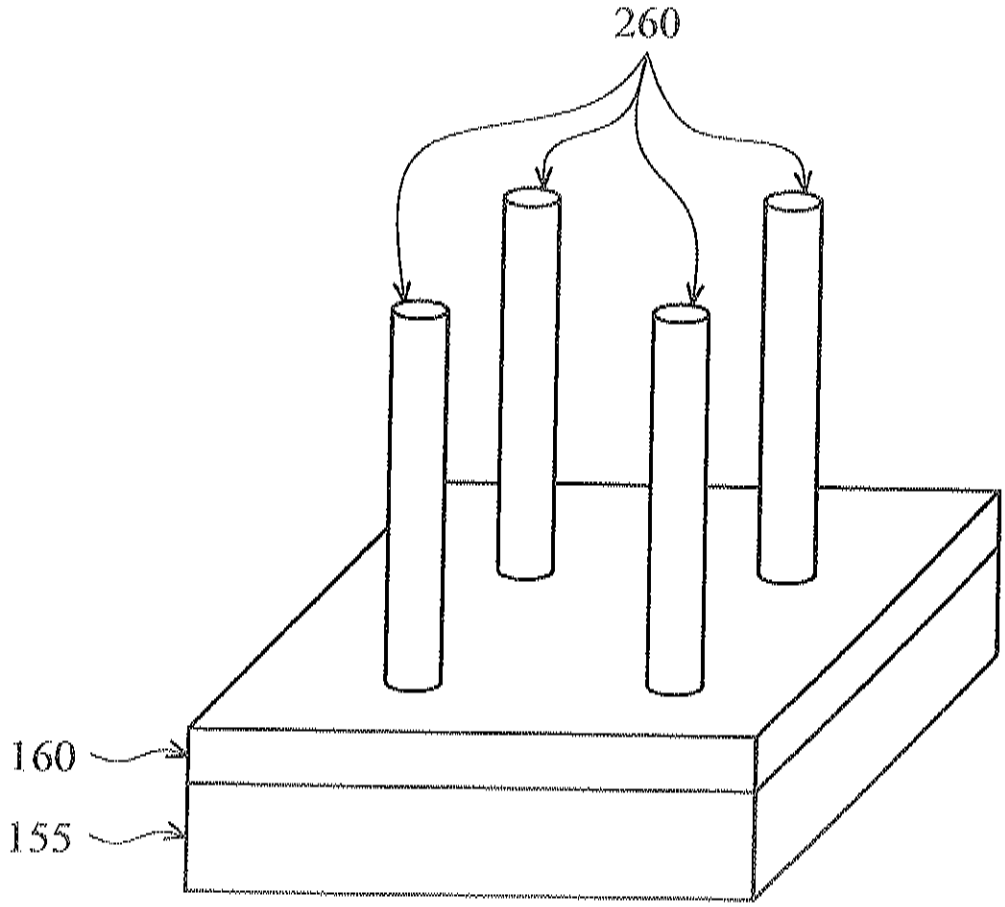


Figure 13

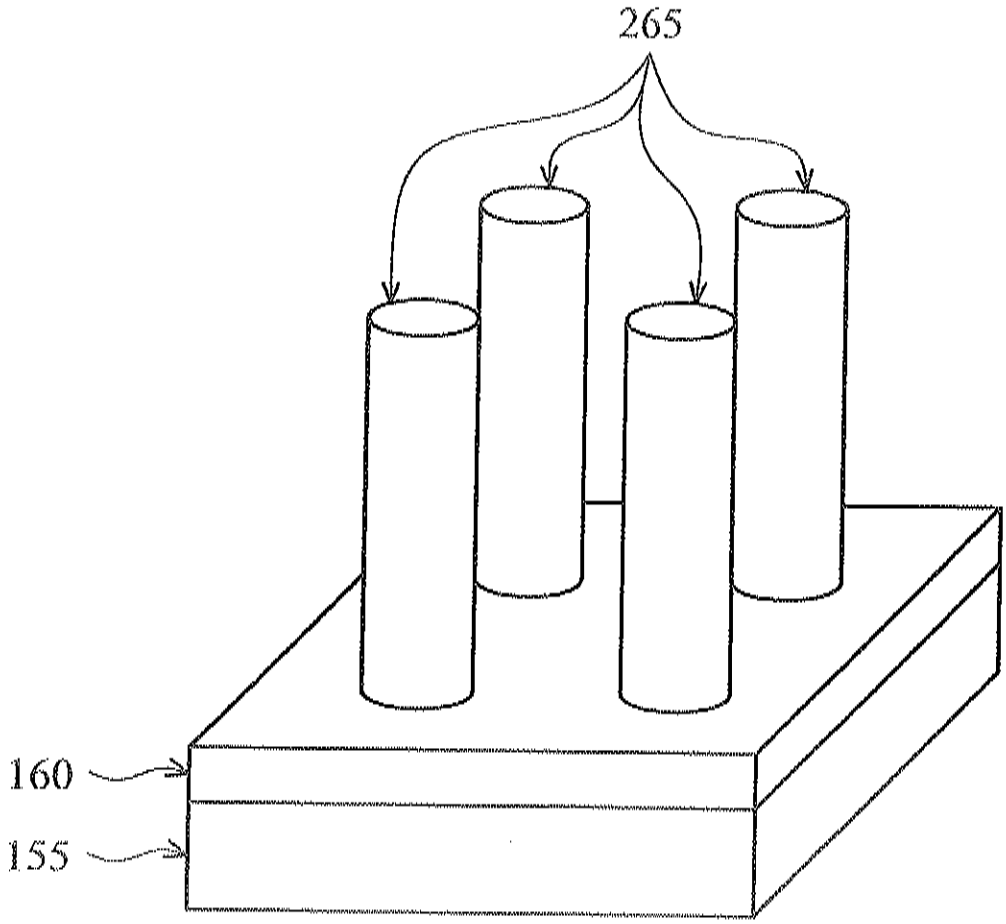


Figure 14

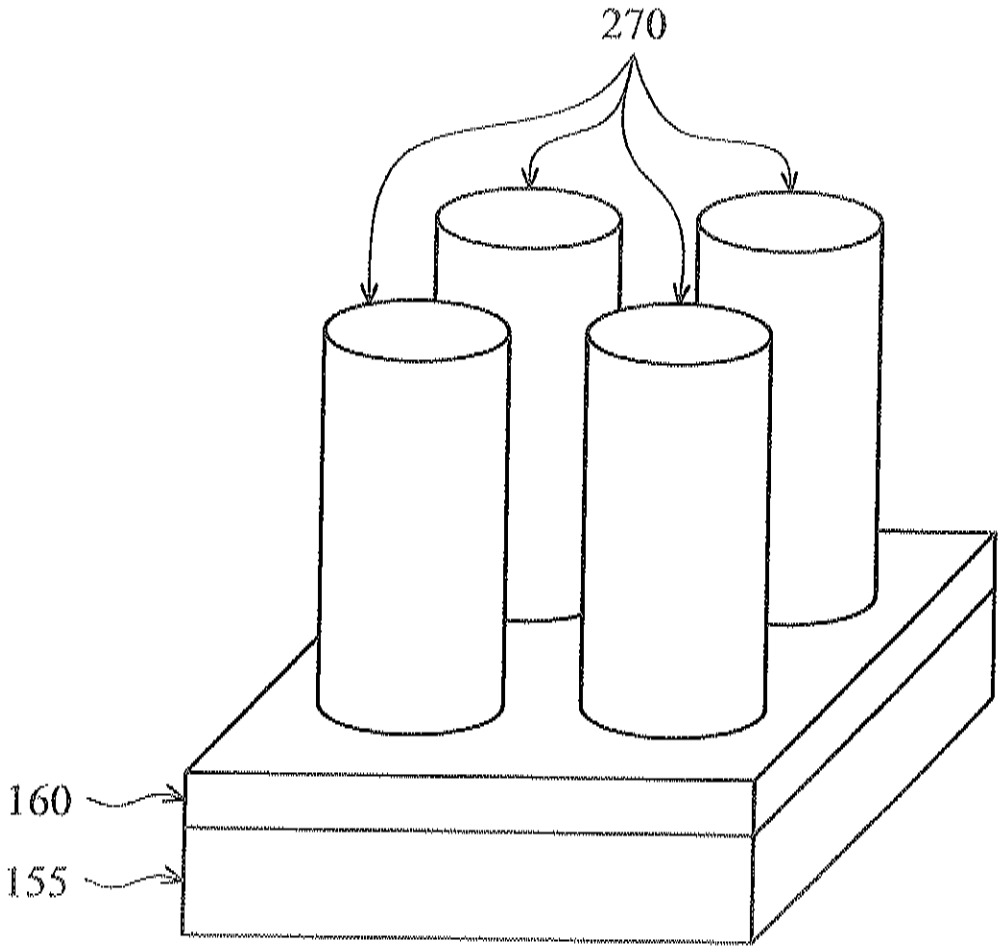


Figure 15

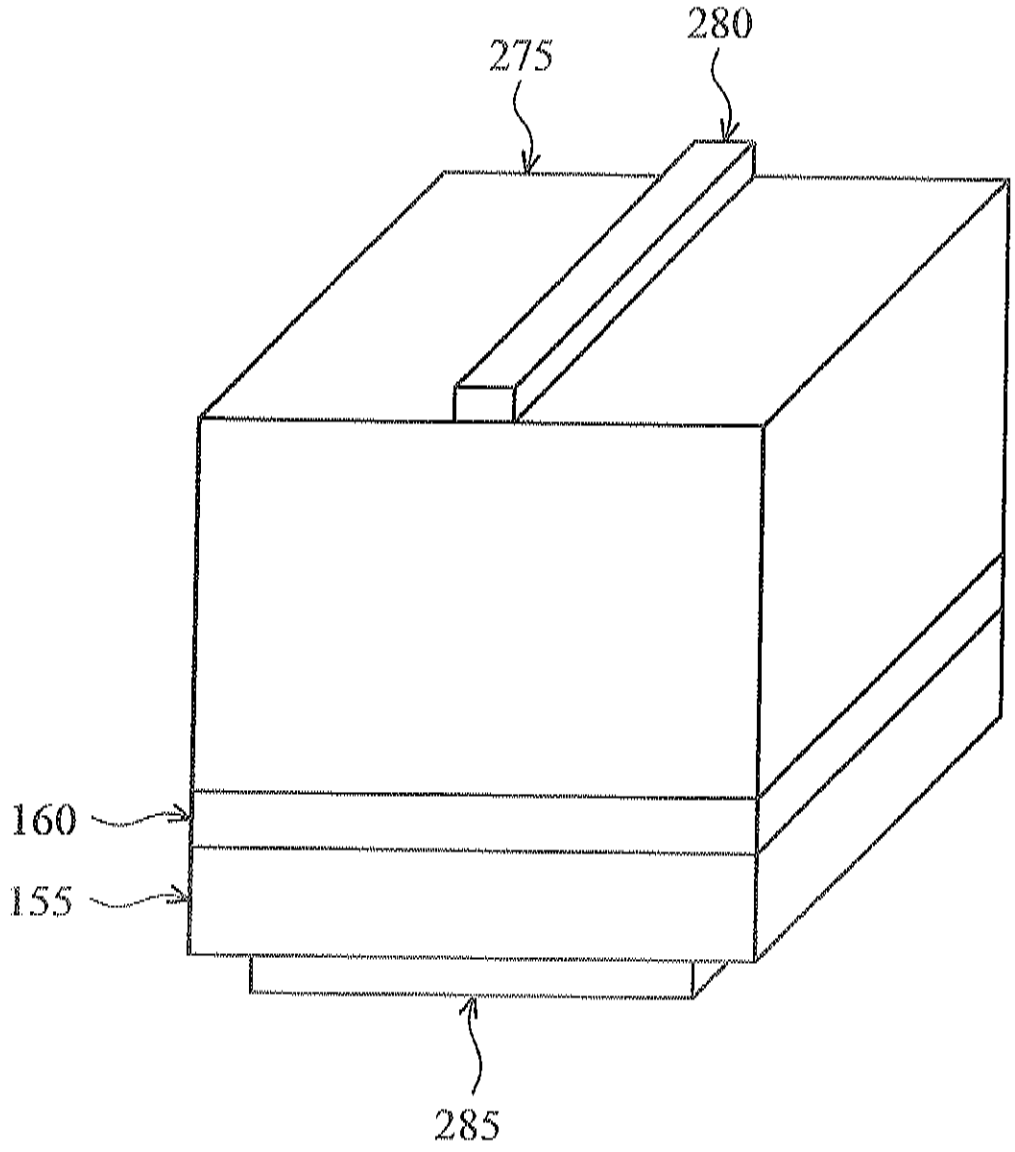


Figure 16

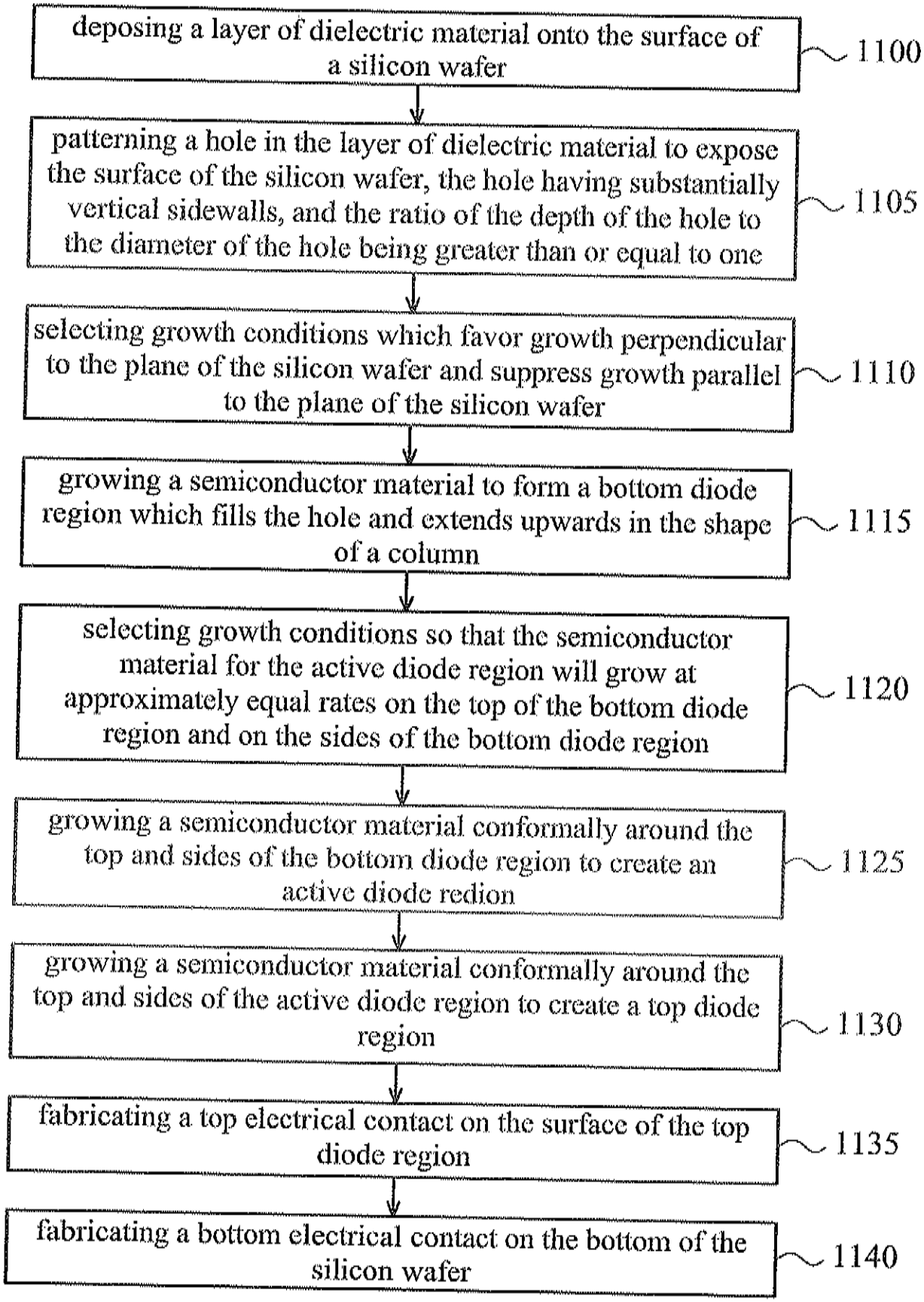

deposing a layer of dielectric material onto the surface of a silicon wafer
1100
patterning a hole in the layer of dielectric material to expose the surface of the silicon wafer, the hole having substantially vertical sidewalls, and the ratio of the depth of the hole to the diameter of the hole being greater than or equal to one
1105
selecting growth conditions which favor growth perpendicular to the plane of the silicon wafer and suppress growth parallel to the plane of the silicon wafer
1110
growing a semiconductor material to form a bottom diode region which fills the hole and extends upwards in the shape of a column
1115
selecting growth conditions so that the semiconductor material for the active diode region will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region
1120
growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode redion
1125
growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region
1130
fabricating a top electrical contact on the surface of the top diode region
1135
fabricating a bottom electrical contact on the bottom of the silicon wafer
1140

Figure 17

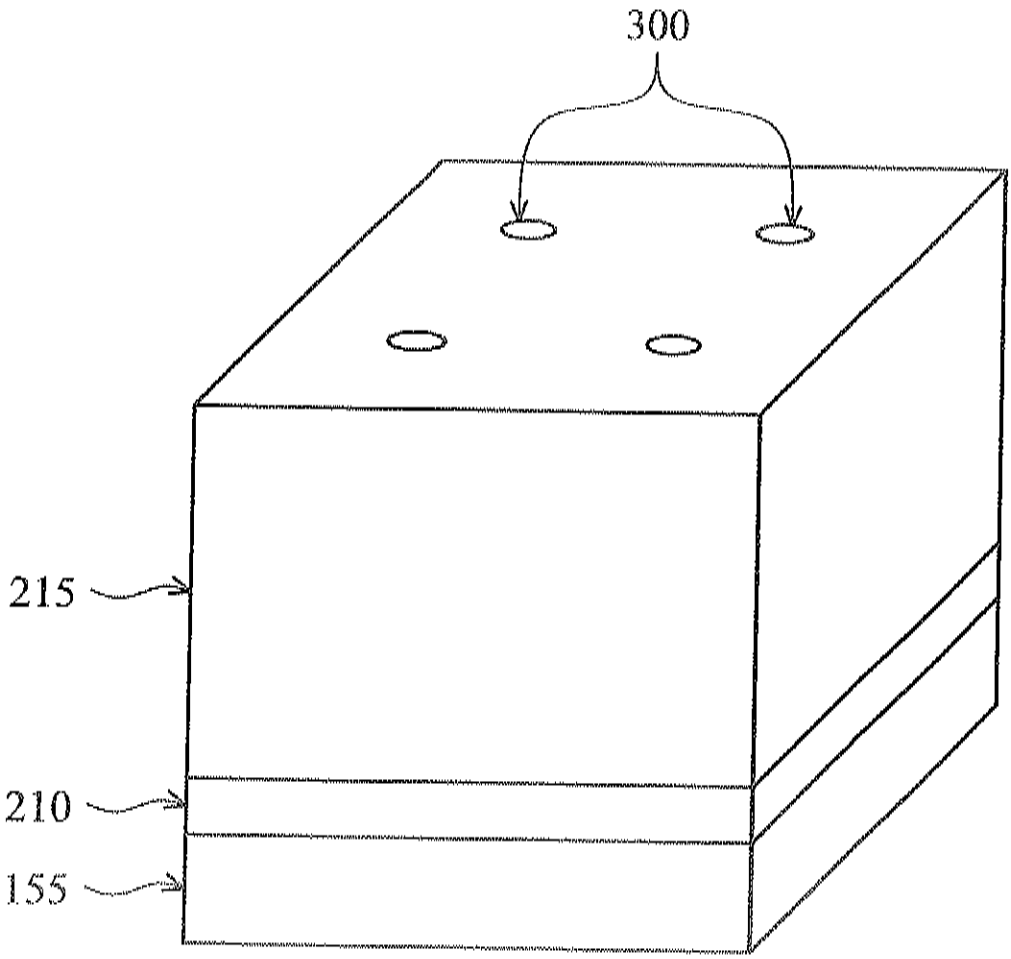


Figure 18

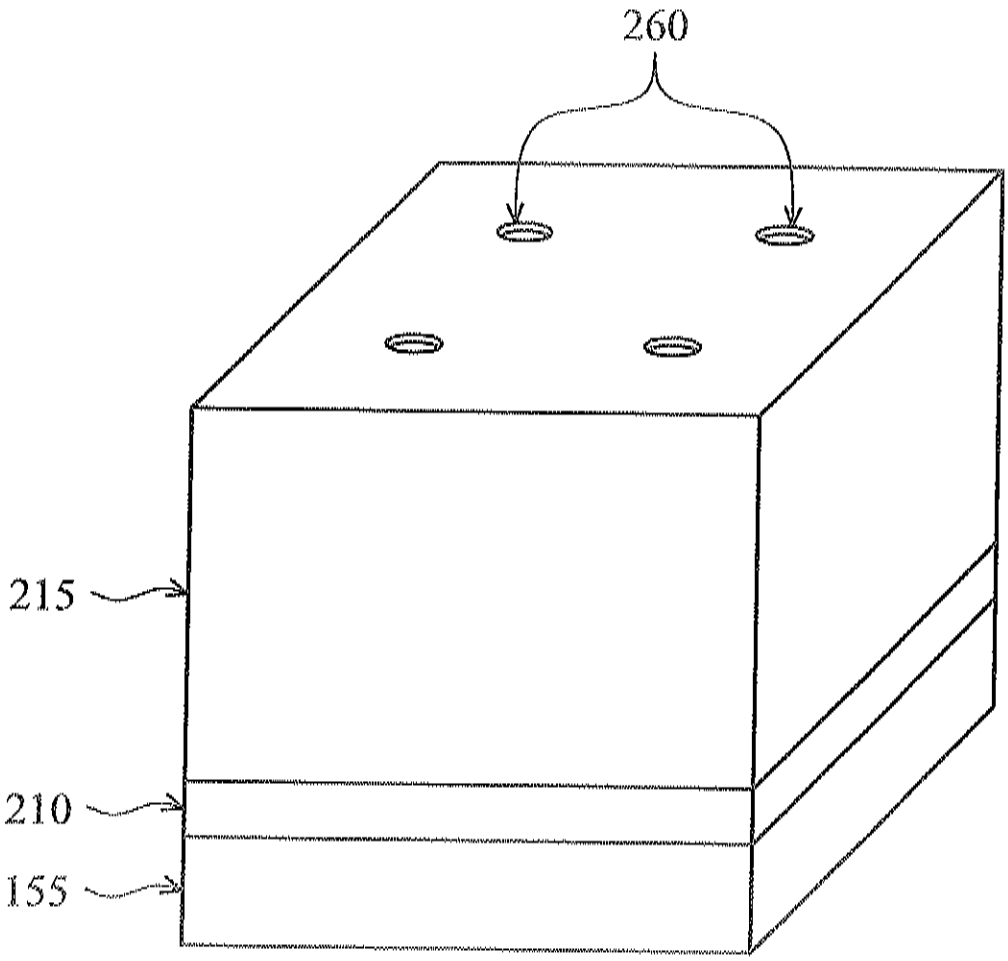


Figure 19

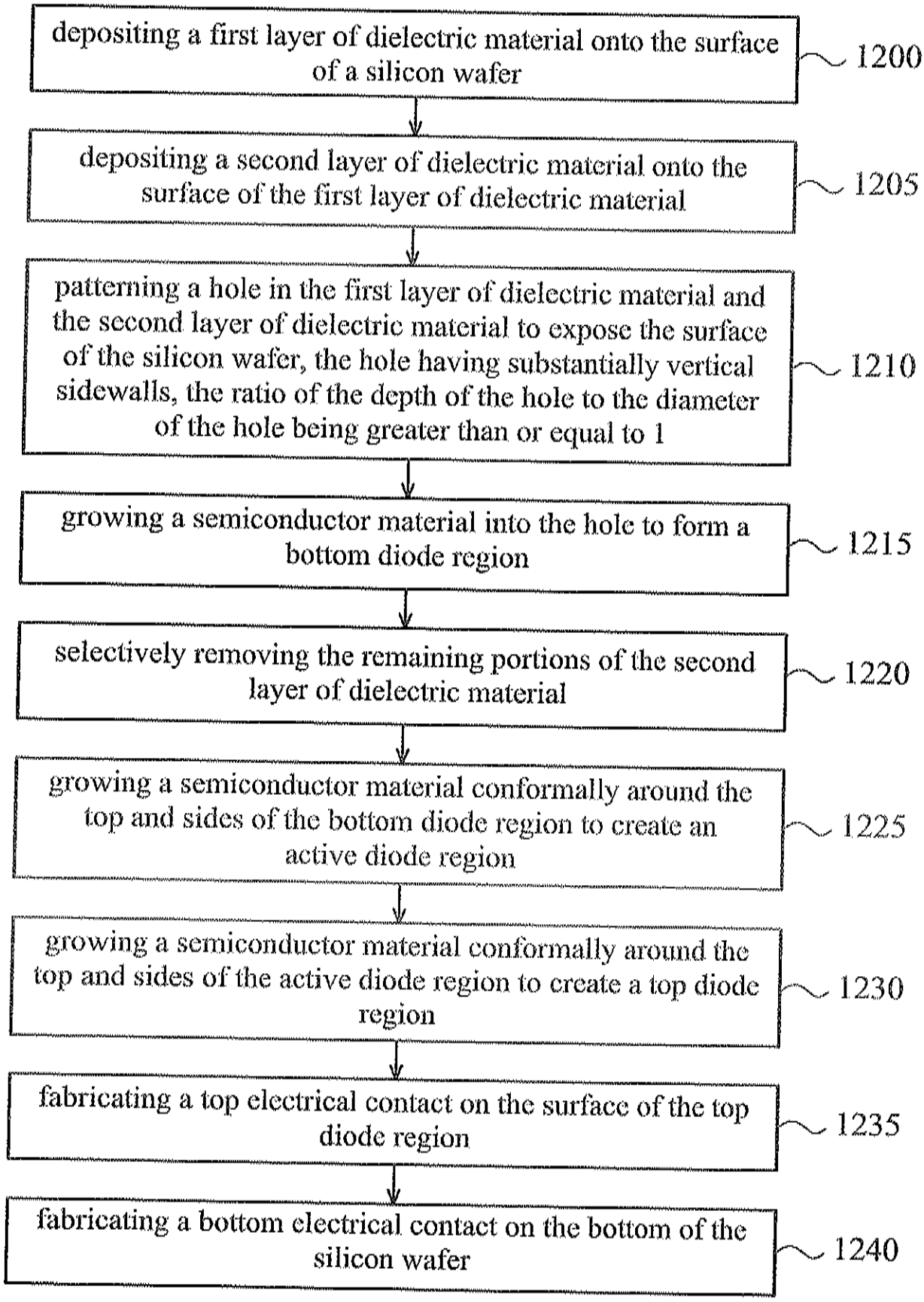

depositing a first layer of dielectric material onto the surface of a silicon wafer
1200
depositing a second layer of dielectric material onto the surface of the first layer of dielectric material
1205
patterning a hole in the first layer of dielectric material and the second layer of dielectric material to expose the surface of the silicon wafer, the hole having substantially vertical sidewalls, the ratio of the depth of the hole to the diameter of the hole being greater than or equal to 1
1210
growing a semiconductor material into the hole to form a bottom diode region
1215
selectively removing the remaining portions of the second layer of dielectric material
1220
growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region
1225
growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region
1230
fabricating a top electrical contact on the surface of the top diode region
1235
fabricating a bottom electrical contact on the bottom of the silicon wafer
1240

Figure 20

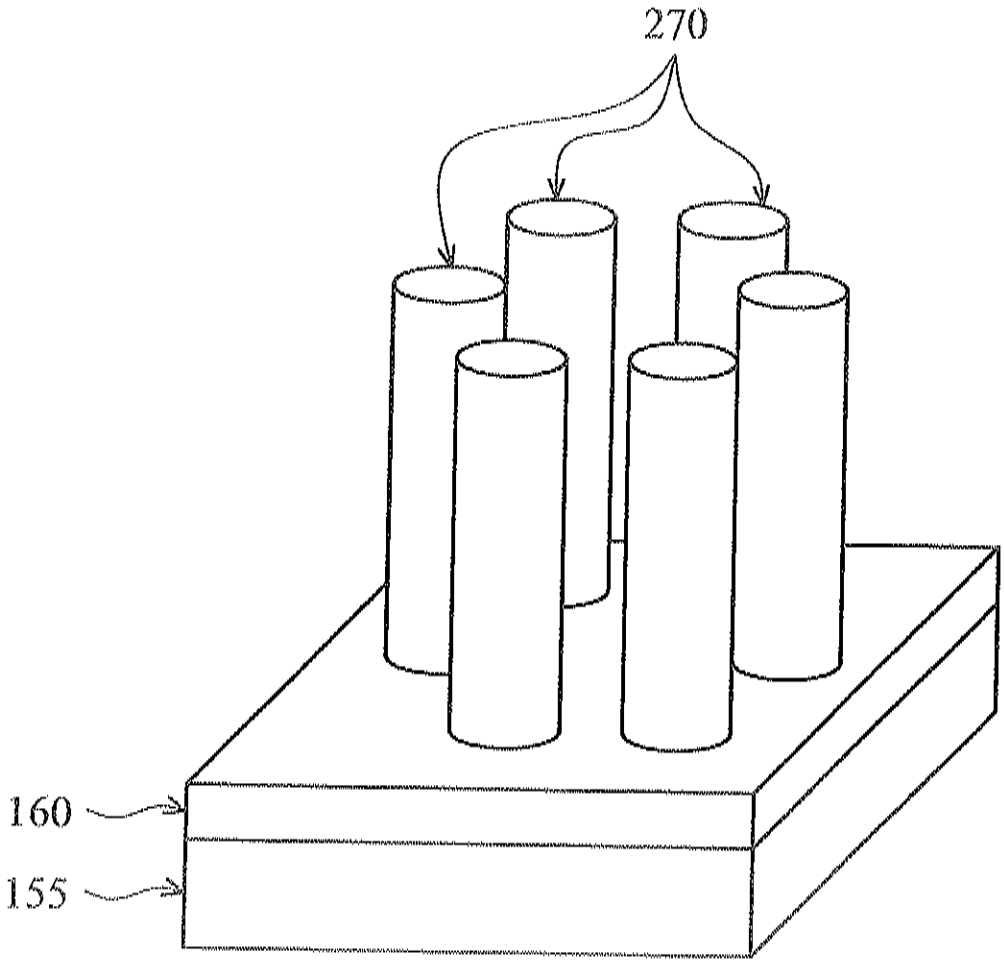


Figure 21

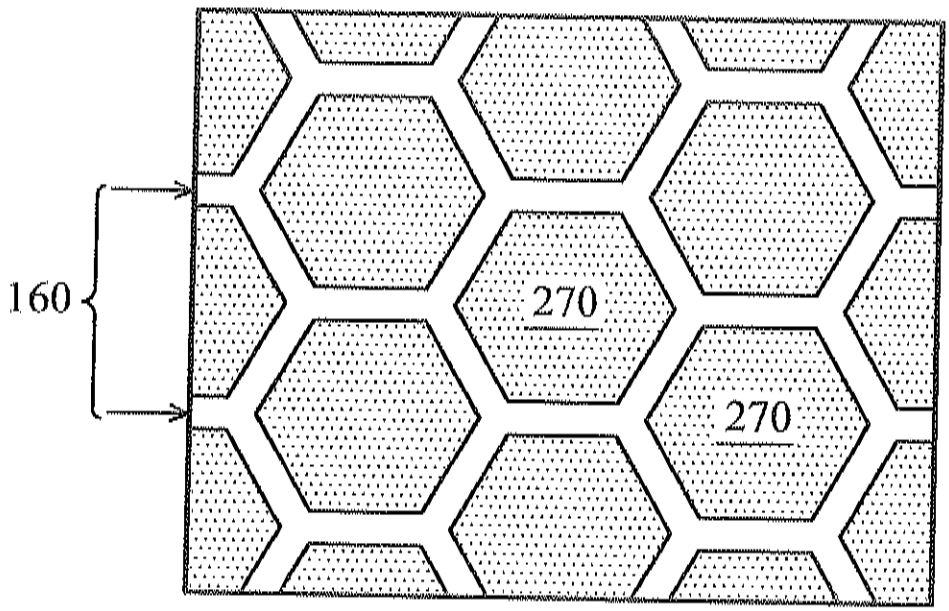


Figure 22

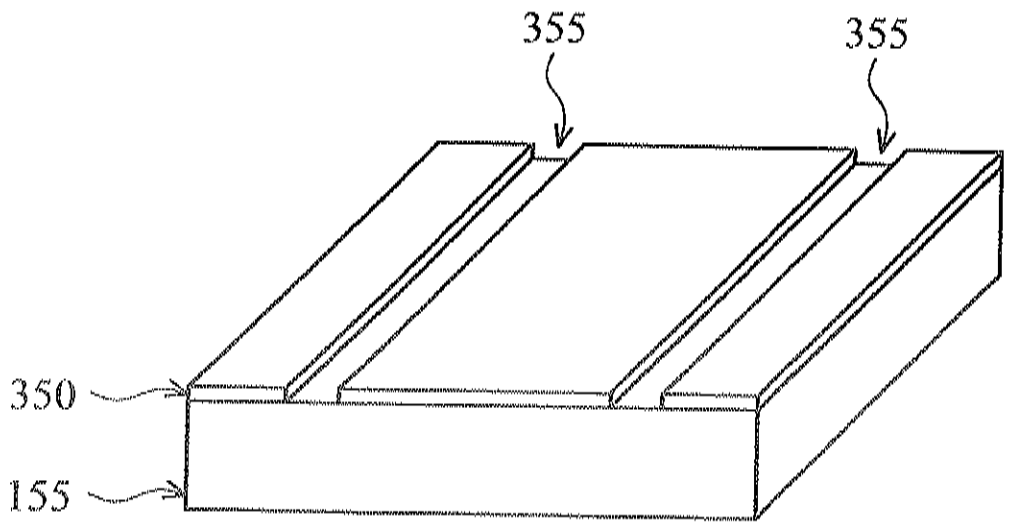


Figure 23

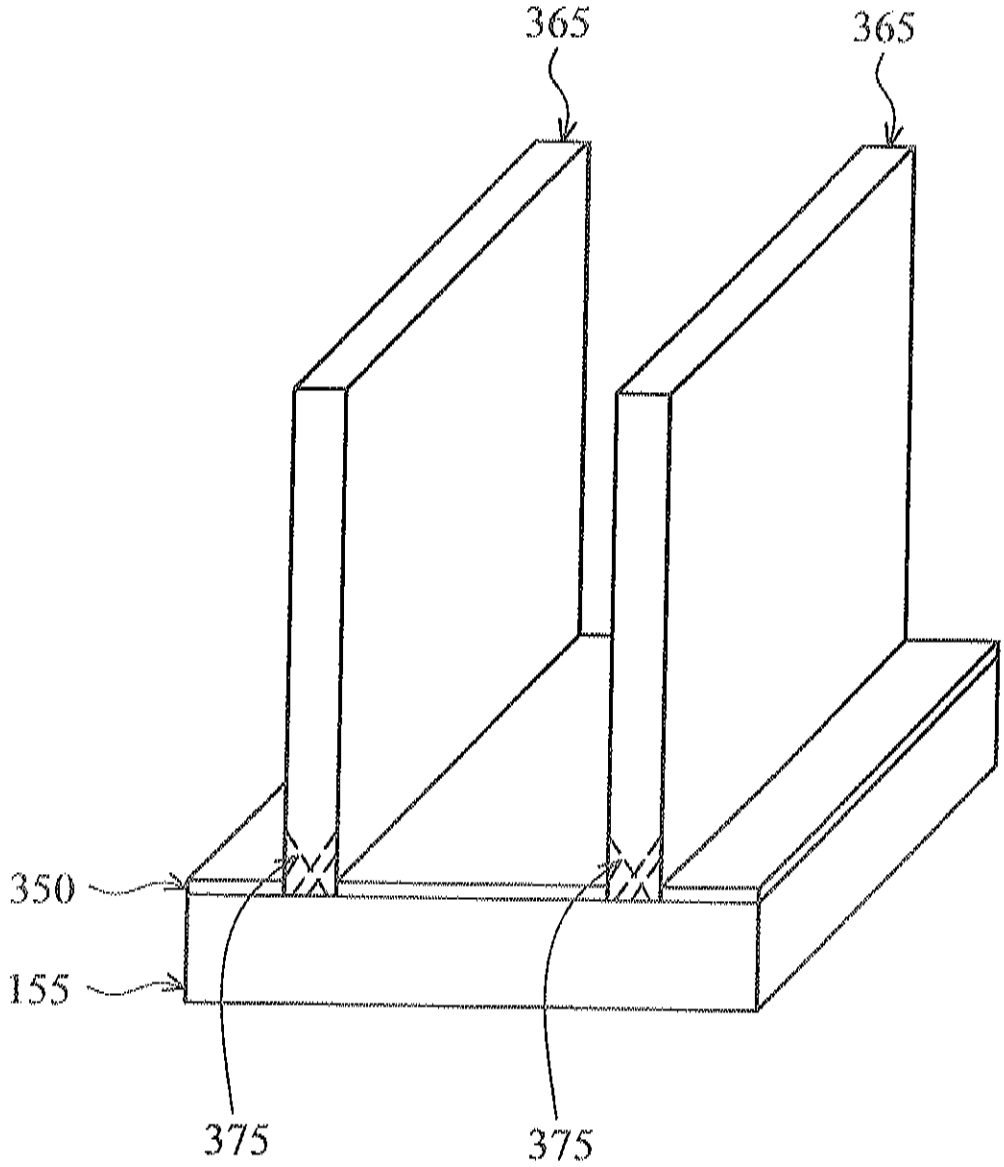


Figure 24

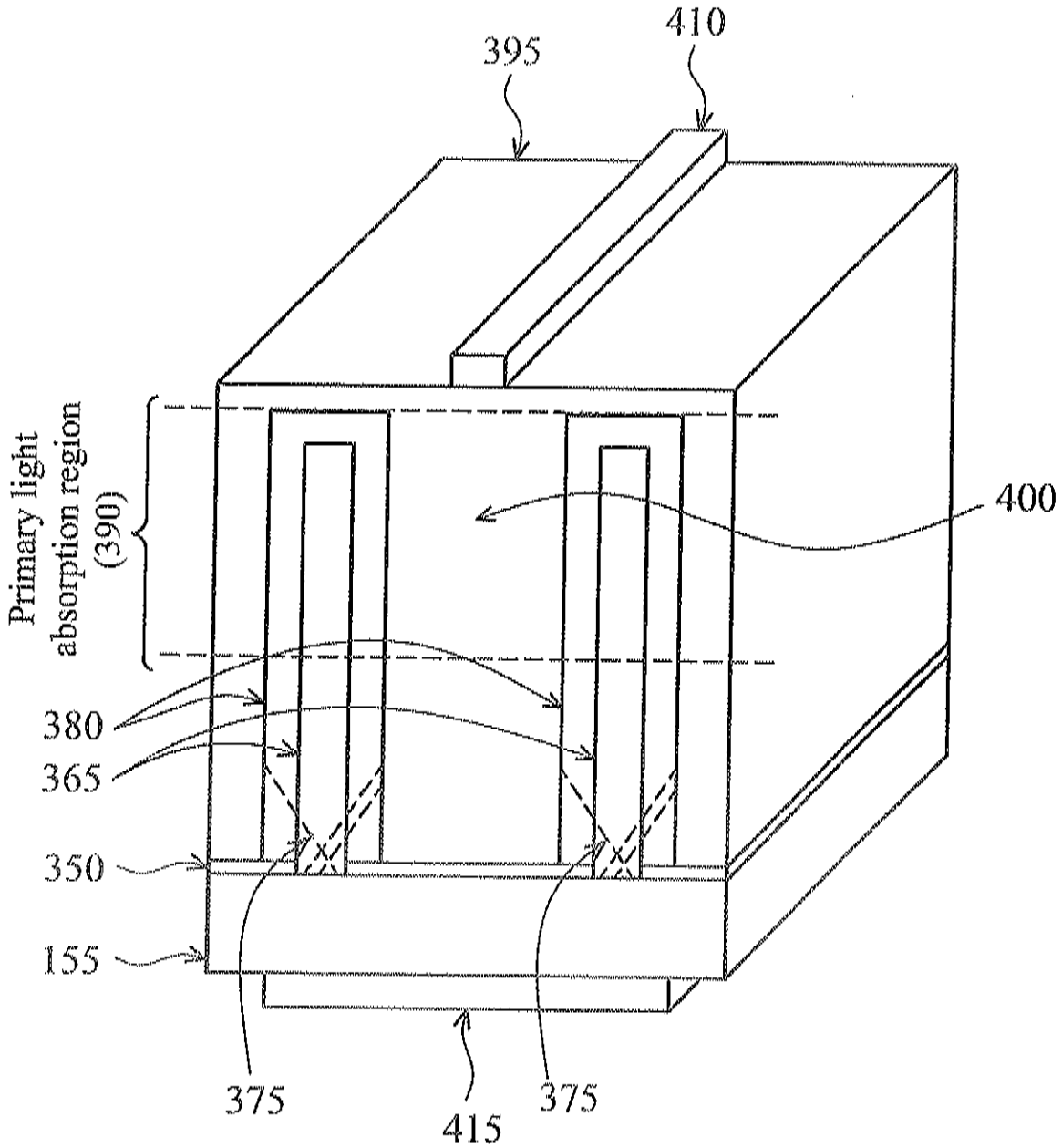

395
410
Primary light absorption region (390)
400
380
365
350
155
375
415
375

Figure 25

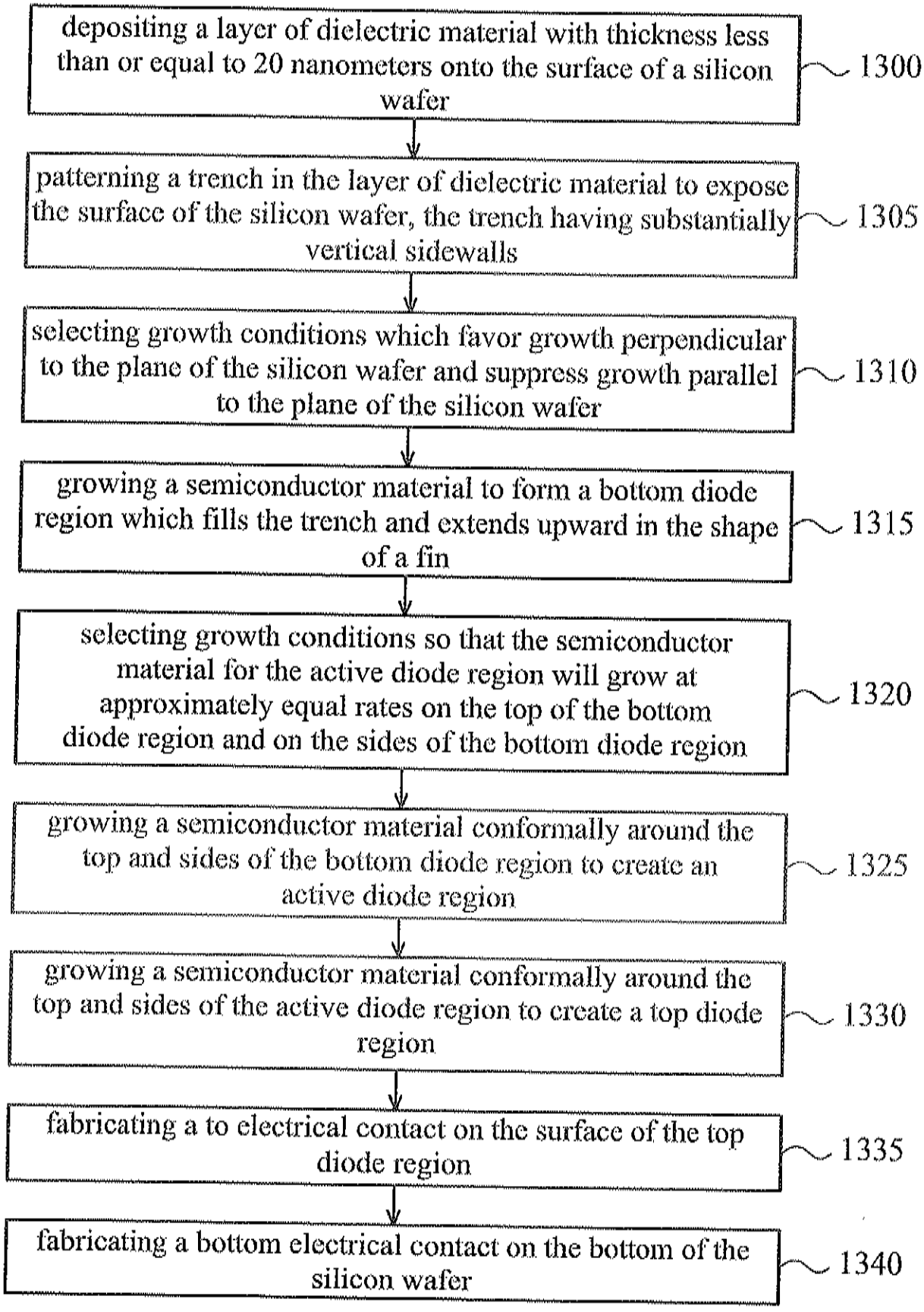

depositing a layer of dielectric material with thickness less than or equal to 20 nanometers onto the surface of a silicon wafer
1300
patterning a trench in the layer of dielectric material to expose the surface of the silicon wafer, the trench having substantially vertical sidewalls
1305
selecting growth conditions which favor growth perpendicular to the plane of the silicon wafer and suppress growth parallel to the plane of the silicon wafer
1310
growing a semiconductor material to form a bottom diode region which fills the trench and extends upward in the shape of a fin
1315
selecting growth conditions so that the semiconductor material for the active diode region will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region
1320
growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region
1325
growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region
1330
fabricating a to electrical contact on the surface of the top diode region
1335
fabricating a bottom electrical contact on the bottom of the silicon wafer
1340

Figure 26

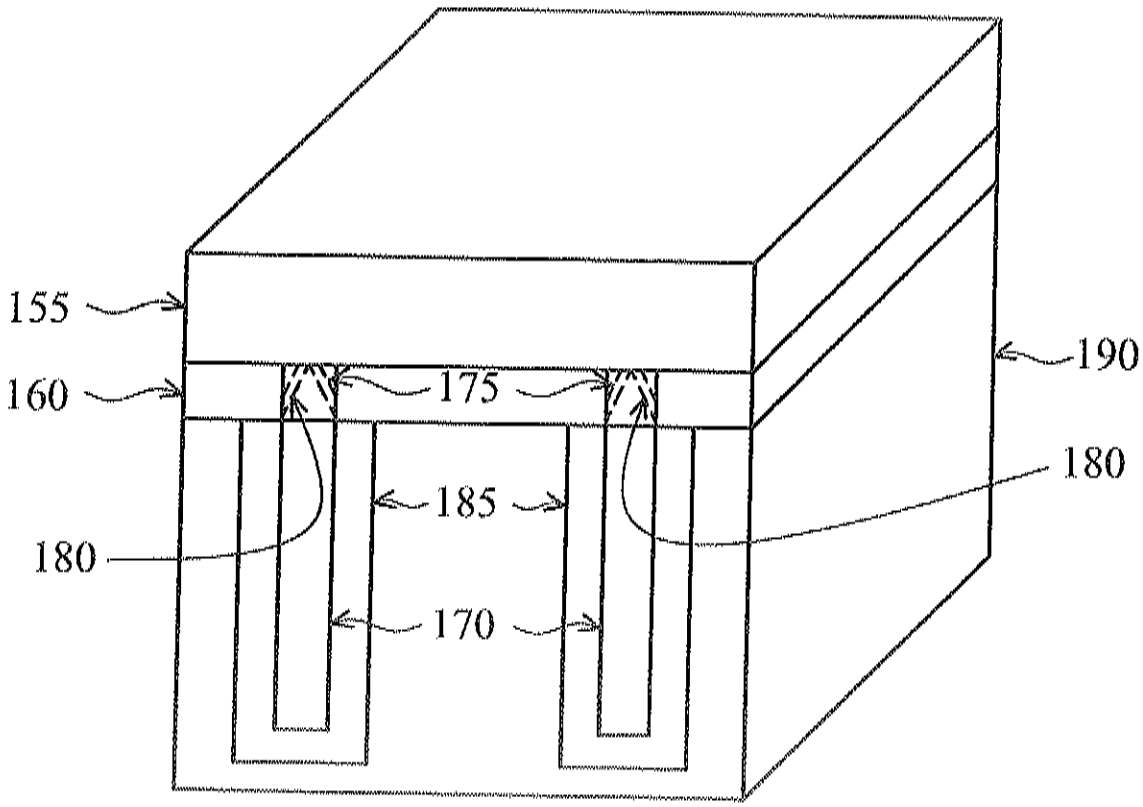


Figure 27

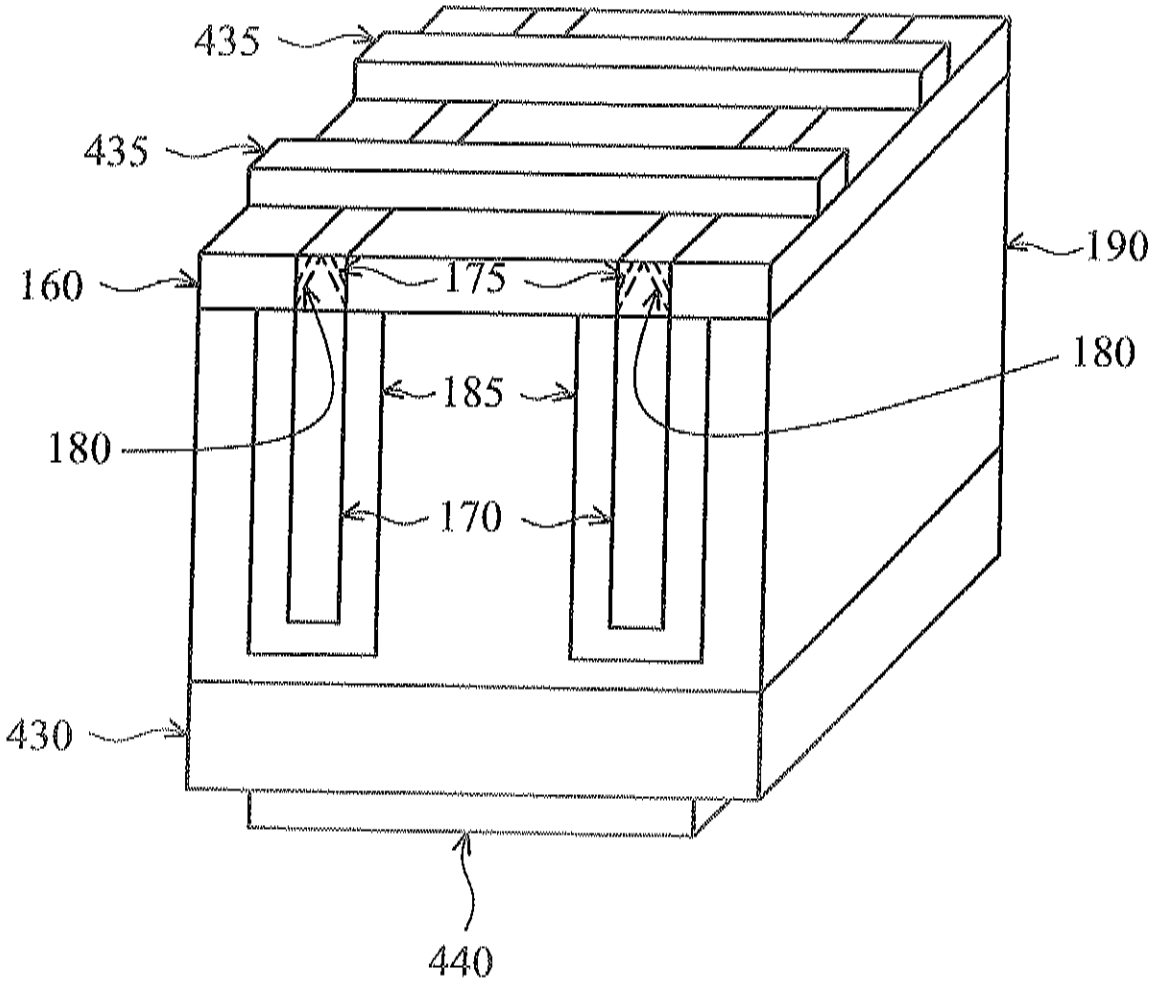


Figure 28

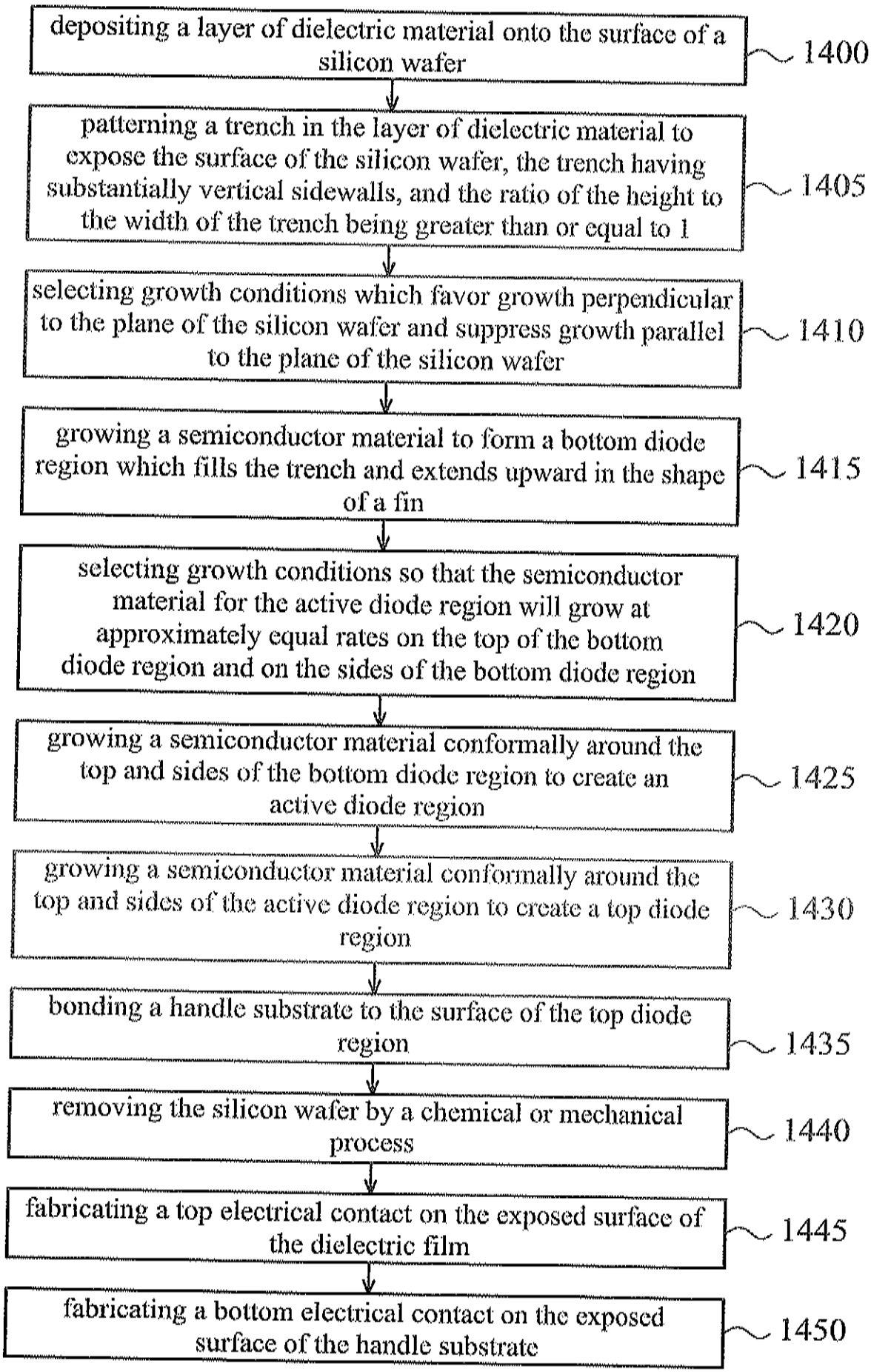

depositing a layer of dielectric material onto the surface of a silicon wafer
1400
patterning a trench in the layer of dielectric material to expose the surface of the silicon wafer, the trench having substantially vertical sidewalls, and the ratio of the height to the width of the trench being greater than or equal to 1
1405
selecting growth conditions which favor growth perpendicular to the plane of the silicon wafer and suppress growth parallel to the plane of the silicon wafer
1410
growing a semiconductor material to form a bottom diode region which fills the trench and extends upward in the shape of a fin
1415
selecting growth conditions so that the semiconductor material for the active diode region will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region
1420
growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region
1425
growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region
1430
bonding a handle substrate to the surface of the top diode region
1435
removing the silicon wafer by a chemical or mechanical process
1440
fabricating a top electrical contact on the exposed surface of the dielectric film
1445
fabricating a bottom electrical contact on the exposed surface of the handle substrate
1450

Figure 29

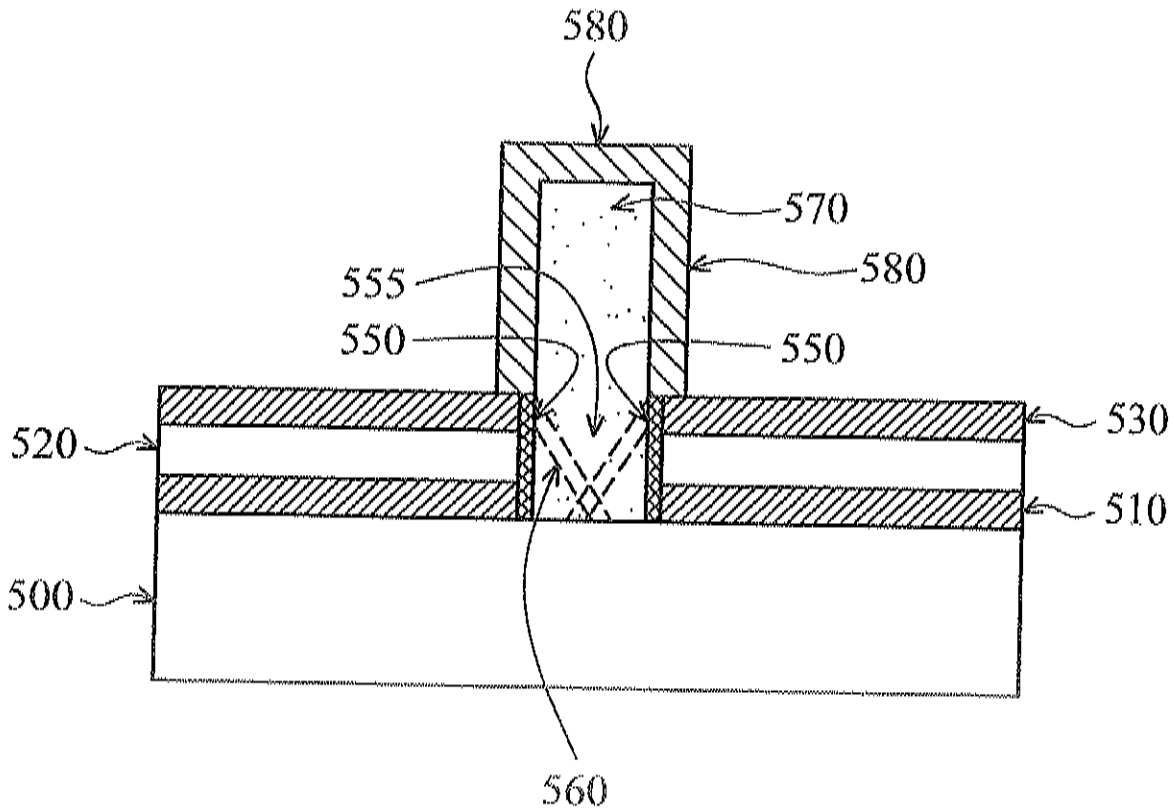


Figure 30

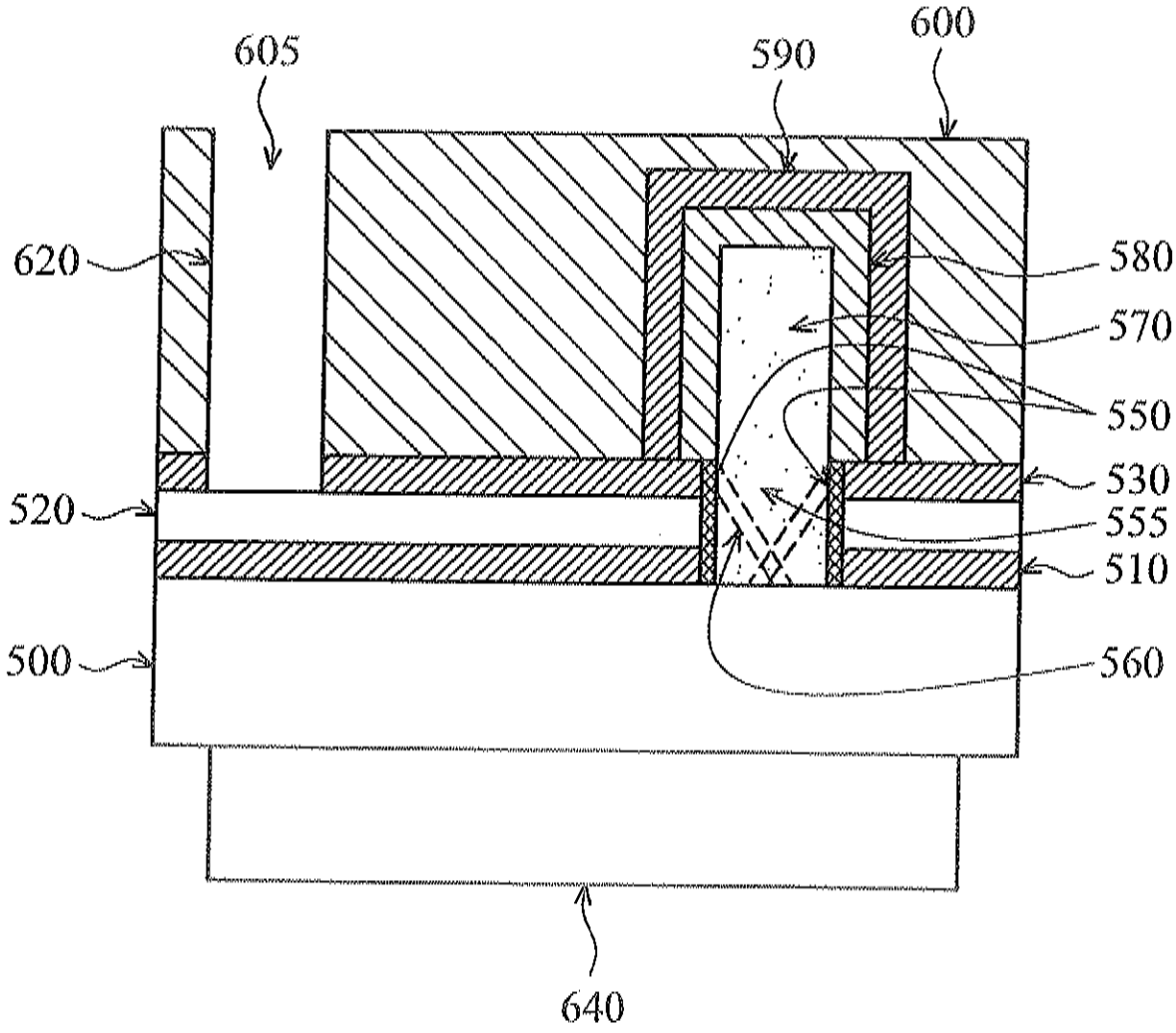


Figure 31

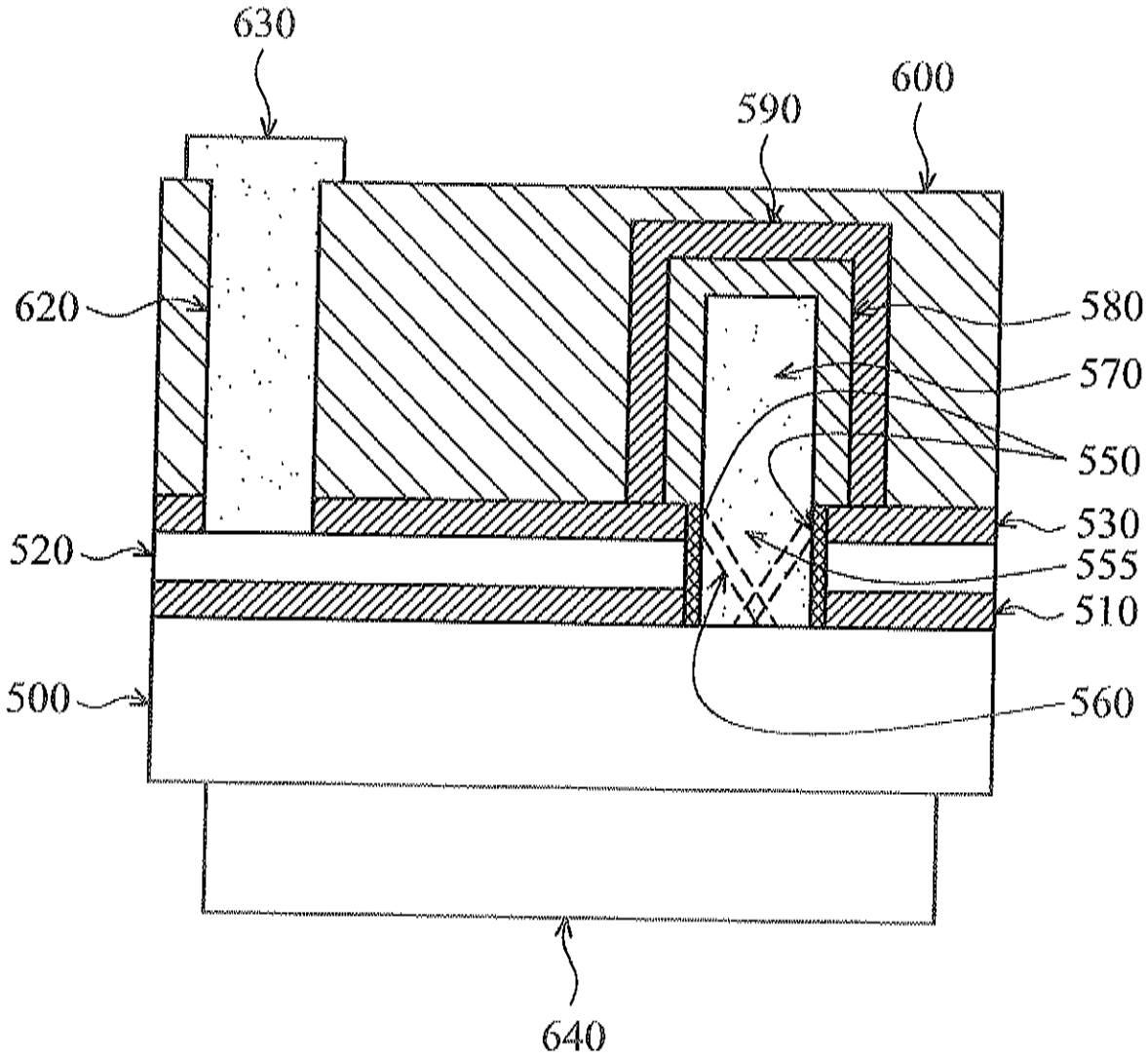


Figure 32

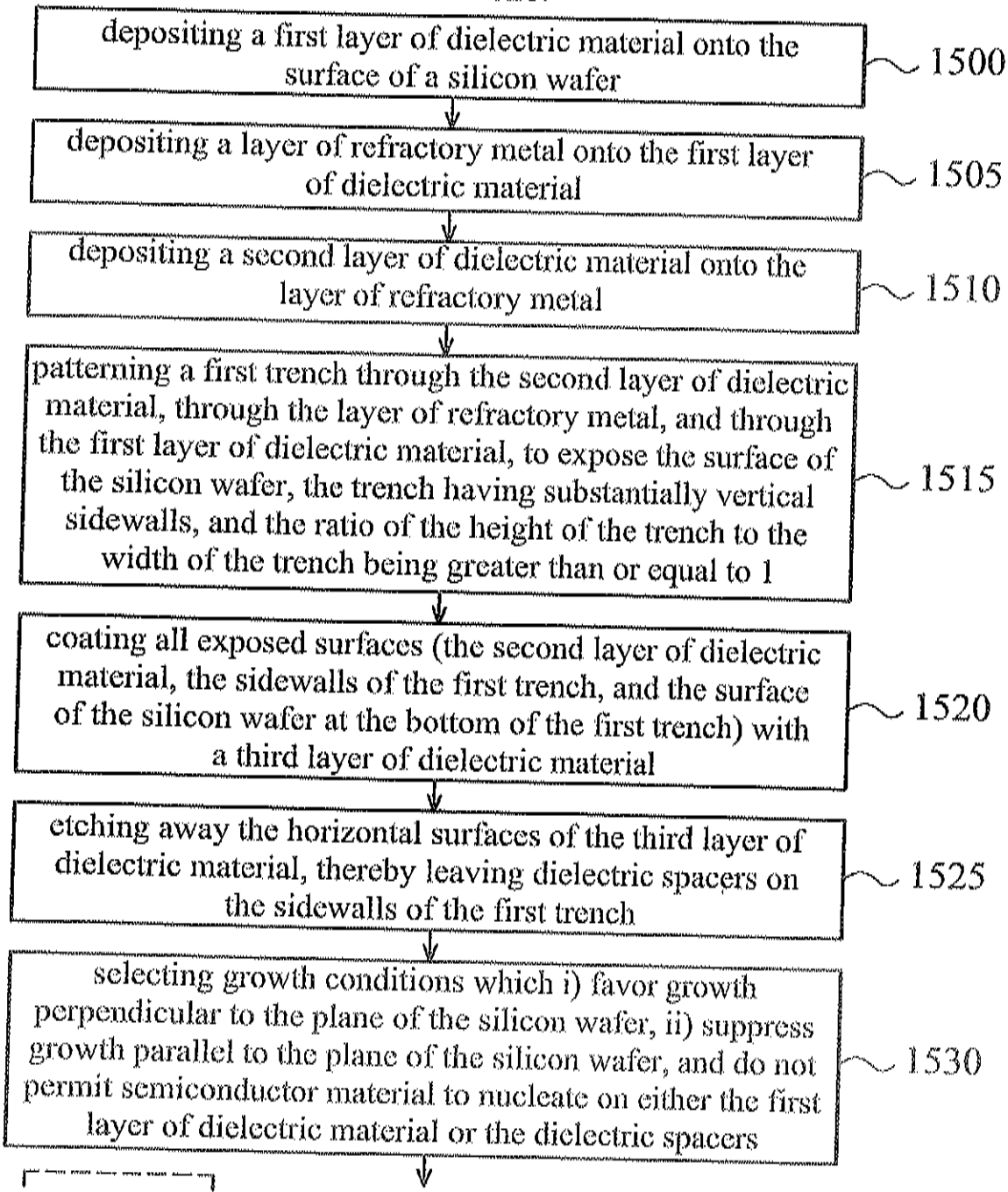


Figure 33-1

Figure 33-2

Figure 33-1

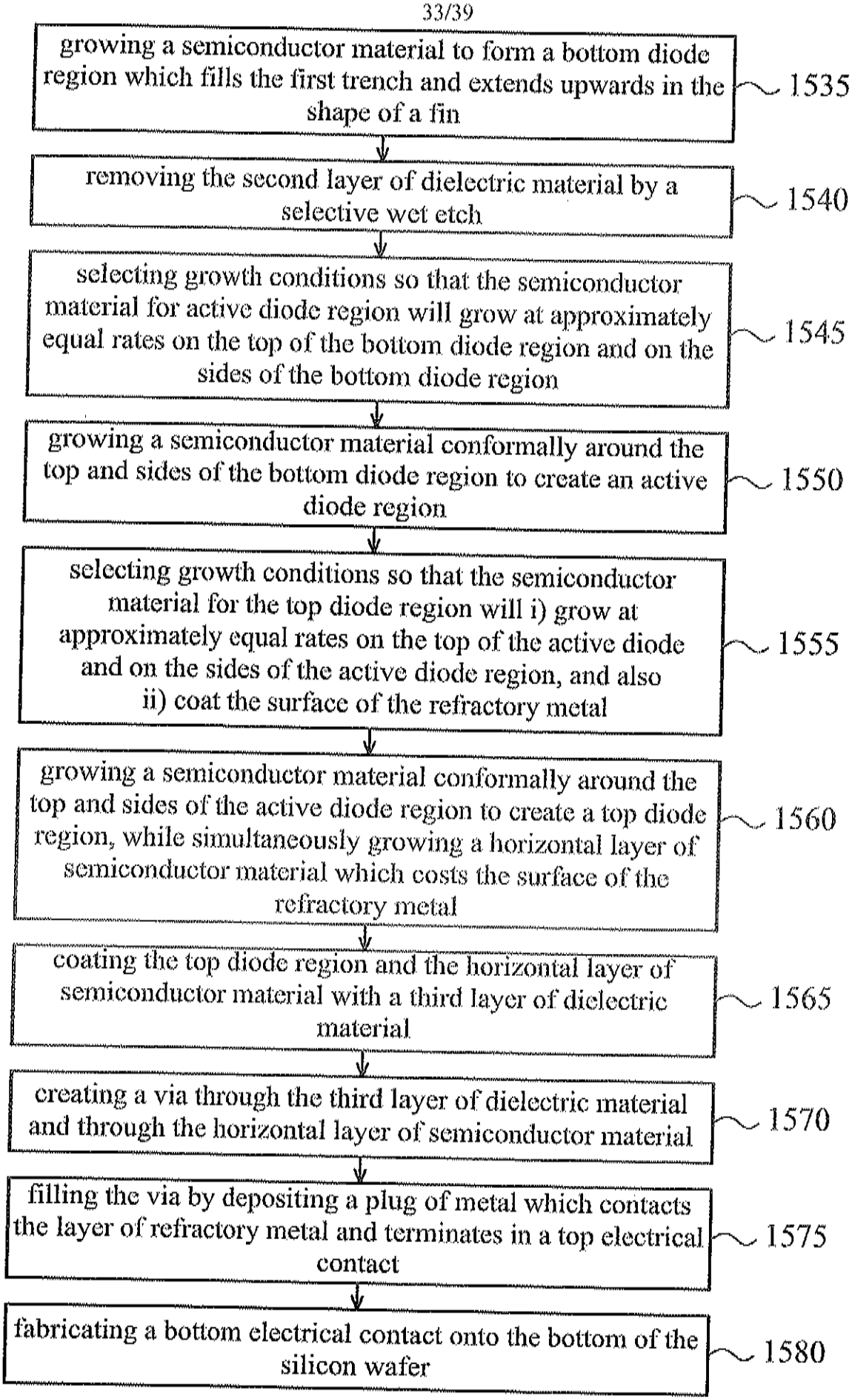

growing a semiconductor material to form a bottom diode region which fills the first trench and extends upwards in the shape of a fin
1535
removing the second layer of dielectric material by a selective wet etch
1540
selecting growth conditions so that the semiconductor material for active diode region will grow at approximately equal rates on the top of the bottom diode region and on the sides of the bottom diode region
1545
growing a semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region
1550
selecting growth conditions so that the semiconductor material for the top diode region will i) grow at approximately equal rates on the top of the active diode and on the sides of the active diode region, and also ii) coat the surface of the refractory metal
1555
growing a semiconductor material conformally around the top and sides of the active diode region to create a top diode region, while simultaneously growing a horizontal layer of semiconductor material which costs the surface of the refractory metal
1560
coating the top diode region and the horizontal layer of semiconductor material with a third layer of dielectric material
1565
creating a via through the third layer of dielectric material and through the horizontal layer of semiconductor material
1570
filling the via by depositing a plug of metal which contacts the layer of refractory metal and terminates in a top electrical contact
1575
fabricating a bottom electrical contact onto the bottom of the silicon wafer
1580

Figure 33-2

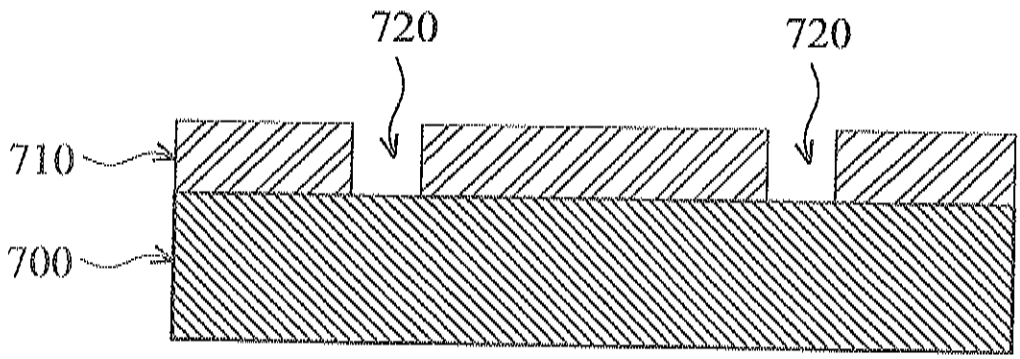


Figure 34

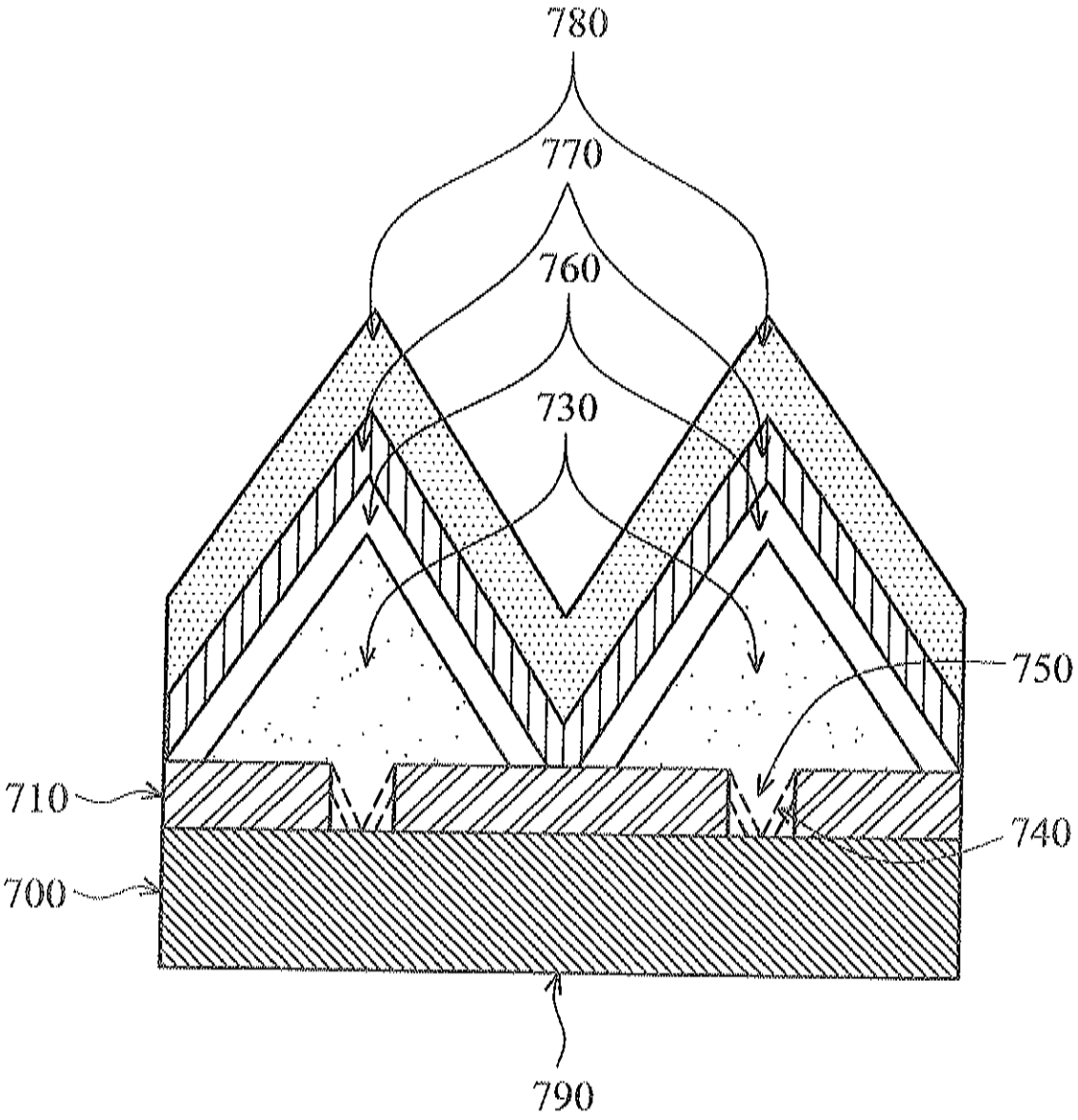


Figure 35

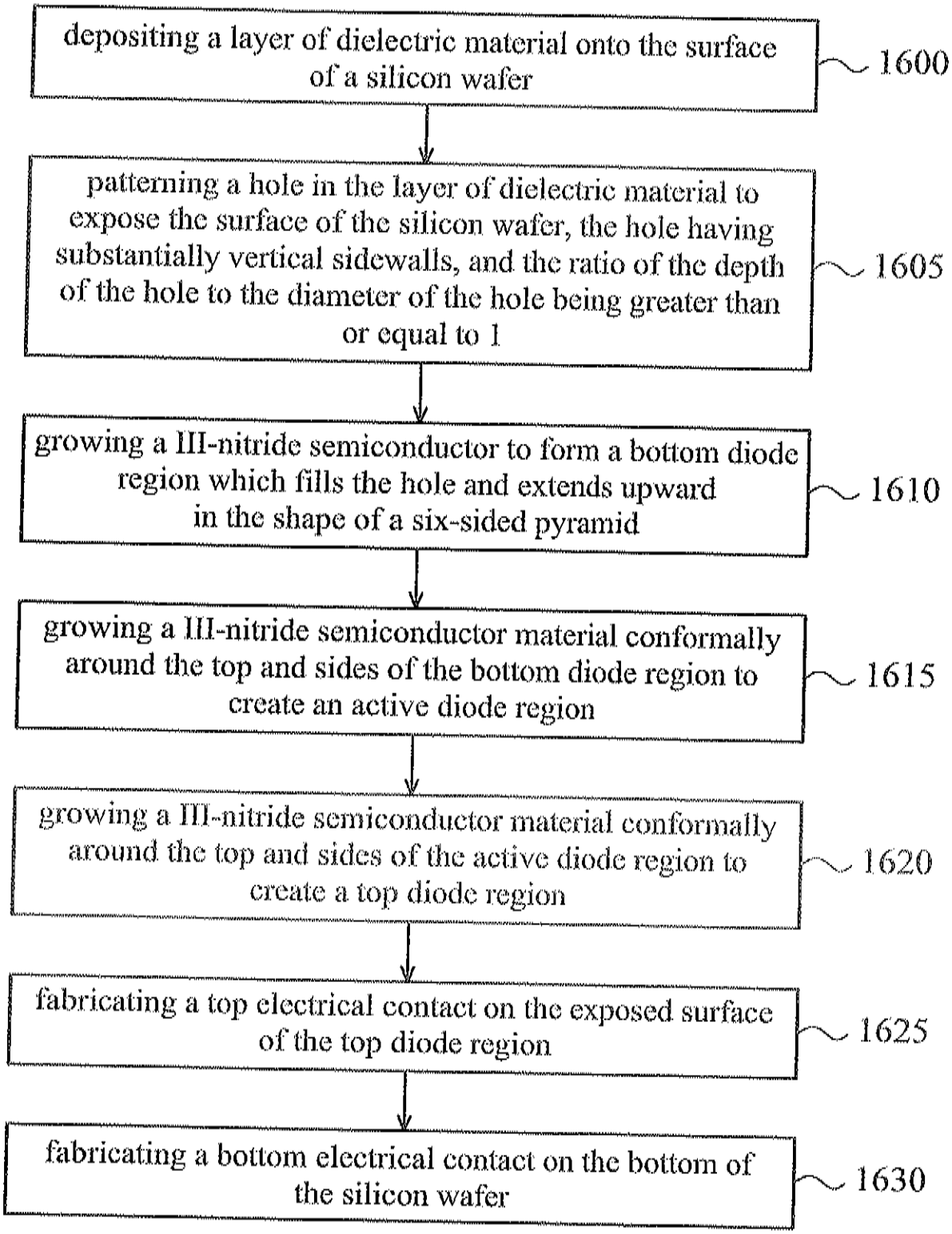

depositing a layer of dielectric material onto the surface of a silicon wafer
1600
patterning a hole in the layer of dielectric material to expose the surface of the silicon wafer, the hole having substantially vertical sidewalls, and the ratio of the depth of the hole to the diameter of the hole being greater than or equal to 1
1605
growing a III-nitride semiconductor to form a bottom diode region which fills the hole and extends upward in the shape of a six-sided pyramid
1610
growing a III-nitride semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region
1615
growing a III-nitride semiconductor material conformally around the top and sides of the active diode region to create a top diode region
1620
fabricating a top electrical contact on the exposed surface of the top diode region
1625
fabricating a bottom electrical contact on the bottom of the silicon wafer
1630

Figure 36

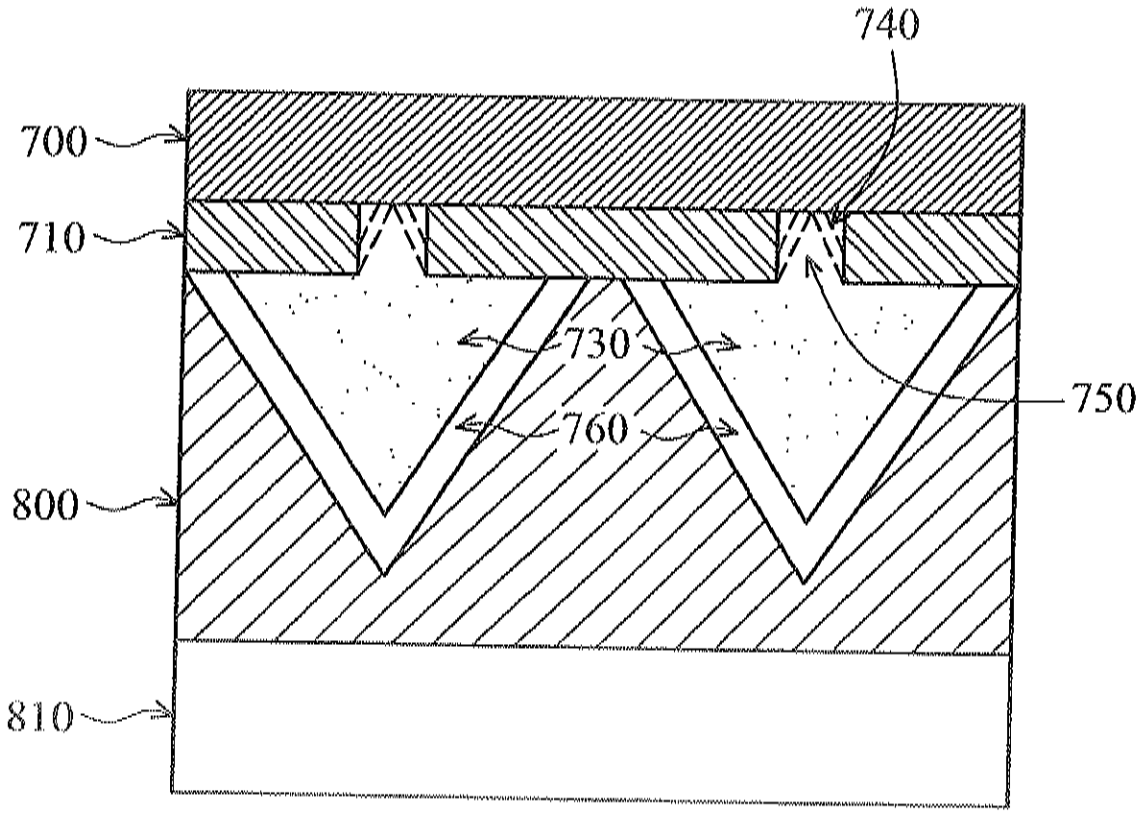


Figure 37

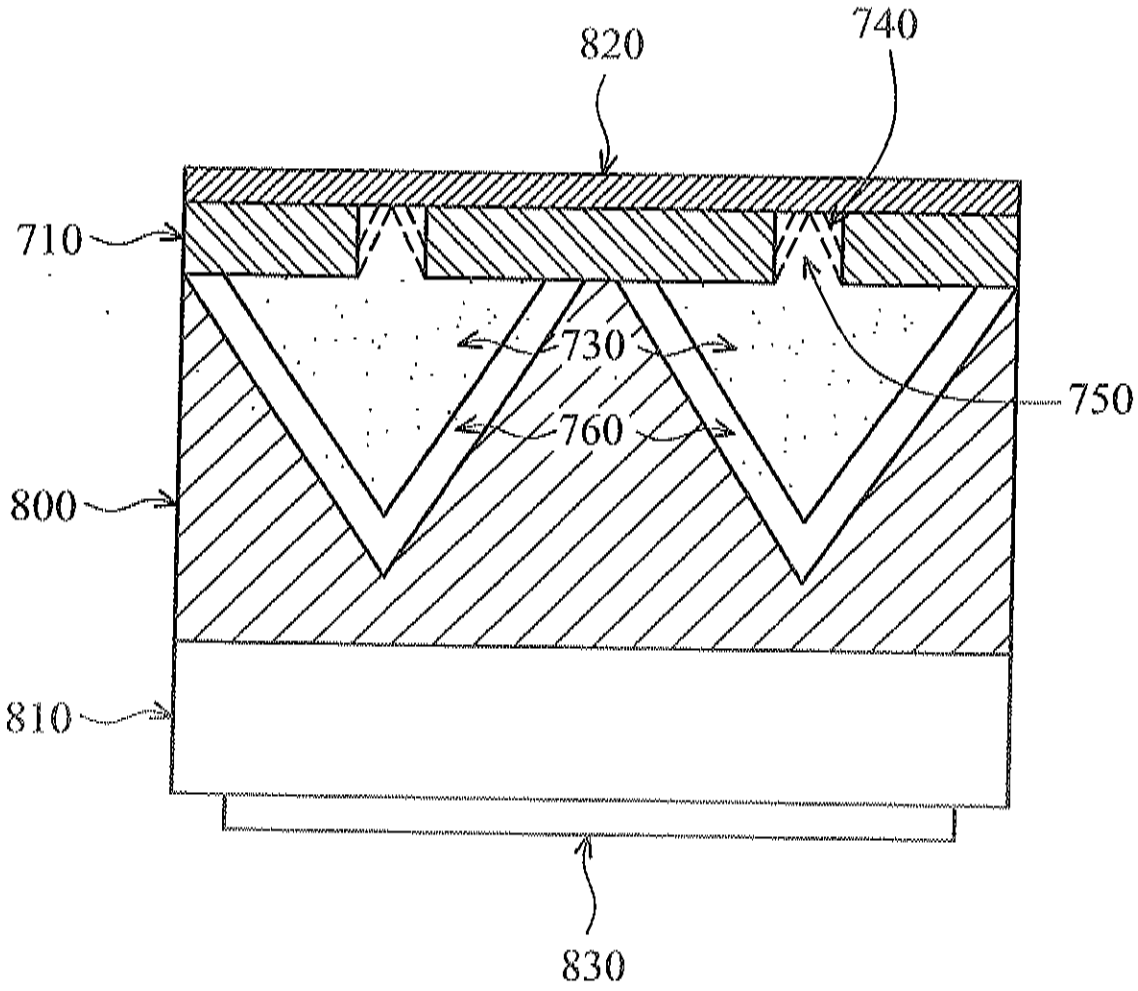


Figure 38

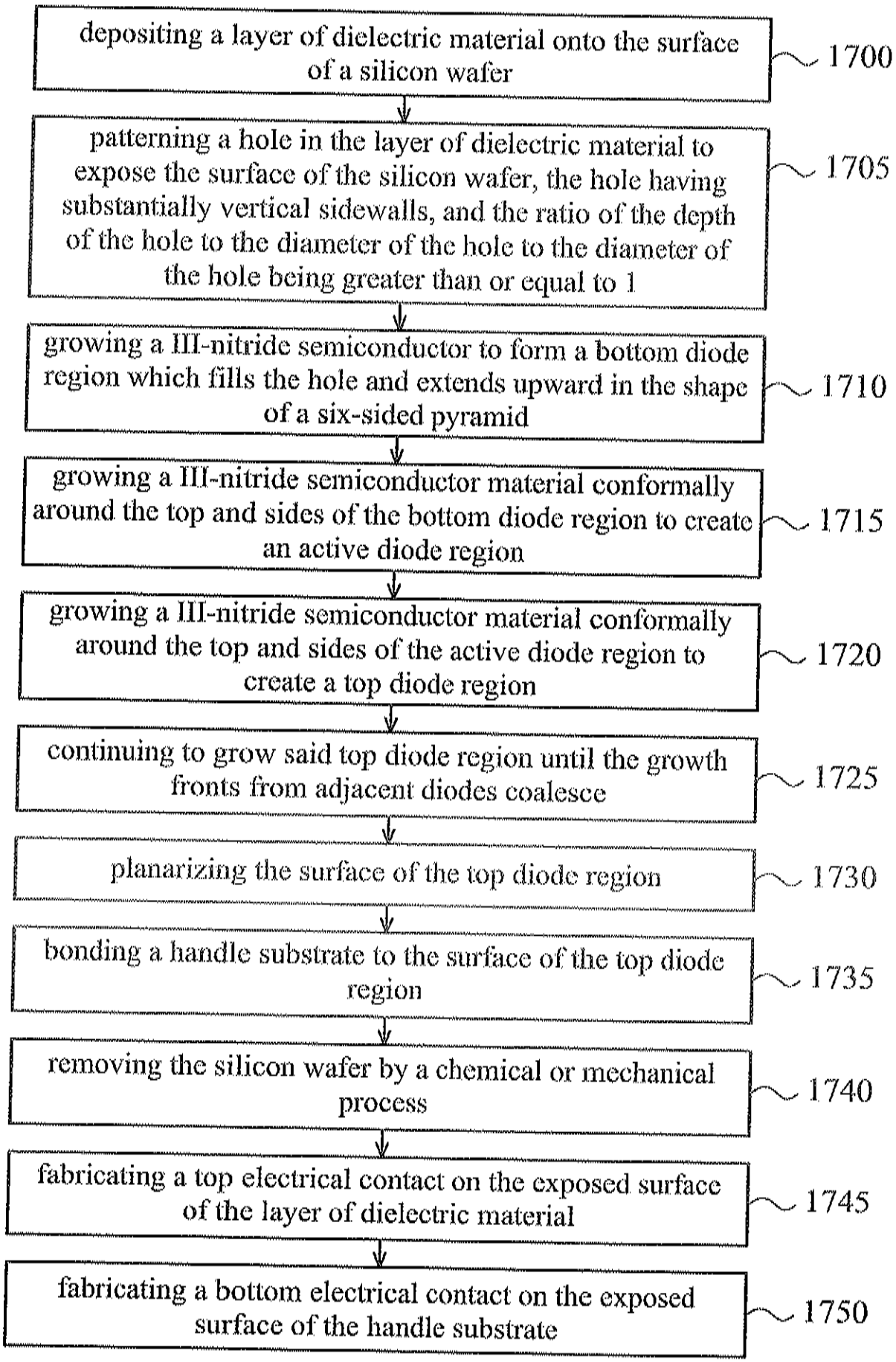

depositing a layer of dielectric material onto the surface of a silicon wafer
1700
patterning a hole in the layer of dielectric material to expose the surface of the silicon wafer, the hole having substantially vertical sidewalls, and the ratio of the depth of the hole to the diameter of the hole to the diameter of the hole being greater than or equal to 1
1705
growing a III-nitride semiconductor to form a bottom diode region which fills the hole and extends upward in the shape of a six-sided pyramid
1710
growing a III-nitride semiconductor material conformally around the top and sides of the bottom diode region to create an active diode region
1715
growing a III-nitride semiconductor material conformally around the top and sides of the active diode region to create a top diode region
1720
continuing to grow said top diode region until the growth fronts from adjacent diodes coalesce
1725
planarizing the surface of the top diode region
1730
bonding a handle substrate to the surface of the top diode region
1735
removing the silicon wafer by a chemical or mechanical process
1740
fabricating a top electrical contact on the exposed surface of the layer of dielectric material
1745
fabricating a bottom electrical contact on the exposed surface of the handle substrate
1750

Figure 39