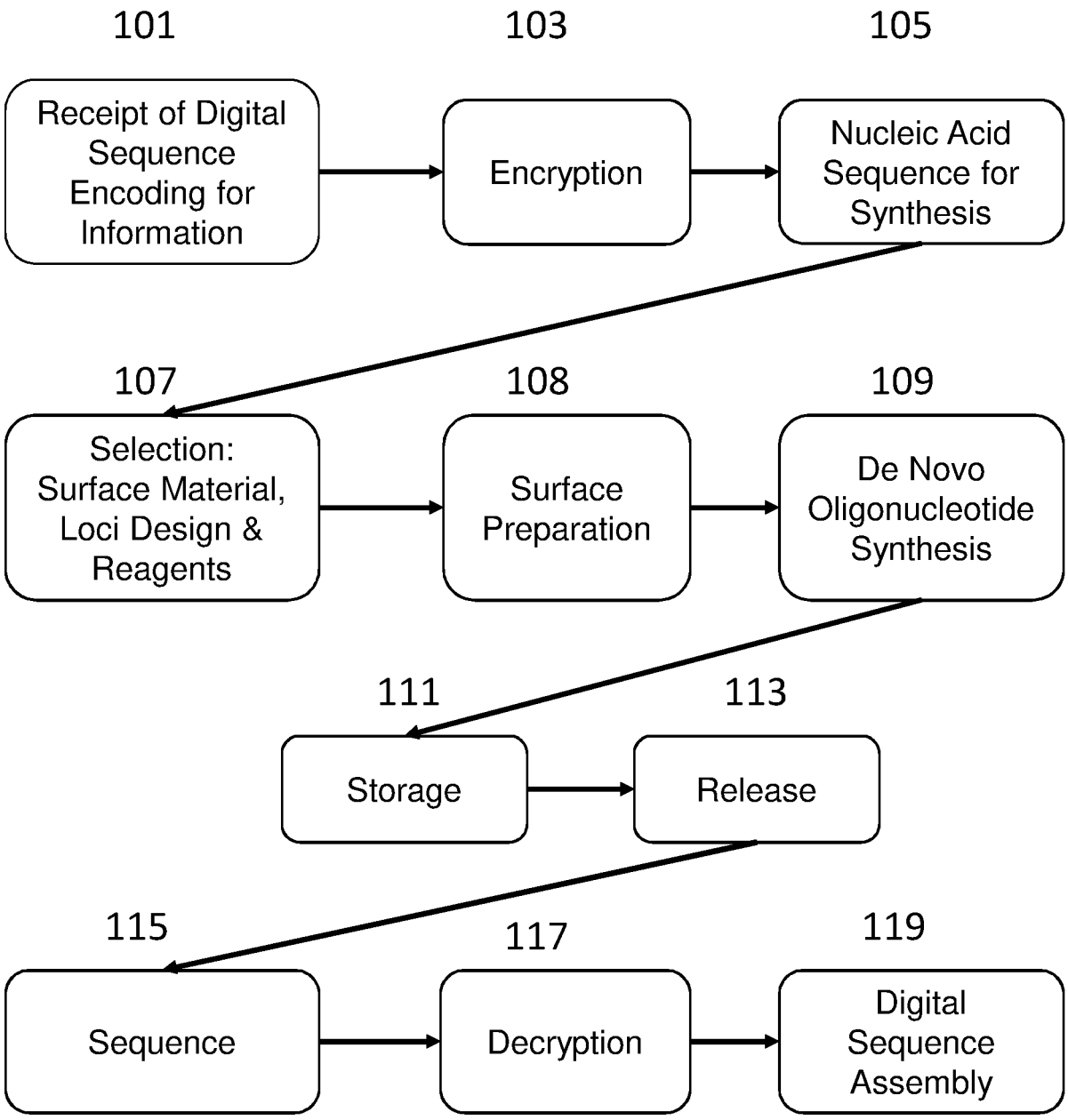

101
103
105
Receipt of Digital Sequence Encoding for Information
Encryption
Nucleic Acid Sequence for Synthesis
107
108
109
Selection: Surface Material, Loci Design & Reagents
Surface Preparation
De Novo Oligonucleotide Synthesis
111
113
Storage
Release
115
117
119
Sequence
Decryption
Digital Sequence Assembly

FIG. 1

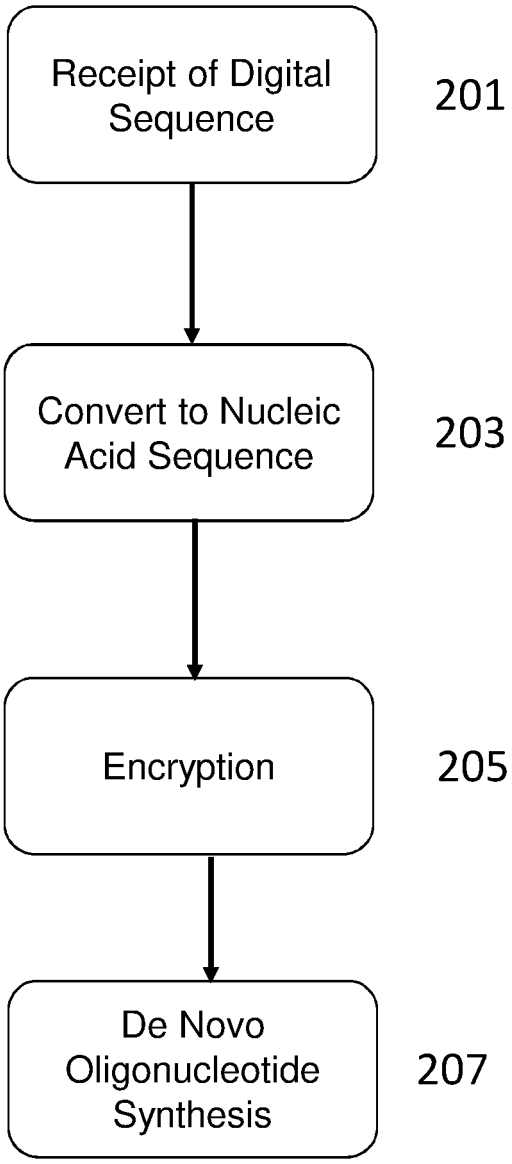

Receipt of Digital Sequence
201
Convert to Nucleic Acid Sequence
203
Encryption
205
De Novo Oligonucleotide Synthesis
207

FIG. 2

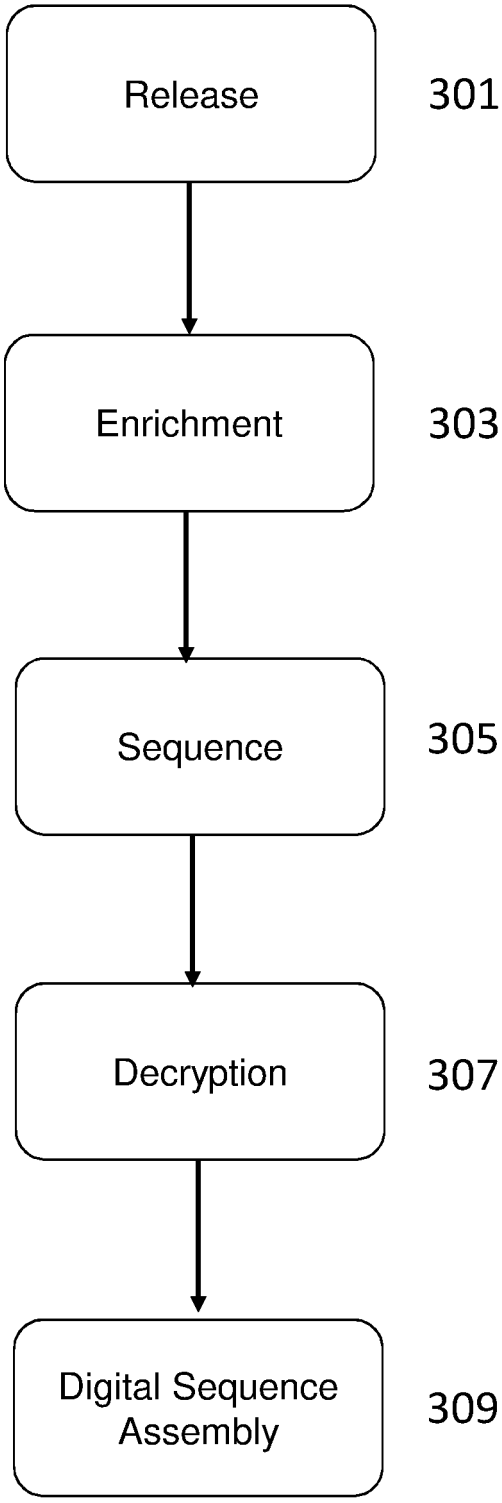

Release
301
Enrichment
303
Sequence
305
Decryption
307
Digital Sequence Assembly
309

FIG. 3

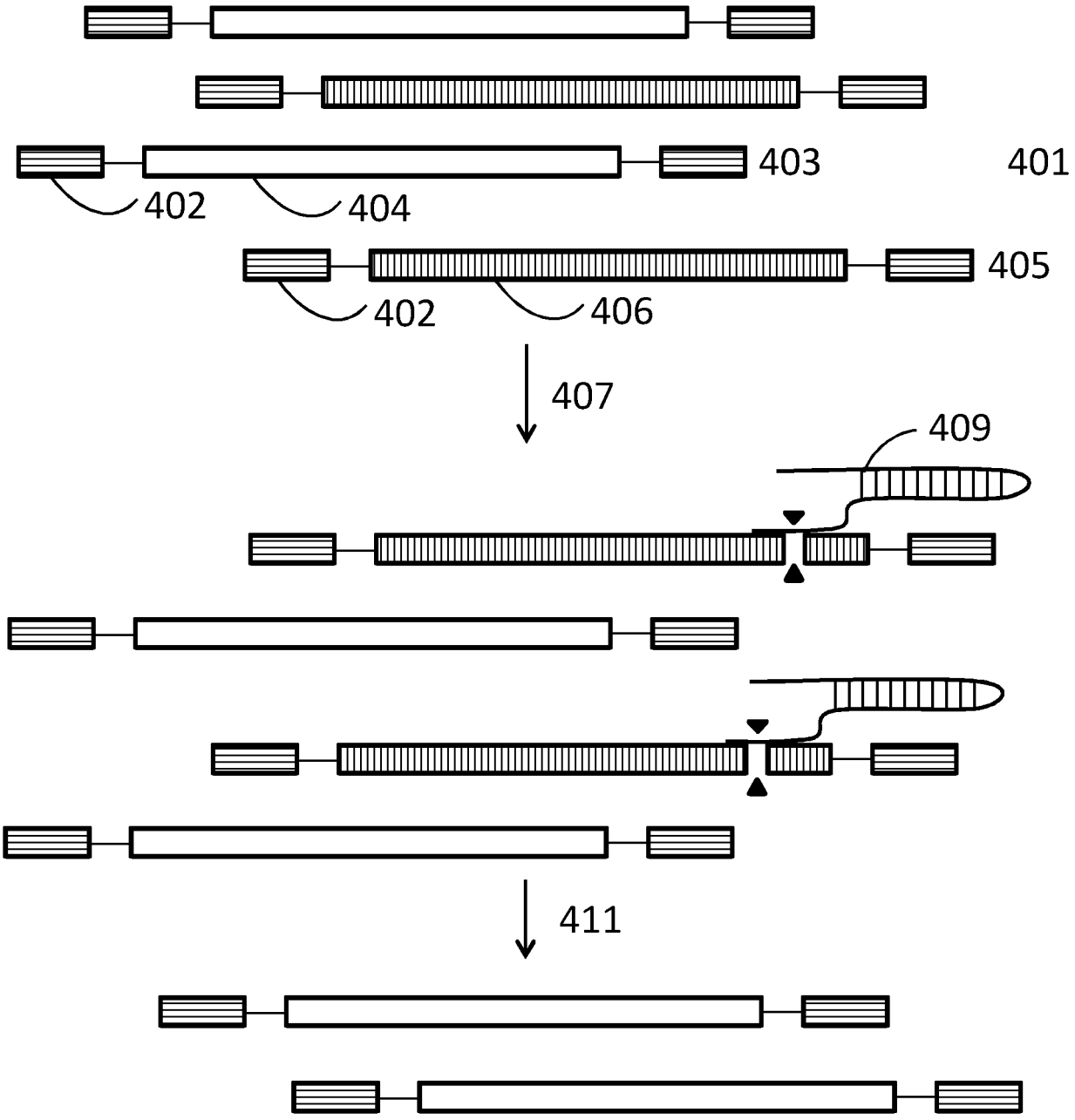


FIG. 4A

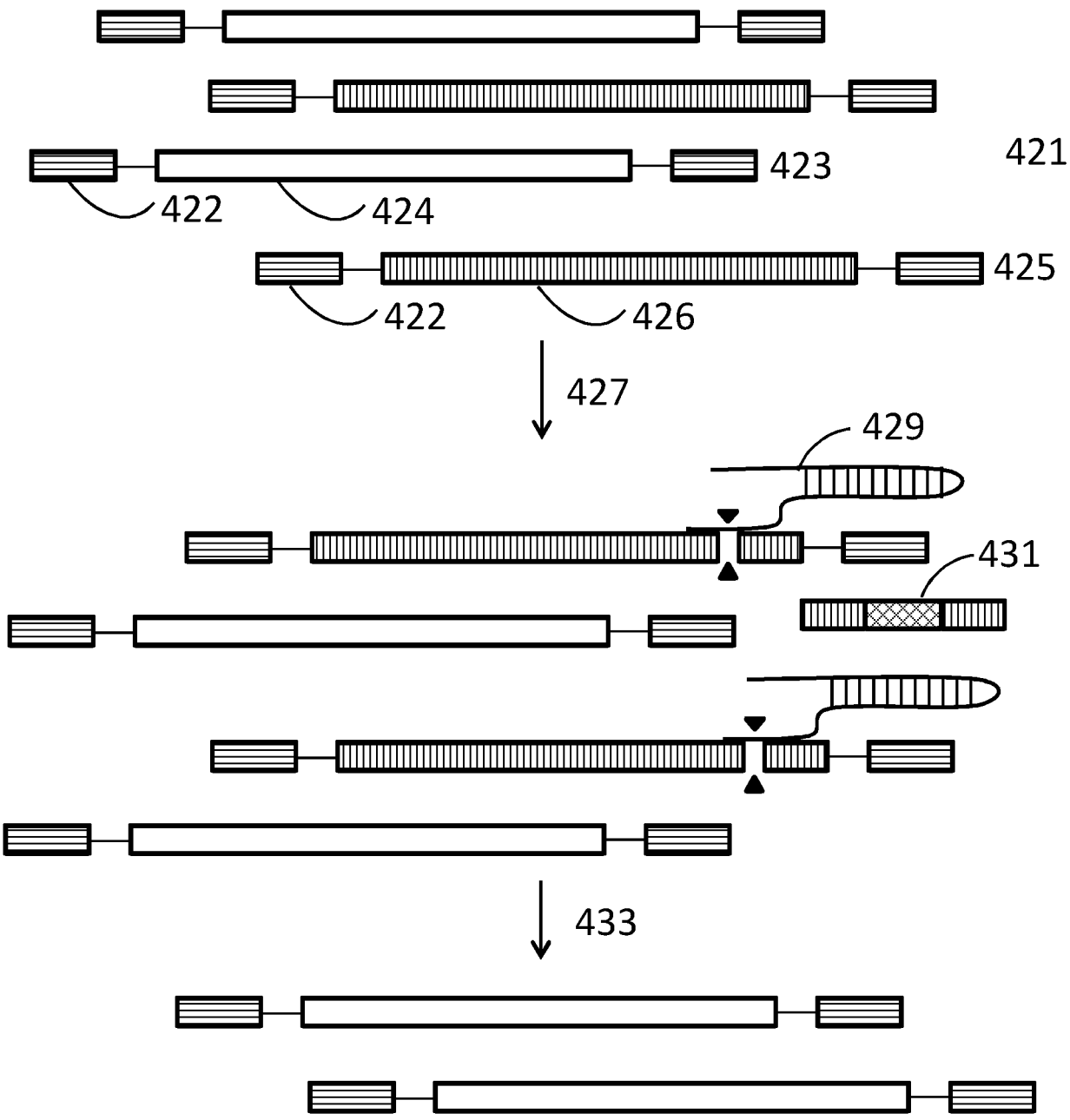


FIG. 4B

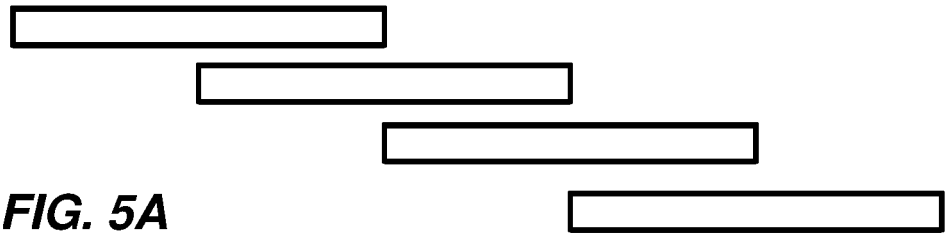


FIG. 5A



FIG. 5B

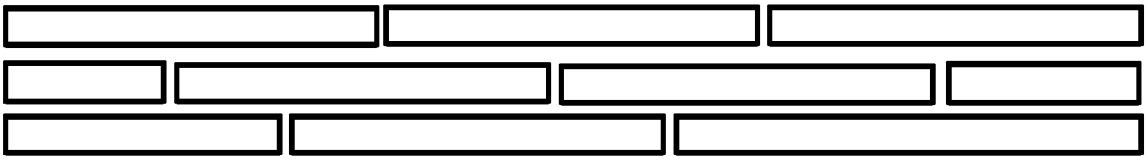


FIG. 5C

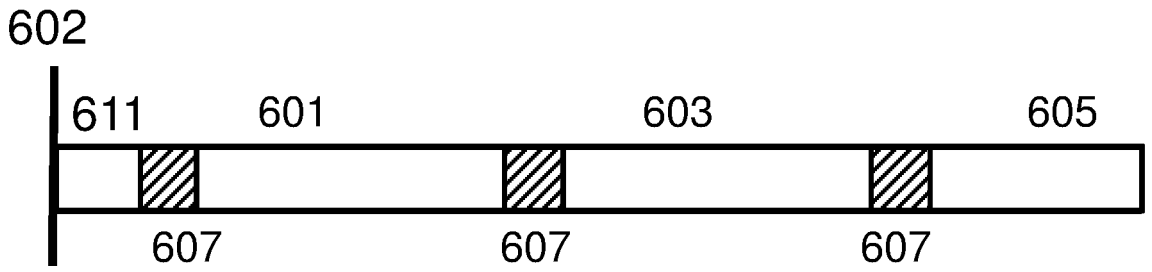


FIG. 6A

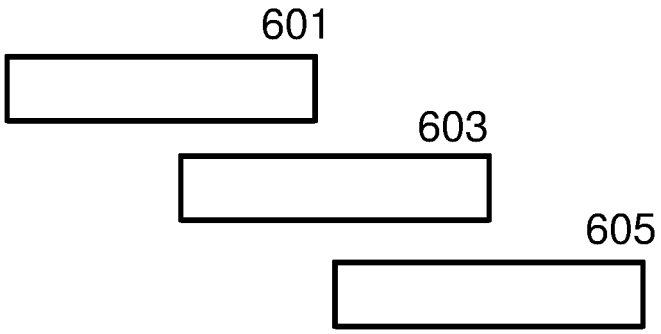


FIG. 6B

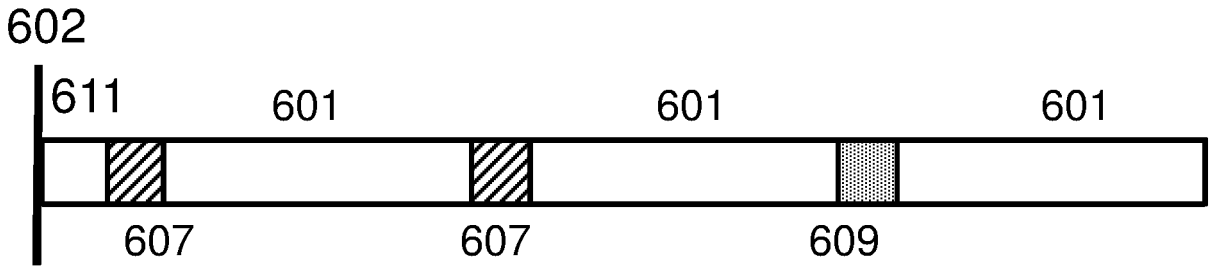


FIG. 6C

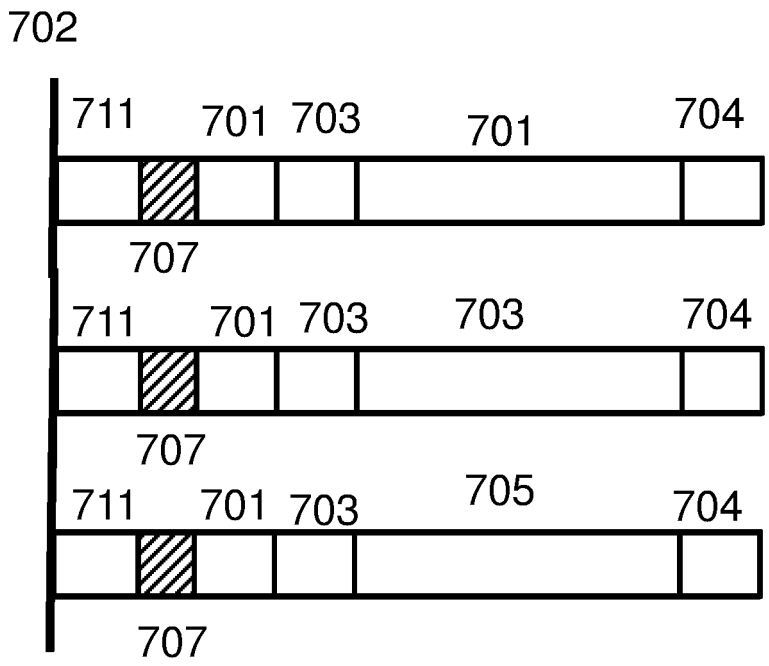

702
711
701
703
701
704
707
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701
703
703
704
707
711
701
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705
704
707

FIG. 7A

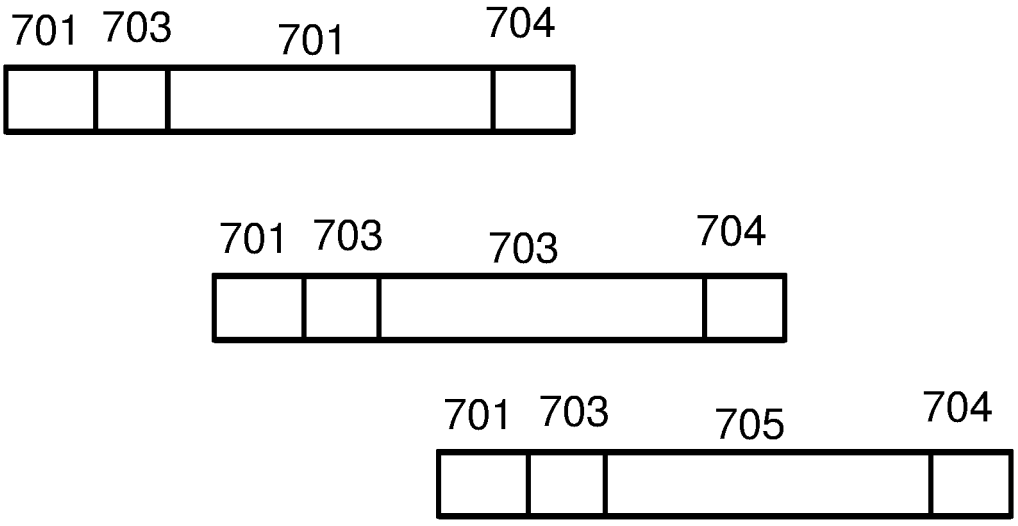

701
703
701
704
701
703
703
704
701
703
705
704

FIG. 7B

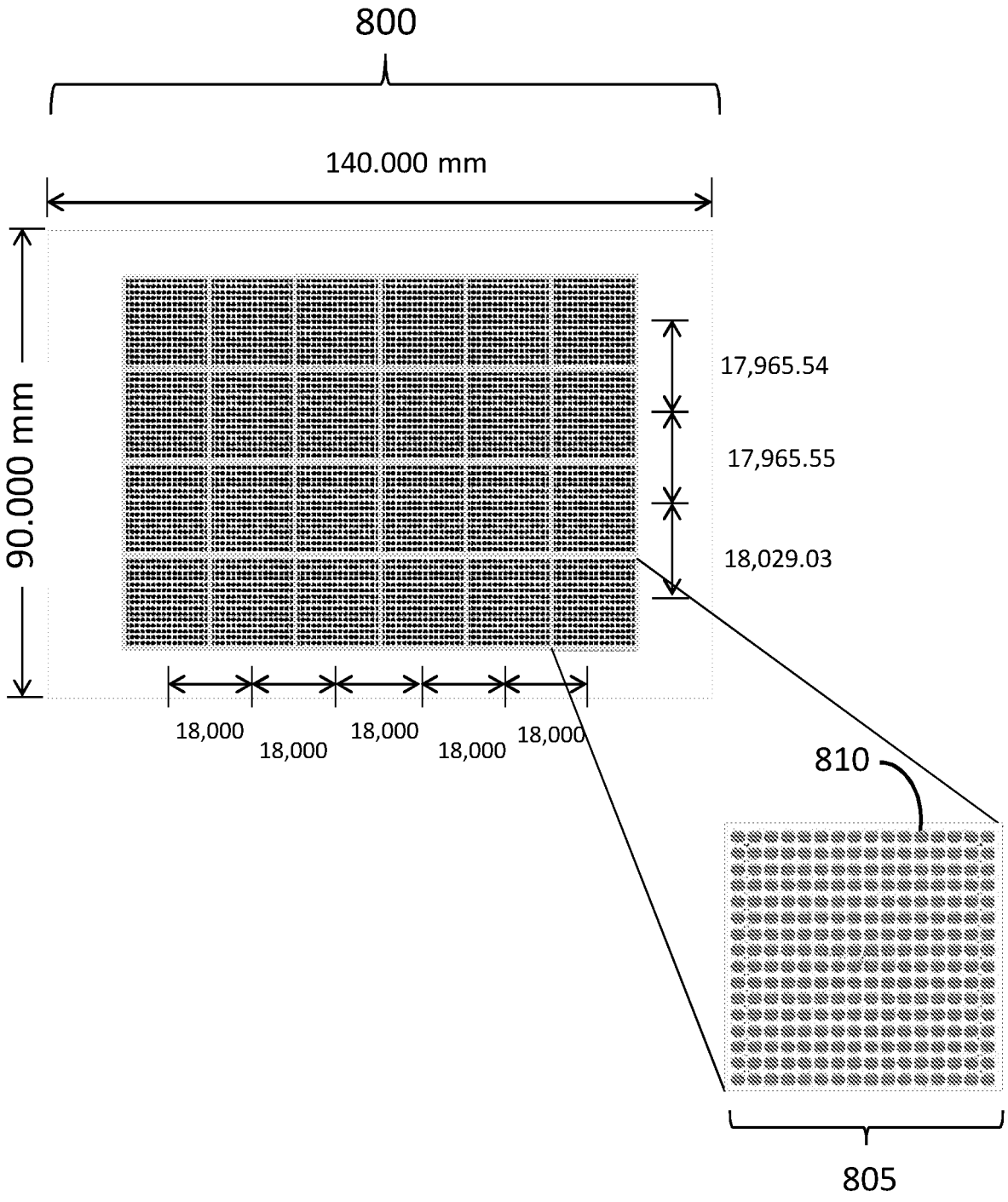

800
140.000 mm
90.000 mm
17,965.54
17,965.55
18,029.03
18,000
18,000
18,000
18,000
18,000
810
805

FIG. 8

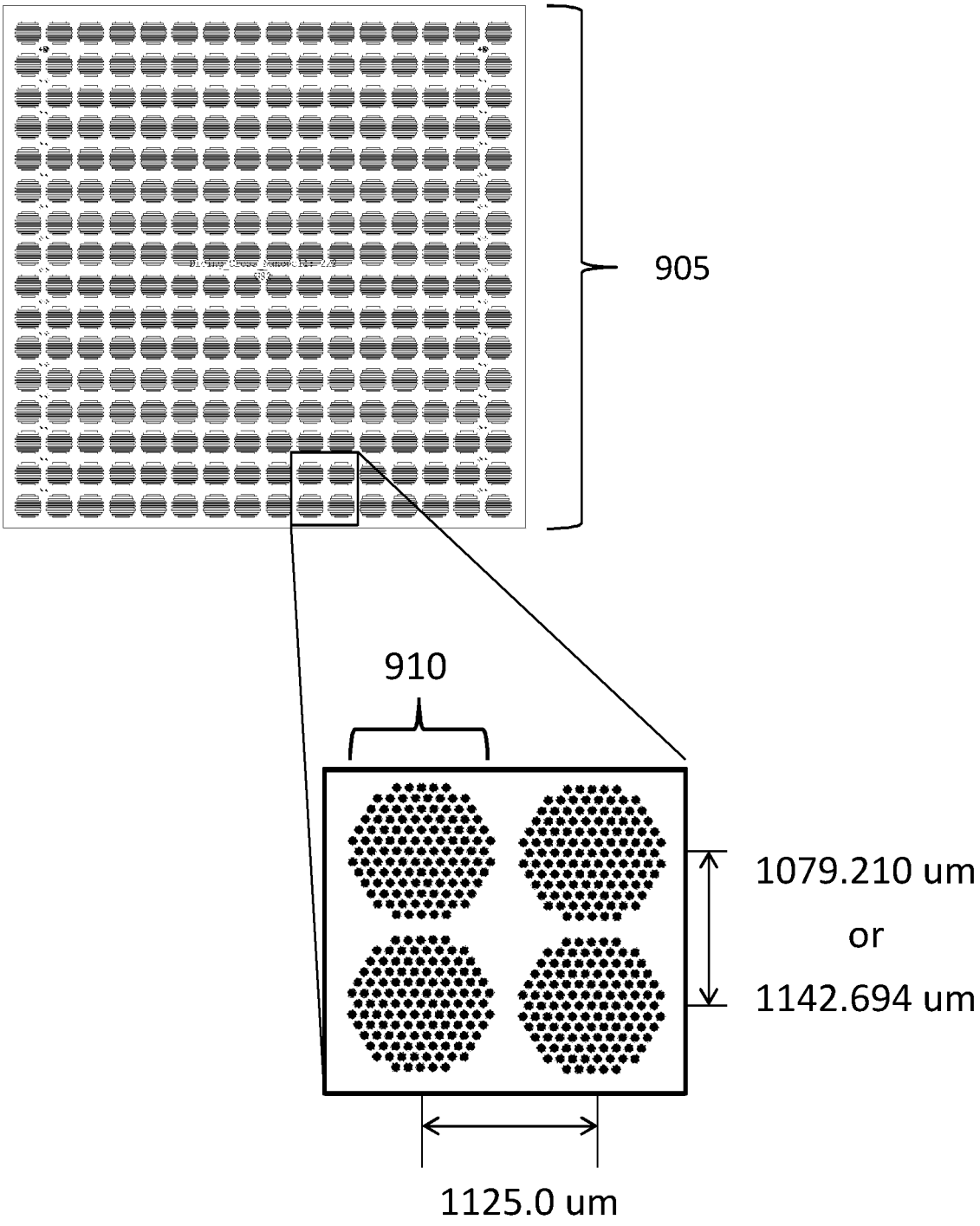


FIG. 9

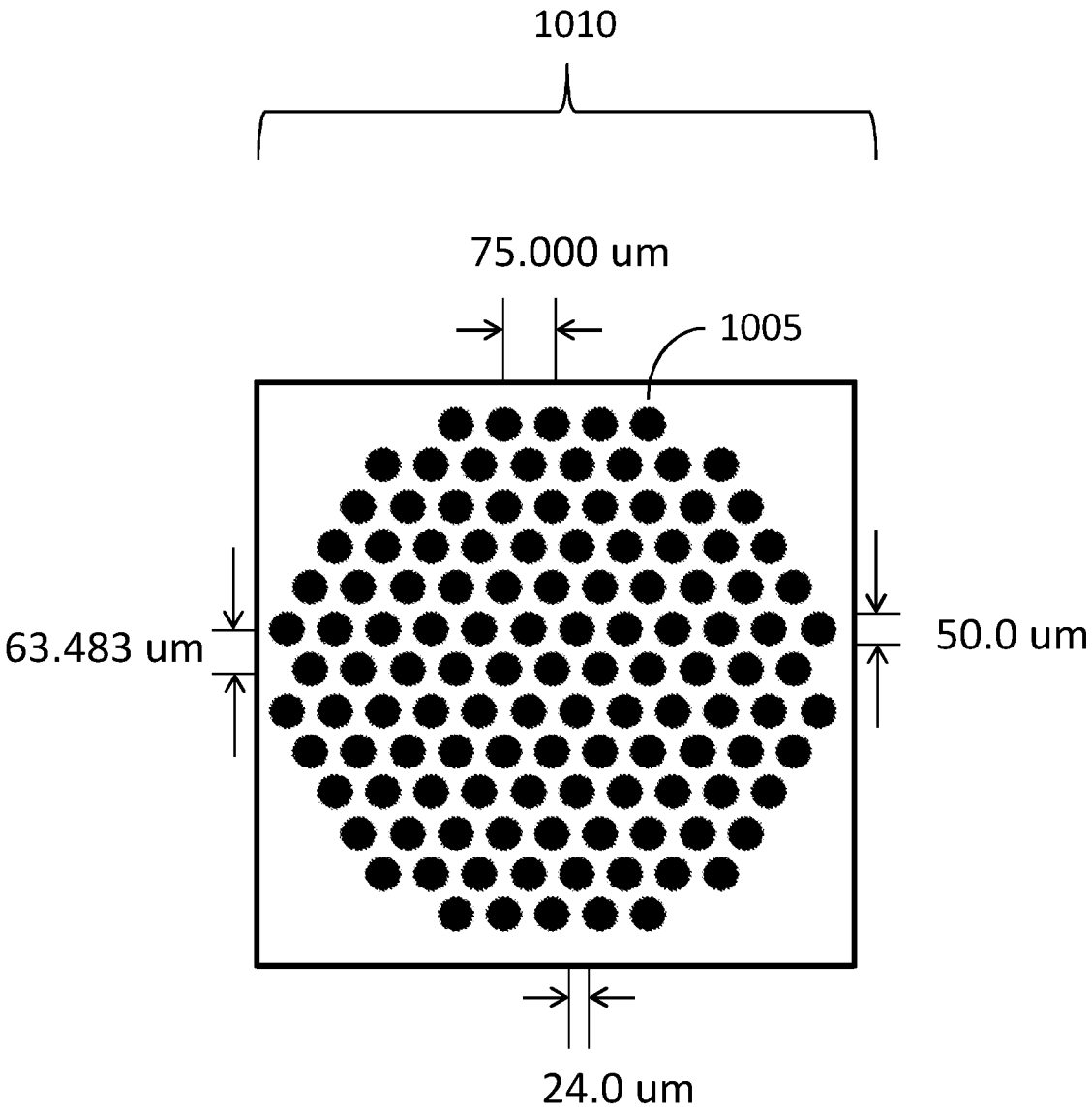


FIG. 10

FIG. 11A

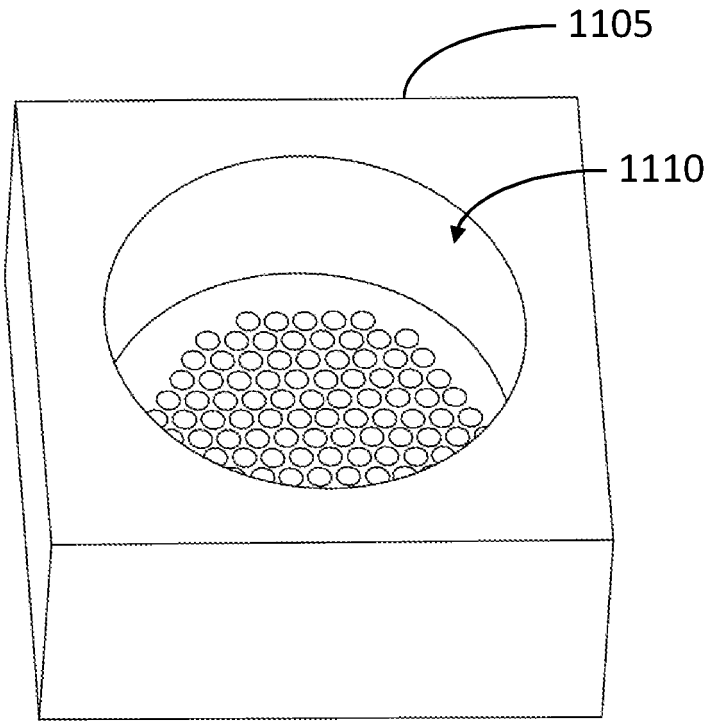
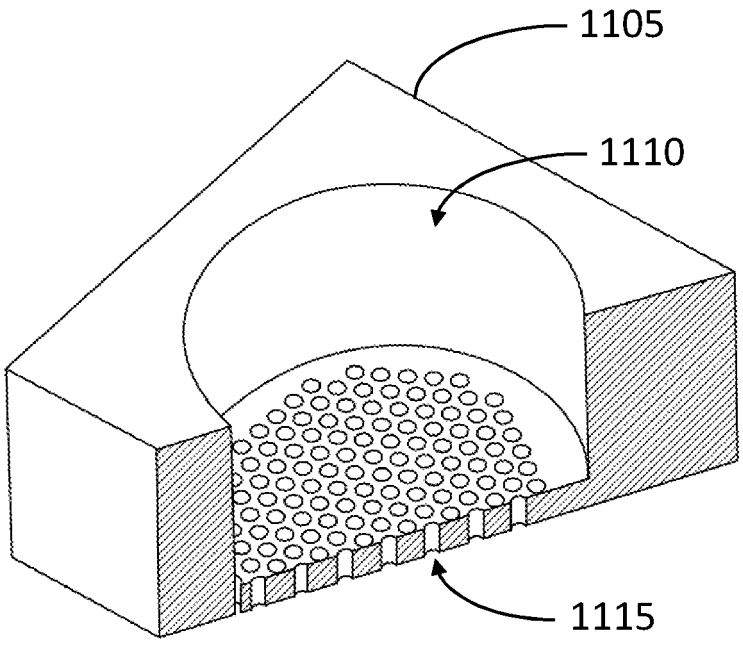


FIG. 11B



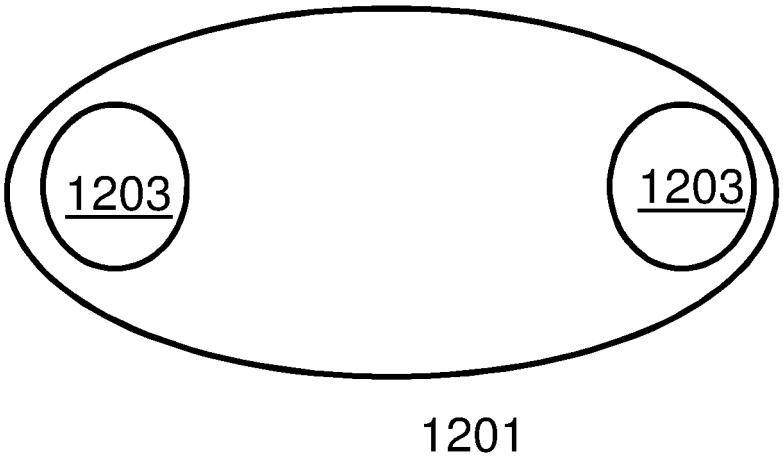


FIG. 12A

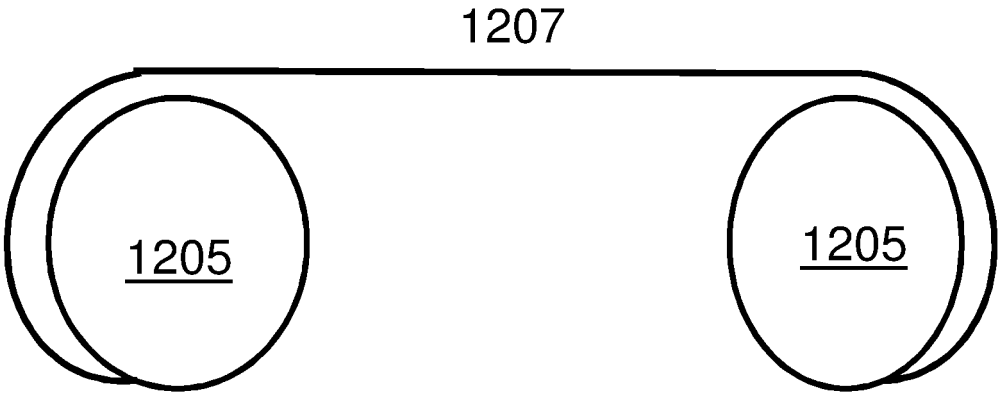


FIG. 12B

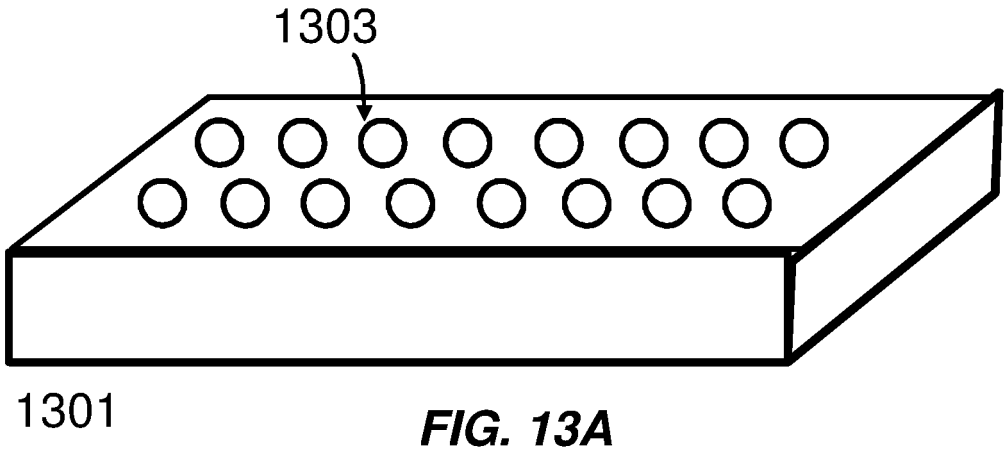


FIG. 13A

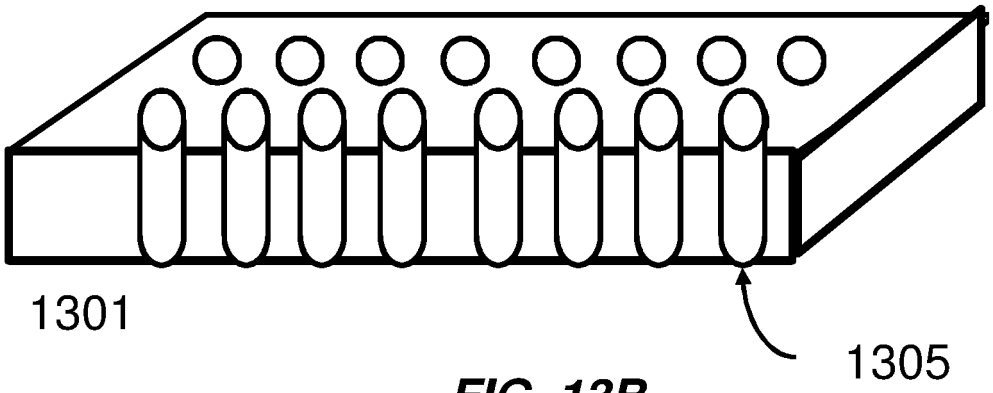


FIG. 13B

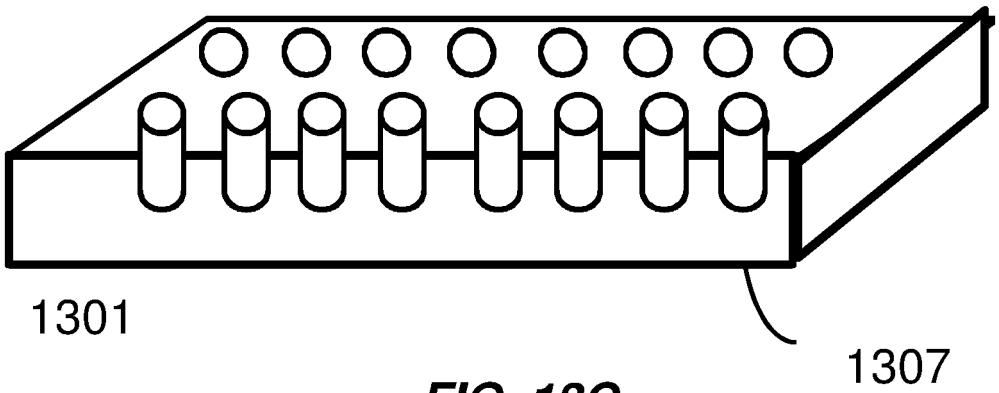


FIG. 13C

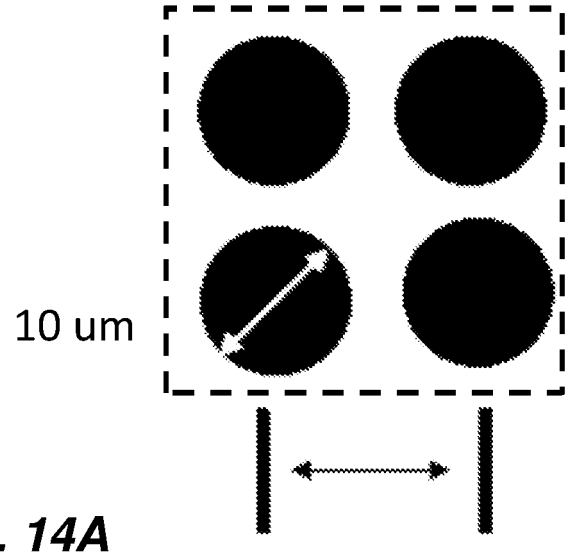


FIG. 14A

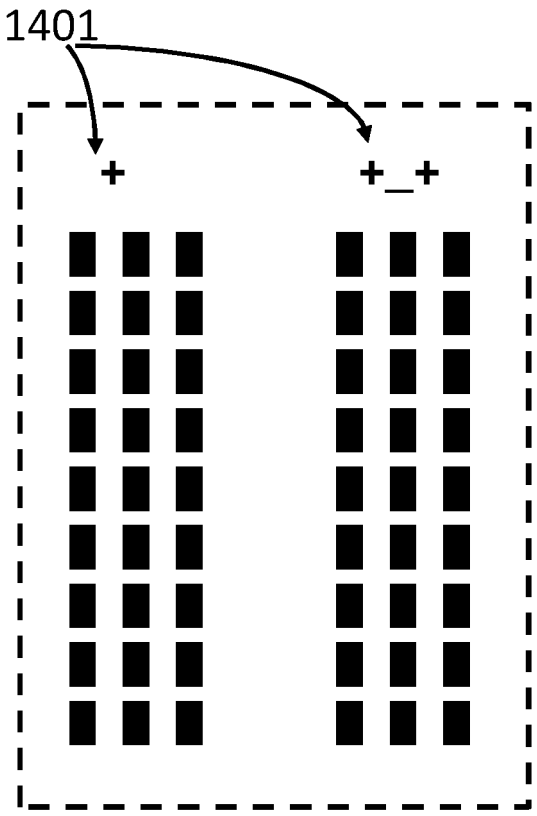


FIG. 14B

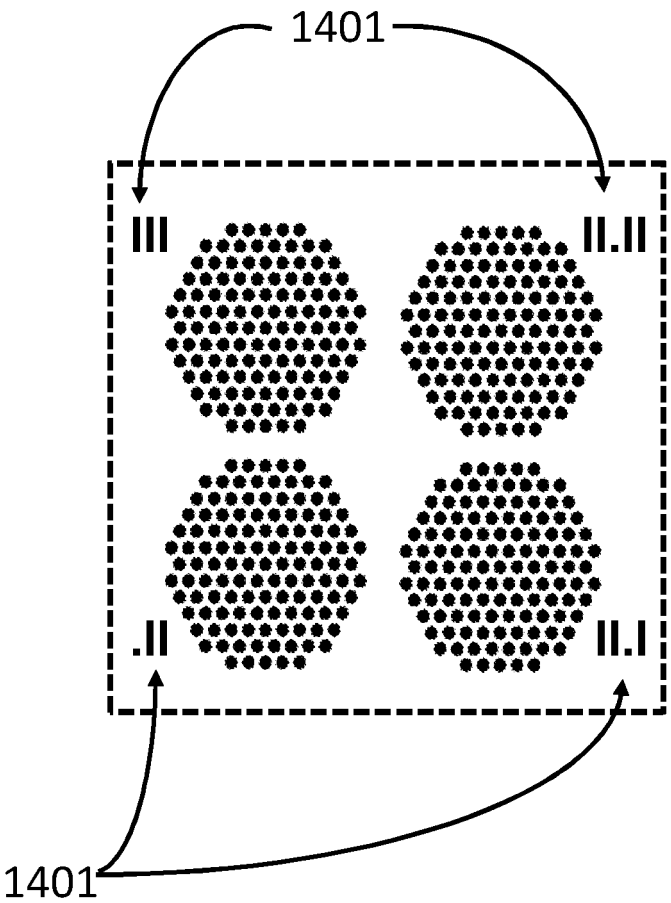


FIG. 14C

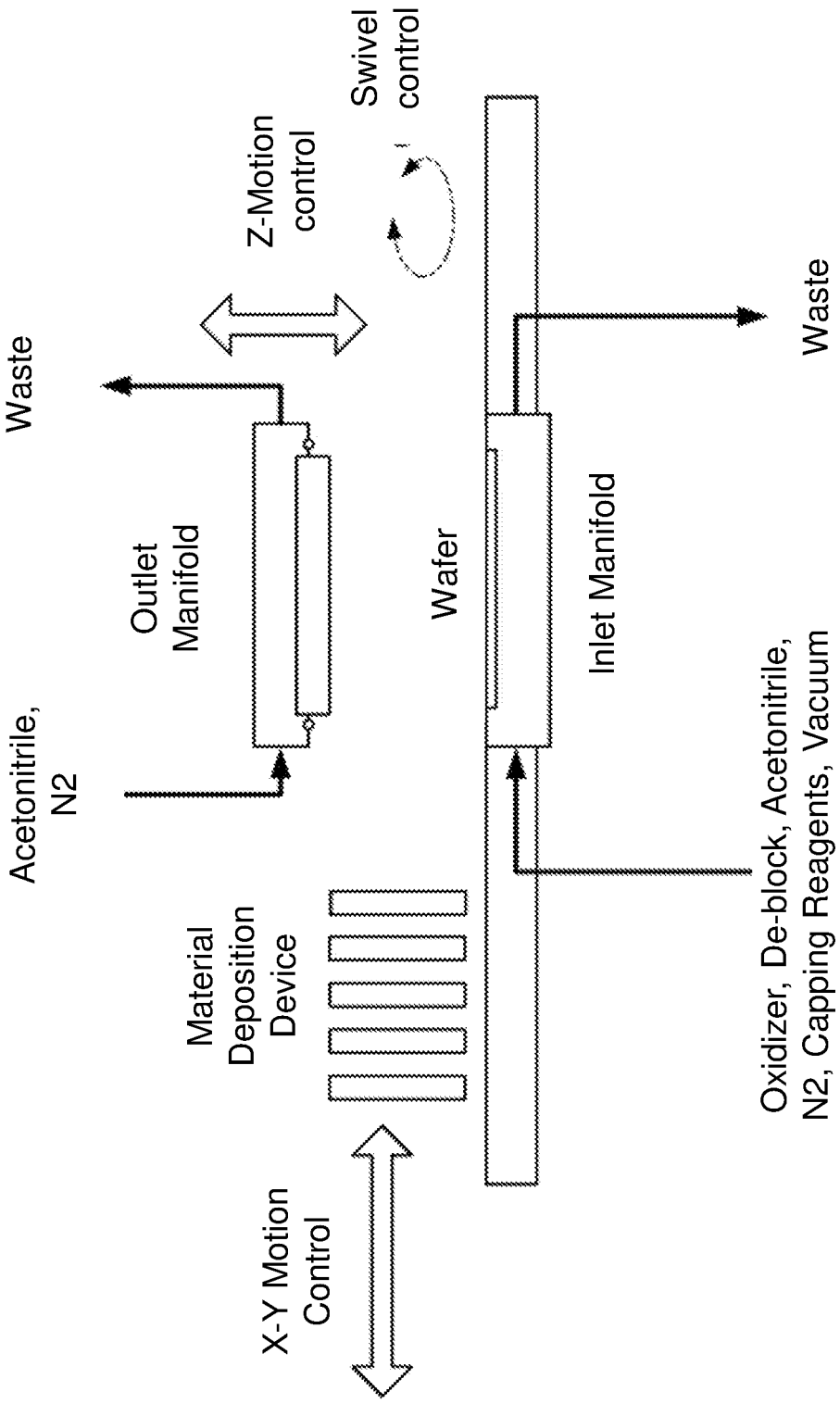

Swivel control
Z-Motion control
Waste
Outlet Manifold
Acetonitrile, N2
Material Deposition Device
X-Y Motion Control
Wafer
Inlet Manifold
Waste
Oxidizer, De-block, Acetonitrile, N2, Capping Reagents, Vacuum

FIG. 15

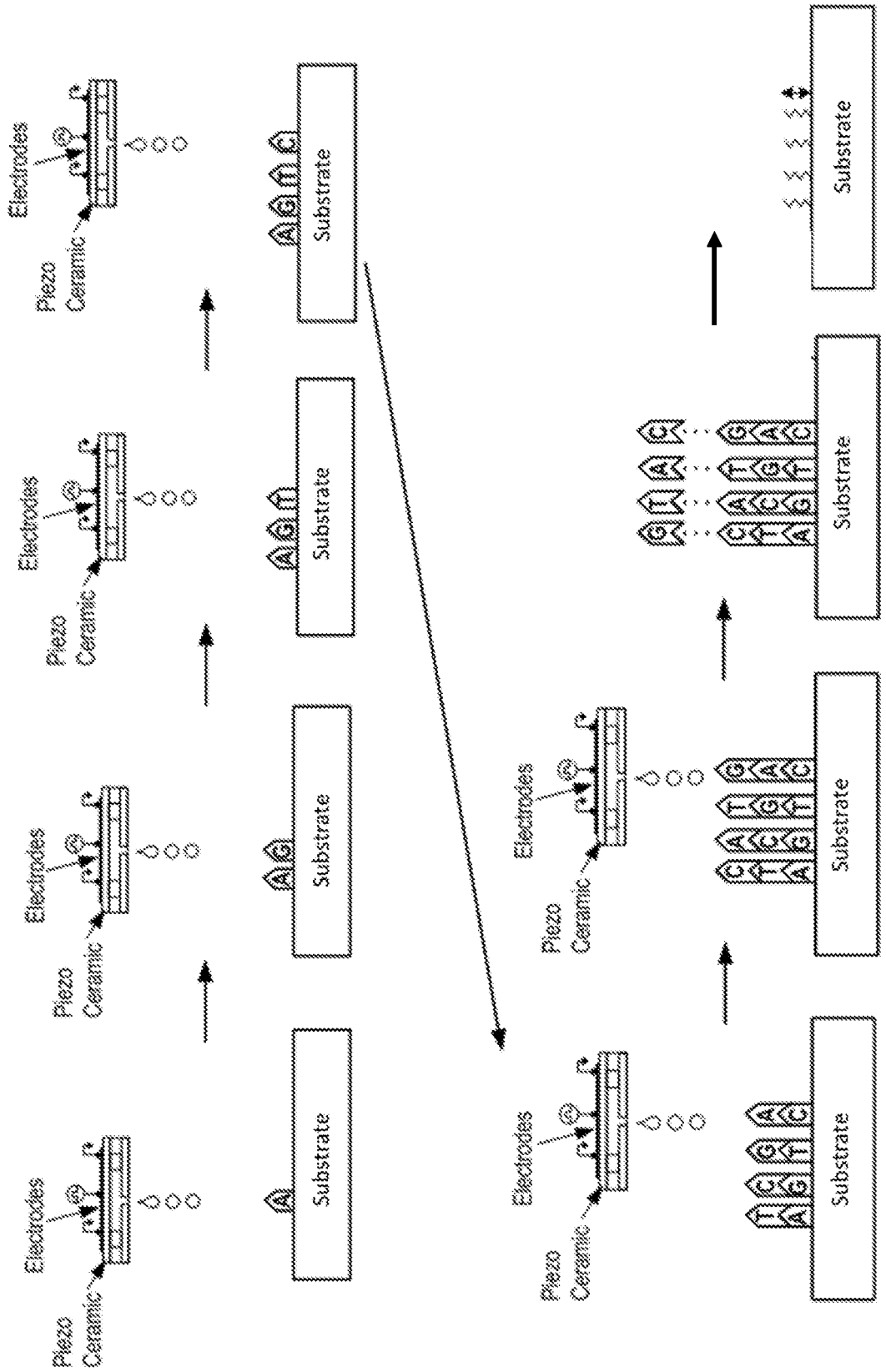


FIG. 16

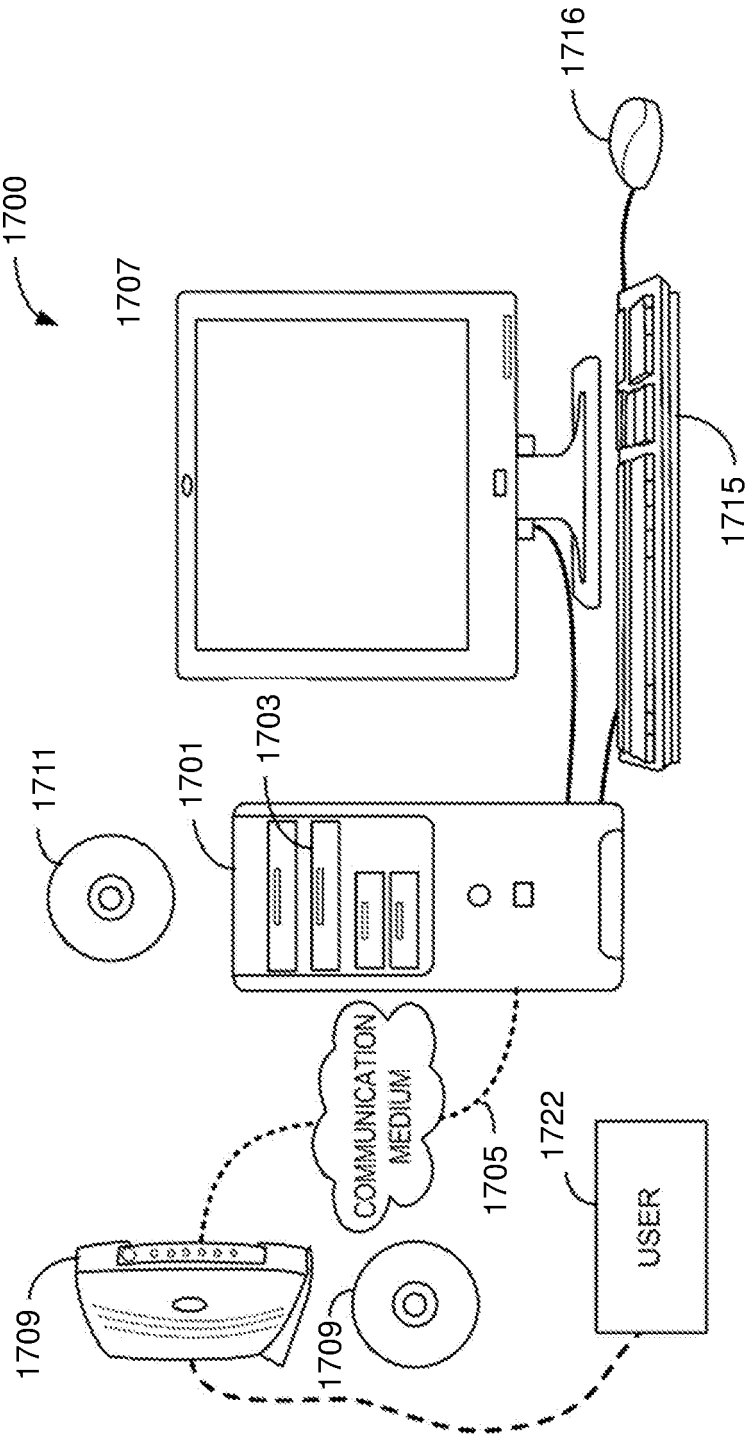

1700
1707
1716
1715
1703
1701
1711
COMMUNICATION MEDIUM
1705
1722
USER
1709
1709

FIG. 17

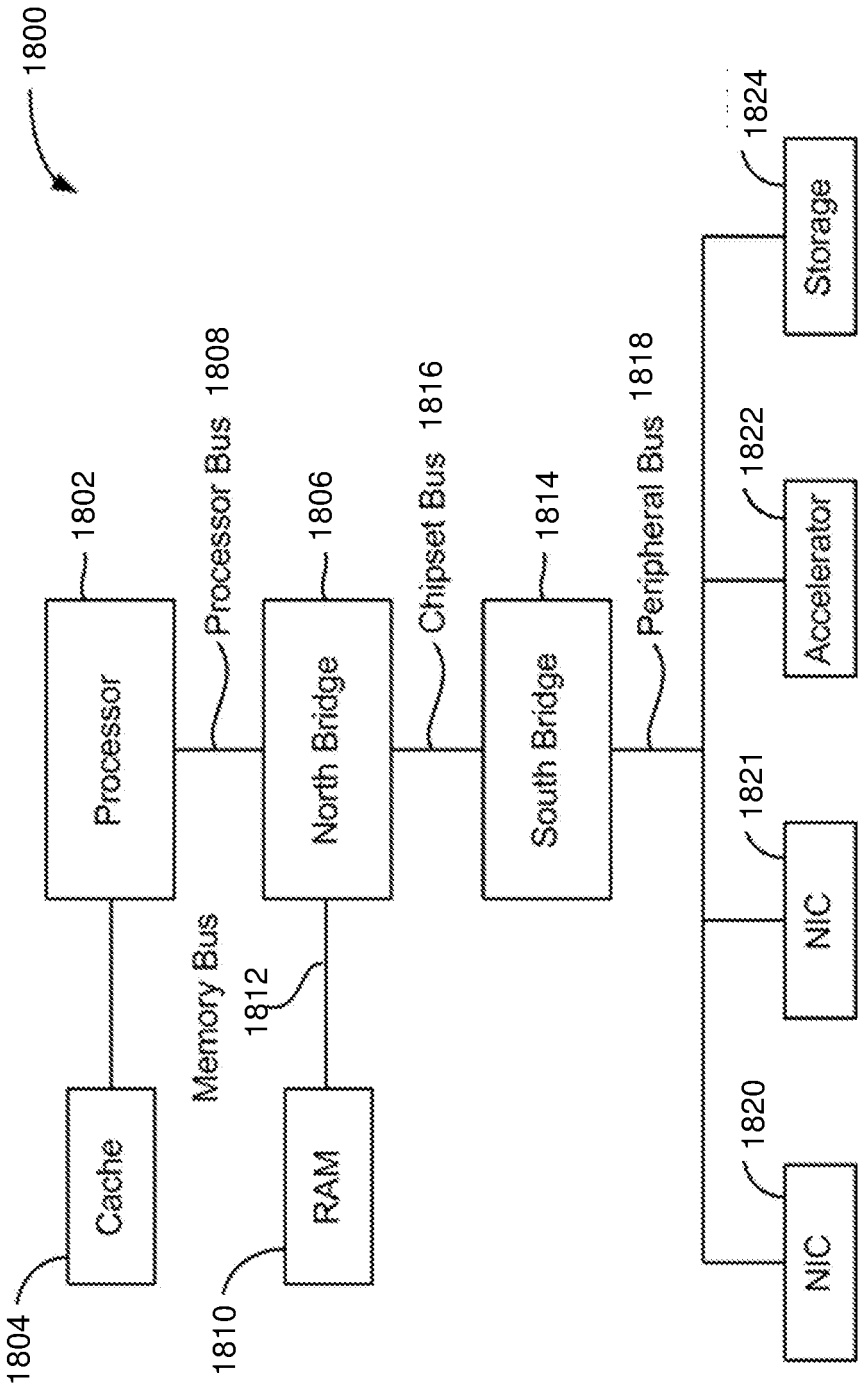

1800
Processor
1802
Processor Bus
1808
North Bridge
1806
Chipset Bus
1816
South Bridge
1814
Peripheral Bus
1818
Storage
1824
Accelerator
1822
NIC
1821
NIC
1820
Cache
1804
Memory Bus
1812
RAM
1810

FIG. 18

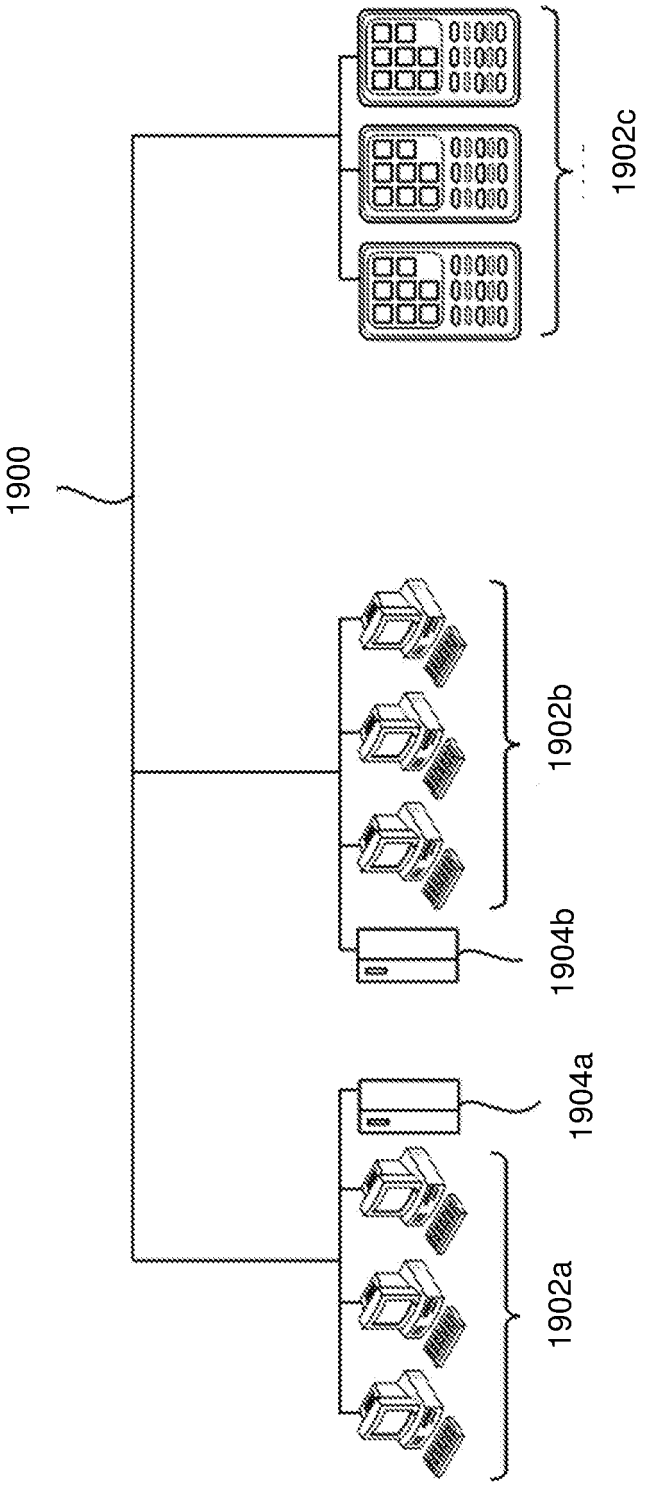


FIG. 19

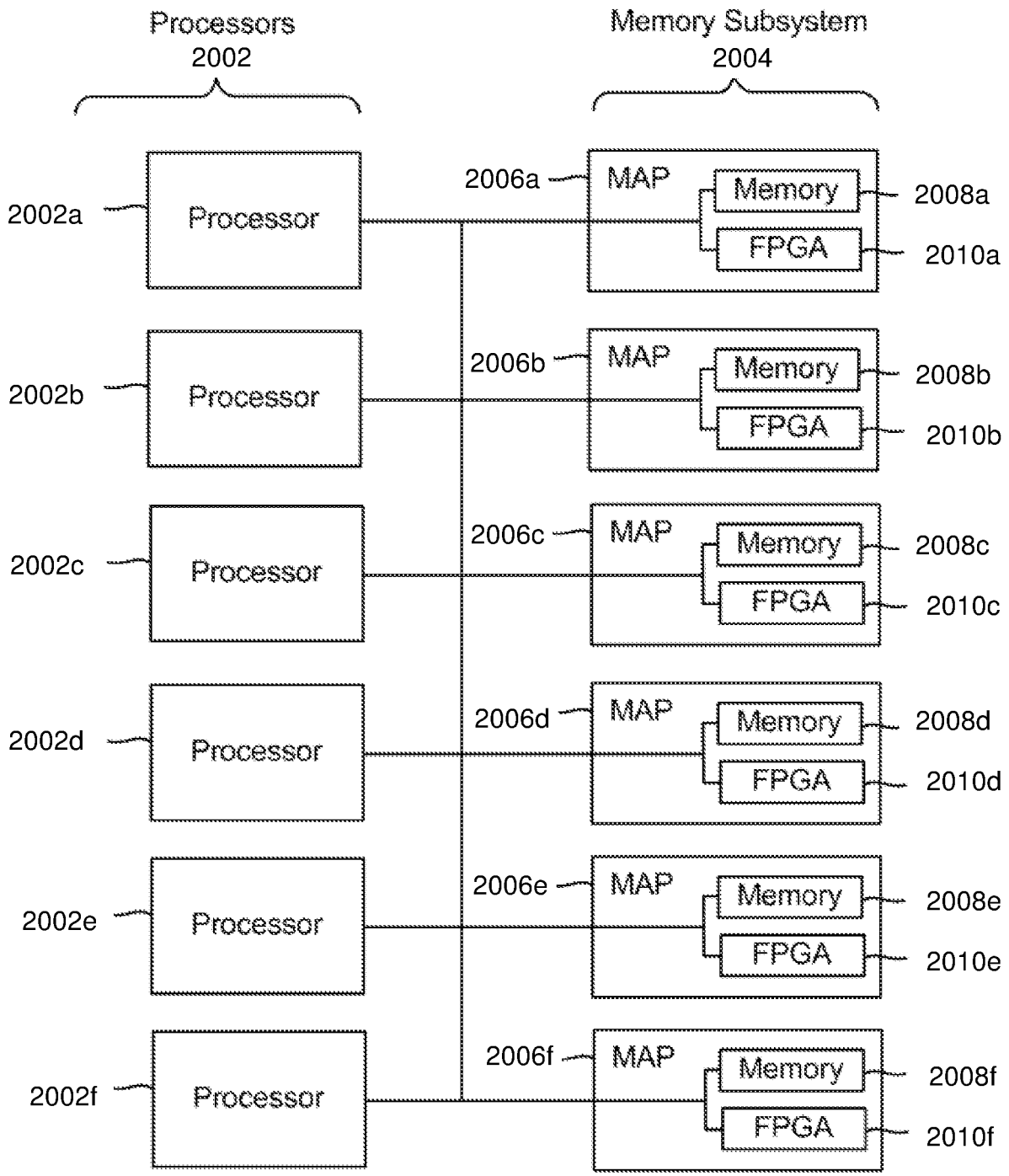

Processors
2002
Memory Subsystem
2004
2002a
Processor
2006a
MAP
Memory
FPGA
2008a
2010a
2002b
Processor
2006b
MAP
Memory
FPGA
2008b
2010b
2002c
Processor
2006c
MAP
Memory
FPGA
2008c
2010c
2002d
Processor
2006d
MAP
Memory
FPGA
2008d
2010d
2002e
Processor
2006e
MAP
Memory
FPGA
2008e
2010e
2002f
Processor
2006f
MAP
Memory
FPGA
2008f
2010f

FIG. 20