

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
4 March 2004 (04.03.2004)

PCT

(10) International Publication Number
WO 2004/019384 A3

(51) International Patent Classification⁷: **H01L 21/765**,
21/8238, 27/105, 27/108

(21) International Application Number:
PCT/US2003/026906

(22) International Filing Date: 25 August 2003 (25.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/229,336 26 August 2002 (26.08.2002) US

(71) Applicant: MICRON TECHNOLOGY, INC. [US/US];
8000 South Federal Way, Boise, ID 83716 (US).

(72) Inventor: LUAN, Tran, C.; 1125 W. Sandy, Ct., Meridian,
ID 83642 (US).

(74) Agents: TAYLOR, Jennifer, J. et al.; Wells St. John P.S.,
601 West First Ave, Spokane, WA 99201 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,

CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC,
SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA,
UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),
Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),
European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE,
ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO,
SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

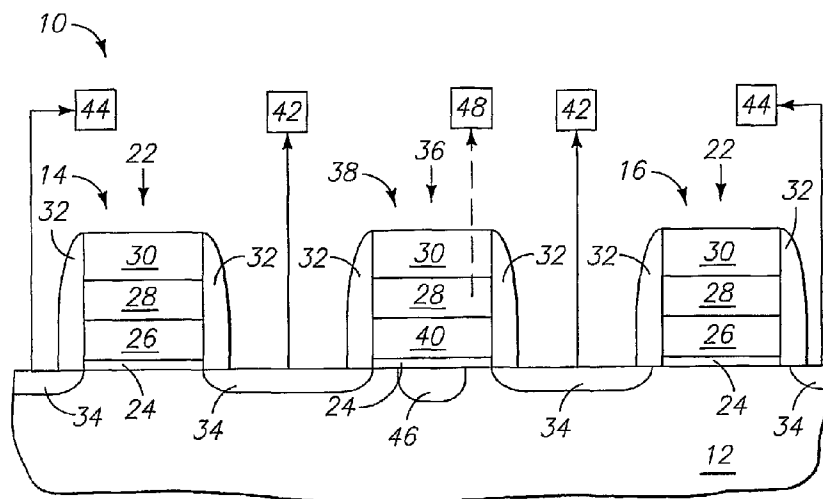
Published:
— with international search report
— with amended claims

(88) Date of publication of the international search report:
16 September 2004

Date of publication of the amended claims: 2 December 2004

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SEMICONDUCTOR CONSTRUCTIONS WITH GATED ISOLATION REGIONS HAVING INDIUM-DOPED SUB-REGIONS



(57) Abstract: The invention includes a semiconductor construction wherein gate structures are separated by isolation regions that are provided with an indium-doped pocket and a covering gate. The invention also includes a semiconductor construction having a pair of channel regions that have sub-regions doped with indium and surrounded by boron. A pair of transistor constructions are located over the channel regions and are separated by an isolation region. The transistors have gates that are wider than the underlying sub-regions. The invention also includes a semiconductor construction that has transistor constructions with insulative spacers along gate sidewalls. Each transistor construction is between a pair source/drain regions that extend beneath the spacers. A source/drain extension extends the source/drain region farther beneath the transistor constructions on only one side of each of the transistor constructions. The invention also includes methods of forming semiconductor constructions.