

PATENT SPECIFICATION

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DRAWINGS ATTACHED

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(54) DETECTOR WITH INACTIVATING CIRCUITRY

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a detector capable of inactivation in response to an electric control signal. A preferred embodiment is useful in automatically disabling a stereophonic FM receiver when it receives a non-stereophonic broadcast transmission, so that no changes are introduced into the quiescent bias of the detector output, and useful in color-killer arrangements in television receivers employing product detectors to demodulate chrominance signal.

Under the presently employed method of FM stereophonic broadcasting in the United States, a main carrier wave is frequency modulated by the sum of two audio frequency signals such as two stereophonically related left (L) and right (R) signals, the carrier wave being adapted for compatible reception by either monophonic or stereophonic receivers. The main carrier wave further is provided with stereophonic information in the form of a suppressed sub-carrier wave amplitude modulated with the difference of the two stereophonically related signals (L-R) and a pilot signal for use in demodulating the suppressed sub-carrier wave.

In the stereophonic receiver, a composite signal is produced at the output of the frequency modulation detector, the composite signal comprising the sum (L+R) signal component useable either by monophonic or stereophonic frequency modulation receivers, a 19 kHz (kilohertz) pilot signal and side bands of a suppressed 38 kHz sub-carrier representative of the difference (L-R) signal component. In order to reproduce the audio stereophonic program information, a 38 kHz signal is generated in the receiver in timed relation with the

19 kHz pilot signal to permit detection of the difference signal component and its subsequent combination (matrixing) with the sum signal component to reproduce the left and right separated audio signals. In order to prevent cross talk and consequent loss of separation between the signals, the regenerated 38 kHz signal must be accurately timed and, furthermore, relative signal gains of the sum and difference components must be accurately maintained.

Furthermore, when a frequency modulation station broadcasts monophonic program material and therefore does not transmit a 19 kHz pilot signal, it is desirable to automatically disable the 38 kHz generating circuits. When the broadcast program material does include stereophonic information, it is desirable to activate the stereophonic circuits automatically. This is done when the 19 kHz pilot signal exceeds a predetermined threshold level.

A product detector multiplying the composite signal by 38 kHz sine-wave or square-wave regenerated subcarrier is normally used for the detection of the difference signal component. A product detector constructed so as to have its output balanced against both its composite signal input and its subcarrier input is advantageous to use because it rejects all signals which are not contained in symmetrical AM sidebands with respect to the subcarrier input.

One such product detector which can be used advantageously in integrated circuits comprises first, second, third and fourth transistors and has first and second terminals for application of balanced signal input currents to be detected, third and fourth terminals for application of a switching carrier signal and fifth and sixth terminals from which balanced difference signal currents may be taken. The emitter electrodes of the first and second transistors are connected to the first terminal; the emitter electrodes of the third and fourth transistors are connected to the second terminal. The base electrodes of the first and third transistors are connected to the third terminal;

[Price 25p]

Price 75p

the base electrodes of the second and fourth transistors are connected to the fourth terminal. The collector electrodes of the first and fourth transistors are connected to the fifth terminal; and the collector electrodes of the second and third transistors are connected to the sixth terminal. The first and second terminals are each supplied a quiescent bias current larger than the peak swings of the signal to be detected. A usual practice is to apply large sine-wave or square-wave signals at switching carrier frequency between said third and fourth terminals which cause equal duty cycle switching of currents between the first and second transistors and between the third and fourth transistors.

The type of product detector described above is used in other applications such as the demodulation of chrominance signals in television receivers. Controllable disabling of such a chrominance signal demodulator by the techniques of the present invention is a good way of performing the color-killer function in television receivers using such chrominance signal detectors. The chrominance signal detectors would in such instance be disabled during the reception of black and white broadcasts or during color broadcasts in which the picture content is too much disturbed by noise for satisfactory viewing in color.

The present invention is a detector capable of inactivation in response to an electric control signal. The present invention comprises a detection apparatus, connection means for connecting outputs of the detection apparatus to a source of energizing potential and means for disabling the detection apparatus. The detection apparatus, of which the product detector described supra is an example, has a first and second input, each input exhibiting unidirectionally conductive characteristics, and a first and a second output. The first and second outputs of the detector apparatus are connected to a source of energizing potential by connection means. This may be done with a resistor connecting each detection apparatus output to the source of energizing potential, permitting push-pull detected signals to be obtained at the outputs of the detection apparatus in response to its inputs being provided with push-pull signal currents to be detected and quiescent bias currents. Another example of the manner in which the detection apparatus may be connected to a source of energizing potential is by connection means consisting of a direct connection of one of the detector outputs to the source and the connection of the other output as it was in the previous example. This connection of the detection apparatus provides a single-ended detected signal output in response to the inputs of the detection apparatus being provided push-pull signal currents to be detected and quiescent bias currents. In any case, the quiescent current flow out of the first and second detection apparatus outputs is equal to one-

half the sum of the quiescent bias currents applied to the first and second detection apparatus inputs. The means of disabling the detection apparatus comprises switching means responsive to the electric control signal to direct current conductively couple each of the first and second detection apparatus inputs to each of its outputs through paths of similar conductivity. This direct current conductive coupling causes the application of push-pull input signal currents and their accompanying quiescent bias currents to flow through the paths of similar conductivity rather than through the detection apparatus. The detector will exhibit no difference in the quiescent current flowing through the connection means whether activated or inactivated.

The present invention will be more fully explained in the following description of the drawing in which means are shown in block and schematic form for detecting an audio difference signal ($L-R$) component of a composite stereophonic signal and for combining such component with an audio sum signal ($L+R$) component so as to produce stereophonically related left and right channel audio signals. The illustrated difference signal detector and combining (matrix amplifier) means, features of which form the subject of copending application No. 60160/70, Serial No. 1,332,513, are particularly adapted for fabrication using integrated circuit techniques.

An FM radio tuner-detector 10 which processes FM broadcast signals to provide composite stereophonic signals is coupled via a terminal T_1 of an integrated circuit chip 11 to a composite signal amplifier 12. The composite stereophonic signals comprise an audio frequency sum signal ($L+R$) in the case of reception of monophonic broadcast material or, in the case of reception of stereophonic broadcast material, the composite stereophonic signal comprises an audio sum signal ($L+R$) component, a pilot (19 kHz component) and a suppressed subcarrier amplitude modulated by a difference signal ($L-R$) component. In either case, FM background (SCA) music components also may be coupled to terminal T_1 .

Composite signal amplifier 12 is arranged to amplify, in a linear manner, signals in the range of approximately 10 Hz to 150 kHz so as to produce first and second amplifier composite signal voltages, which are substantially identical to each other but 180° out of phase with each other (i.e., push-pull), for direct application to circuit elements within integrated circuit chip 11.

A specific configuration for amplifier 12, as well as for other circuit elements shown in block diagram form on chip 11, is described in United Kingdom Patent Application No. 60162/70 (Serial No. 1,332,515).

The push-pull composite signal voltages, along with suitable substantially equal biasing

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voltages, are direct coupled from amplifier 12 to the base electrodes of common emitter amplifier transistors 14 and 15, the emitter electrodes of which are individually coupled to ground through resistors 16 and 17, respectively.

The collector electrodes of transistors 14 and 15 supply push-pull composite signal currents with substantially equal bias currents to each of the product detector input terminals 1, 2. The product detector used for difference signal detection is indicated generally by the reference numeral 13 and has first and second terminals 1, 2 for application of push-pull composite signal currents, third and fourth terminals 3, 4 for application of 38 kHz sub-carrier swings and fifth and sixth terminals 5, 6 from which detected difference signal currents may be taken.

The first terminal 1 of the product detector is directly connected to joined emitter electrodes of a first pair of switching transistors 18, 19 and its second terminal 2 is directly connected to joined emitter electrodes of a second pair of switching transistors 20, 21. The base electrodes of both transistors 18 and 20 are directly connected to the third terminal 3 of the product detector, which is shown connected in turn to one of a pair of 38 kHz square wave outputs of a synchronized 38 kHz push-pull signal source 42. The base electrodes of transistors 19 and 21 are directly connected to the fourth terminal 4 of the product detector, which is shown connected in turn to the other of the 38 kHz square wave outputs.

Square wave signal source 42 is synchronized with respect to the 19 kHz pilot component of the composite signals provided by amplifier 12 in any of the many known techniques employed in FM multiplex stereophonic decoder systems. One particularly advantageous synchronizing system is set forth in the above-identified United Kingdom Patent Application 60162/70 (Serial No. 1,332,515).

A source of operating voltage (B+) is coupled to the fifth terminal 5 of the product detector by means of an output resistor 22 and to the sixth terminal 6 of the product detector by means of an output resistor 23 substantially equal to resistor 22. Also connected to terminal 5 are the collector electrodes of transistors 18 and 21. Connected to terminal 6 are the collector electrodes of transistors 19 and 20.

Push-pull output currents including the demodulated difference signal components, (L-R) and -(L-R), are provided at the fifth and sixth terminals 5, 6 of the product detector and push-pull voltages proportionate to these currents are developed across resistors 22 and 23, respectively. These push-pull voltages are coupled, respectively, to emitter follower output transistors 24 and 25 serving as voltage sources to produce the desired push-pull difference signal components across respective matrix resistors 26 and 27.

The sum (L+R) signal information is also developed across resistors 26 and 27 by means of respective transistors 28 and 29, the collector electrodes of which are coupled to resistors 26 and 27 remote from transistors 26 and 25. The base electrodes of transistors 28 and 29 both are coupled to one of the push-pull outputs of composite signal amplifier 12. The emitter electrodes of transistors 28 and 29 are returned to ground by means of individual resistors 30 and 31, respectively.

Transistors 25 and 29 comprise a first matrix amplifier arrangement, the output of which (e.g., R) is coupled via a terminal T₁₁ of chip 11 and a de-emphasis network 32 to audio reproducing means such as an amplifier and loudspeaker (not shown). Transistors 24 and 28 comprise a second matrix amplifier arrangement, the output of which (e.g., L) is coupled via a terminal T₁₀ of chip 11 and a de-emphasis network 33 to audio reproducing means such as a second amplifier and loudspeaker (not shown).

In order to maintain the impedance at the emitters of follower transistors 24 and 25 substantially constant as conduction (and therefore the impedances) of transistors 28 and 29 vary with applied composite signals, a composite signal of opposite phase with respect to that of the signal applied to transistors 28 and 29 is applied from amplifier 12 to the base of electrodes of compensating transistors 34 and 35. The collector electrodes of transistors 34 and 35 are directly connected, respectively, to the emitter electrodes of followers 24 and 25. The emitter electrodes of transistors 34 and 35 are returned to ground by separate resistors 36 and 37.

As the output signals produced by composite signal amplifier 12 vary, conduction of transistors 28 and 34 vary equally and oppositely (push-pull input signals). Therefore, the sum of the collector currents of transistors 28 and 34 (which load transistor 24) remains substantially constant. Similarly, variations in the output of composite signal amplifier 12 do not produce variations in the load on transistor 25 since the sum of the collector currents of transistors 29 and 35 remains substantially constant as the output of composite signal amplifier 12 varies. Accurate matrixing of the sum and difference signal components is therefore not comprised by variations in loading on voltage source transistors 24 and 25 as the composite signal varies.

In the operation of the difference signal detector 13 described above, the complementary 38 kHz square wave outputs of signal source 42 are provided in predetermined time relationship with respect to the received 19 kHz pilot signal component (and therefore with respect to the suppressed 38 kHz subcarrier) to provide synchronous detection of the difference signal components (L-R) of the amplitude modulated suppressed subcarrier com-

ponent coupled from amplifier 12 to transistors 14 and 15.

That is, the average axis crossings of the 38 kHz square waves coincide in time with average axis crossings of the pilot signal component. The balanced synchronous detector 13 comprising transistors 14, 18 and 19 and transistors 15, 20, 21 responds to the combination of the complementary 38 kHz square waves and the push-pull composite signals to produce complementary signals including the difference signal components $[(L-R)]$ and $-(L-R)]$ across resistors 22 and 23. The output voltages produced across resistors 22 and 23, including the complementary difference signal components, are coupled via transistors 24 and 25 to resistors 26 and 27. Transistors 24 and 25, along with resistors 22 and 23, therefore serve as difference signal voltage sources with respect to resistors 26 and 27.

The composite signals provided by amplifier 12, including the audio sum $(L+R)$ component, are provided as currents via transistors 28 and 29 to resistors 26 and 27 remote from transistors 24 and 25. The total signals, including the voltages representing difference signal components and currents representing sum signal components are combined in resistors 26 and 27 to produce the desired left (L) and right (R) audio signals at terminals T_{10} and T_{11} .

Because of the doubly balanced nature of the illustrated synchronous detector and the low pass characteristics of the de-emphasis networks 32, 33, components (e.g., pilot, 38 kHz switching signals, sum signal, etc.) other than the desired left and right audio frequency signals are not produced across the output filter capacitors of networks 32 and 33.

Correct matrixing of the sum and difference signal components is dependent in part upon matching of the currents supplied by the source transistors 14, 15, 28 and 29. In the integrated circuit environment, such matching is relatively easily accomplished by constructing substantially identical transistors 14, 15, 28 and 29 and substantially identical associated emitter resistors 16, 17, 30 and 31 in close proximity on the chip 11.

Correct matrixing is also dependent upon the ratios of resistors 22 and 23 to resistors 26 and 27, respectively. In the illustrated doubly-balanced synchronous detector arrangement, the switching transistors 18, 19, 20, 21 are supplied with 38 kHz symmetrical square waves of correct phasing so that full wave detection of the 38 kHz difference signal sub-carrier signal is obtained. The resultant peak to peak amplitude of the audio frequency components of the detected difference signal is related to the peak magnitude of the rectified difference signal carrier wave at the output of the detector 13 by a factor of $2/\pi$. For a left only or a right only audio signal, the peak amplitude of the modulated difference signal

carrier wave component of the composite signal is set by the standards for stereophonic broadcasting as equal to the peak amplitude of the sum signal component. Therefore, to obtain proper matrixing of the sum and difference signals, resistors 22 and 23, across which the difference signals are developed, are selected $\pi/2$ times as large as the resistors 26 and 27 across which the sum signal components are developed.

The synchronous difference signal detector 13 further comprises means for automatically disabling operation of the difference signal detection circuits, for example, either when the prolonged absence of pilot signal greater than a predetermined amplitude indicates that non-stereophonic (monophonic) program material is being received or when the signal-to-noise ratio of the received signal is judged too poor for satisfactory stereophonic reproduction. One system for producing a "stereo-mono" switching signal is described in the above-identified United Kingdom Patent Application 60162/70 (Serial No. 1,332,515). For purposes of the present discussion it is sufficient to recognize that such a switching signal is produced for either of the above-noted conditions.

In the apparatus shown in the drawing, stereophonic-monophonic switching signals are supplied by a stereo switching signal source 38 to an amplifier comprising a first transistor 39 having a collector electrode connected to a source of operating voltage $(B+)$, a base electrode coupled to stereo switching signal source 38 and an emitter electrode coupled via a resistor 40 to the base electrode of a switching transistor 41. The emitter electrode of transistor 41 is connected to ground and an output switching signal is derived at the collector electrode thereof across a resistor 43 coupled to the source of operating voltage. The output of switching transistor 41 is coupled to a multiple V_{BE} bias supply of the type described in British Patent No. 1,229,274. As used herein, the term V_{BE} is defined as the forward voltage drop across the base-emitter junction of a normally conducting transistor (e.g., approximately 0.65 to 0.7 volts for silicon transistors such as are fabricated in integrated circuits). Reference voltage supplies (usually internal to the integrated circuit) which provide one or more integral multiples of V_{BE} above ground potential at a low impedance are designated as "multiple V_{BE} supplies".

In the present case, the multiple V_{BE} supply comprises a common collector transistor 44 and a common emitter transistor 45 coupled together in a negative feedback arrangement. The collector electrode of transistor 44 is coupled to the source of operating voltage $B+$ while a plurality of resistors 46, 47, 48 are coupled in series relation between the emitter electrode and transistor 44 and ground. The junction of resistors 47 and 48 is connected

to the base electrode of transistors 45. The emitter electrode of transistor 45 is connected to ground while the collector electrode of transistor 45 is directly connected to the base electrode of transistor 44. As is explained in Patent No. 1,229,274, when transistors 44 and 45 are conducting, a voltage equal to V_{BE} exists across resistor 48. Resistor 48 is selected smaller than the base-emitter impedance of transistor 45 and the additional resistors 46, 47 are selected smaller than the input impedances of the respective circuits to which they are coupled. In that case, voltages are developed across each of the series connected resistors 46, and 47 equal to the product of V_{BE} and the ratio between the particular resistor (46 or 47) and resistor 48. Specifically, voltages of $7 V_{BE}$ and $4 V_{BE}$ are developed at the emitter electrode of transistor 44 and at the junction of resistors 46 and 47, respectively.

The junction of resistors 46 and 47 is coupled to a terminal 7 of the difference signal detector 13, to which terminal are also connected the base electrodes of a pair of stereo switching or stereo killer transistors 49 and 50. The emitter electrodes of transistors 49 and 50 are coupled, respectively, to the joined emitter electrodes of switching transistors 18, 19 and the joined emitter electrodes of switching transistors 20, 21.

The collector electrodes of transistors 49 and 50 are directly joined together and this collector junction is connected to the emitter electrodes of respective current splitter transistors 51 and 52 via separate emitter resistors 53 and 54. The base electrodes of current splitter transistors 51 and 52 are directly connected to a terminal 8 of the difference signal detector 13, which terminal is also connected to the emitter electrode of transistor 49 ($7 V_{BE}$ when the multiple V_{BE} supply is operating). The collector electrodes of splitter transistors 51 and 52 are connected to resistors 22 and 23, respectively.

A feedback circuit is coupled between the input and output of the switched multiple V_{BE} supply to increase the rate at which the system switches from stereophonic to monophonic mode. This circuit comprises a transistor 55 having a collector electrode coupled via a resistor 56 to the base electrode of transistor 41, a base electrode coupled via a resistor 57 to the emitter electrode of transistor 44 and an emitter electrode connected to ground.

In operation, upon the loss of stereophonic information suitable for reproduction or when the detected signal is too noisy for satisfactory reproduction as explained in the above referred to United Kingdom Application No. 60162/70 (Serial No. 1,332,515) the voltage at the base electrode of transistor 39 falls below a predetermined level (e.g., one volt) and transistors 39 and 41 begin to switch to an off or non-conductive condition. The volt-

age at the base electrode of transistor 44 increases positively causing transistor 44 and then transistor 45 to conduct so that the multiple V_{BE} supply switches on. This switching action is aided by the presence of transistor 55 which commences conduction along with transistors 44 and 45. Transistor 55 serves to switch transistor 41 off rapidly once the switching operation begins. A positive voltage ($4 V_{BE}$) provided at the junction of resistors 46 and 47 to terminal 7 of the difference signal detector 13, causes killer transistors 49 and 50 to conduct. Similarly, a positive voltage ($7 V_{BE}$) provided at the emitter electrode of transistor 44 to terminal 8 of the difference signal detector 13, causes splitter transistors 51 and 52 to conduct.

When killer transistors 49 and 50 conduct, a sufficiently positive voltage ($3 V_{BE}$) is coupled to the joined emitter electrodes of switching transistors 18 and 19 and to the joined emitter electrodes of switching transistors 20, 21 to reverse bias such switching transistors and thereby disable the difference signal detector 13. The push-pull composite signals supplied via current source transistors 14 and 15 are then diverted through killer transistors 49 and 50 and cancel each other at the joined collector electrodes of transistors 49, 50.

The joined collector electrodes of transistors 49 and 50 also serve to combine the direct current components of the outputs of current source transistors 14 and 15. The combined direct current components are then split into equal components by means of resistors 53, 54 and transistors 51, 52 and the equal components are coupled to load resistors 22 and 23. The direct bias voltage coupled to matrix transistors 24 and 25 is therefore maintained substantially equal for either stereophonic or monophonic reproduction modes. If such direct bias voltage were allowed to change the operating mode of the system changed, a thump would be heard in the associated loudspeakers. The above-described arrangement prevents production of such an undesirable sound.

The disabling of the product detector 13 by diverting the currents applied to its terminals 1 and 2, splitting each of the diverted currents into halves and applying the halves of each of the diverted currents to different ones of its output terminals 5 and 6 can be accomplished in other ways in accordance with the principles of the present invention using control signals provided by the same keyed multiple V_{BE} source. For instance, the base electrodes of transistors 49 and 50 need not be connected through terminal 7 to the junction of resistors 46 and 47 of the switched multiple V_{BE} supply. Instead, the base electrodes of transistors 49 and 50 may be connected to their collector electrodes.

The connection of the base and collector electrodes of a transistor makes it function as

a unilaterally conductive device. This unilaterally conductive device functions just as a semiconductor rectifier diode does and may be replaced by a diode. In the configuration shown in the drawing or in the variation just discussed, the resistors 53 and 54 may be replaced by direct connections if the transistors 51 and 52 have well matched characteristics. The resistors 53 and 54 split the current into more equal halves than transistors 51 and 52 if the tolerances upon the matching of the resistors are more easily maintained than those upon the matching of the emitter input impedances of the transistors in common base connection.

Another variation of the configuration shown in the drawing is to disconnect the base electrodes of transistors 51 and 52 from each other and from the connection through terminal 8 to the switched multiple V_{BE} supply. Instead, the base electrode of each of the transistors 51 and 52 is connected to the collector electrode of that transistor, causing both of the transistors 51 and 52 to function as a unilaterally conductive device replaceable with a diode. The resistors 53 and 54 may be replaced by direct connections, and the splitting of current between transistors 51 and 52, connected to be unilaterally conductive, may be improved by their resistance during conduction being supplemented respectively by the resistances of resistors 22 and 23.

It is also possible to modify the configuration shown in the drawing by removing the transistors 51, 52; the resistors 53, 54 and the interconnection between the collector electrodes of transistors 49, 50. First and second supplementary transistors are connected into the circuit with their base-emitter junctions in parallel connection, respectively, with the base-emitter junctions of transistors 49 and 50. The collector electrodes of the first supplementary transistor and transistor 50 are connected together and to terminal 6 of the product detector. The collector electrodes of the second supplementary transistor and transistor 49 are connected together and to terminal 5 of the product detector. The couplings of each of the emitter electrodes of the first and second supplementary transistors and transistors 49 and 50 to one of the input terminals 1, 2 of the product detector may, in order to make the splitting of the diverted current into halves more precise, be made through equal-valued resistors rather than by direct connections.

A modification of the configuration shown in the drawing, which may be made if $B+$ voltage is high enough, is to connect terminal 8 to a fixed voltage source in the 5 volt range. The configuration shown in the drawing is advantageous in situations where $B+$ voltage is lower valued, because the collector-base junctions of transistors 51 and 52 are biased near ground during normal detector operation and do not interfere with peak downward

voltage swings of the signals at the terminals 5, 6 of the difference signal detector 13.

Each of the above-described arrangements for disabling the product detector 13 is applicable to color-killing arrangements for chrominance signal demodulators using such a product detector, which are used in some color television receivers. The disabling of the chrominance signal demodulators would be done only when detection of the amplitude of the color burst in a received and detected color television signal could not detect the presence of a suitably, large noise-free color burst signal.

The switching characteristics of the multiple V_{BE} supply display a hysteresis effect as will be explained. The difference signal detector is maintained in an inoperative or bypassed condition until an input to transistor 39 representative of, for example, the presence of adequate pilot signal is provided to switch transistors 39 and 41 on and to thereby switch both the multiple V_{BE} supply and each of the detector disabling circuitry transistors off.

As noted above, an input signal greater than approximately one volt (low current V_{BE} of transistor 39 plus normal current V_{BE} of transistor 41) is sufficient to maintain conduction of transistors 39 and 41 (and therefrom maintain operation in the stereophonic mode). However, when transistors 39 and 41 are switched off and transistor 55 is on (i.e., monophonic operating mode), a positive voltage greater than one volt is required at the base of transistors 39 to re-initiate stereophonic operation since resistors 40 and 56 are then coupled via transistor 55 as a voltage divider across the input (base emitter) terminals of transistor 41.

An input voltage of approximately 3 V_{BE} (approximately two volts) is thus required at the base of transistor 39 to switch to stereophonic mode. The difference between the levels required at the base of transistor 39 to initiate and to remain in stereophonic mode thus provides a desirable hysteresis characteristic whereby once stereophonic reproduction is initiated it will be maintained even though momentary fluctuations occur either in the received pilot signal level or in signal-to-noise ratio of the detected signal.

When stereophonic information suitable for reproduction is received and processed by the associated receiver, a sufficiently positive input voltage is supplied to the base of transistor 39 to render it conductive. Transistor 41 also conducts, so that the input to transistor 44 is not sufficiently positive to produce conduction in transistor 44. The multiple V_{BE} supply comprising transistors 44 and 45 is therefore switched "off" and each of transistors 49, 50, 51 and 52 is switched "off". Under these conditions, the difference signal detector circuits 13 operate to produce $(L-R)$ and $-(L-R)$ signals in the manner previously described. It should also be noted that transistor 55 is off under these conditions.

The above-described matrix amplifier and automatic switching arrangement also provides the advantage that, should the output terminals T_{10} and T_{11} accidentally be shorted to ground, the resistors 26 and 27 serve to limit current in the associated transistors and afford short circuit protection to them.

WHAT WE CLAIM IS:—

1. A detector capable of inactivation in response to an electric control signal, said detector comprising a detection circuit having a first and second input, each input exhibiting unidirectionally conductive characteristics, and signal current to be detected and a first input being adapted for application of a first input signal current to be detected and a first input quiescent bias current, said second input being adapted for application of a second input signal current to be detected and a second input quiescent bias current, said first and said second input signal currents being in push-pull relationship with each other, said first and said second outputs respectively providing a first and a second detected output signal current in response to the application of said first and said second input quiescent bias currents and said first and said second input signal currents, said first and said second detected output signal currents respectively being accompanied by a first and a second output quiescent current, each of said quiescent output currents being equal to one-half the sum of said first and said second input quiescent bias currents, said detector further comprising connection means for connecting each of said first and said second outputs of said detection circuit to a source of energizing potential and switching means responsive to said electric control signal to direct current conductively couple each of said detection circuit inputs to each of said detection circuit outputs through paths of similar conductivity, whereby said application of said first and said second input quiescent bias currents and said first and second input signal currents will cause current flow through said paths rather than through said detection circuit and only quiescent current flow through said connection means.

2. A detector as claimed in Claim 1, in which said switching means includes first, second, third and fourth switching elements responsive to said electric control signal to place them into non-conduction during normal operation of said detector and into conduction to inactivate said detector, said first, second, third and fourth switching elements connected between a common point of connection and, respectively, said first detection circuit input, said second detection circuit input, said first detection circuit output and said second detection circuit output.

3. A detector as claimed in Claim 2, in which a source of selectable potentials, its

potential being changeable to provide said electric control signal; said first and second switching elements including first and second transistors respectively of the same conductivity type, each having its base electrode connected to said source of selectable potentials, its collector electrode connected to said common point of connection, and its emitter electrode direct current conductively coupled to a different one of said first and said second detection circuit inputs; and said third and fourth switching elements including, respectively, first and second unidirectionally conductive devices connecting said common point of connection to, respectively, said first and said second detection circuit outputs and poled to jointly conduct the combined collector currents of said first and second transistors.

4. A detector as claimed in Claim 2, comprising a source of selectable potentials, its potential being changeable to provide said electric control signal; said first and second switching elements including first and second transistors, respectively, of the same conductivity type, each having its base electrode connected to said source of selectable potentials, its emitter electrode direct current conductively coupled to said point of common connection, and its collector electrode connected to a different one of said first and said second detection circuit outputs; and said third and fourth switching elements including, respectively, first and second unidirectionally conductive devices connecting said common point of connection to, respectively, said first and said second detection circuit inputs and poled to jointly conduct the combined emitter currents of said first and second transistors.

5. A detector as claimed in Claim 2, comprising first and second sources of selectable potentials, the potential of at least said first source of selectable potential being changeable to provide said electric control signal; said first and second switching elements including first and second transistors, respectively, each having its base electrode connected to said first source of selectable potentials, its collector electrode connected to said common point of connection and its emitter electrode direct current conductively coupled to a different one of said first and said second detection circuit inputs; and said third and fourth switching elements including third and fourth transistors respectively, each having its base electrode connected to said second source of selectable potentials, its emitter electrode direct current conductively coupled to said common point of connection and its collector electrode connected to a different one of said detection circuit outputs, said first, said second, said third and said fourth transistors all being of the same conductivity type.

6. A detector as claimed in Claim 1, comprising first, second, third and fourth switching elements responsive to said electric control

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The above-described matrix amplifier and automatic switching arrangement also provides the advantage that, should the output terminals T_{10} and T_{11} accidentally be shorted to ground, the resistors 26 and 27 serve to limit current in the associated transistors and afford short circuit protection to them.

WHAT WE CLAIM IS:—

1. A detector capable of inactivation in response to an electric control signal, said detector comprising a detection circuit having a first and second input, each input exhibiting unidirectionally conductive characteristics, and signal current to be detected and a first input being adapted for application of a first input signal current to be detected and a first input quiescent bias current, said second input being adapted for application of a second input signal current to be detected and a second input quiescent bias current, said first and said second input signal currents being in push-pull relationship with each other, said first and said second outputs respectively providing a first and a second detected output signal current in response to the application of said first and said second input quiescent bias currents and said first and said second input signal currents, said first and said second detected output signal currents respectively being accompanied by a first and a second output quiescent current, each of said quiescent output currents being equal to one-half the sum of said first and said second input quiescent bias currents, said detector further comprising connection means for connecting each of said first and said second outputs of said detection circuit to a source of energizing potential and switching means responsive to said electric control signal to direct current conductively couple each of said detection circuit inputs to each of said detection circuit outputs through paths of similar conductivity, whereby said application of said first and said second input quiescent bias currents and said first and second input signal currents will cause current flow through said paths rather than through said detection circuit and only quiescent current flow through said connection means.

2. A detector as claimed in Claim 1, in which said switching means includes first, second, third and fourth switching elements responsive to said electric control signal to place them into non-conduction during normal operation of said detector and into conduction to inactivate said detector, said first, second, third and fourth switching elements connected between a common point of connection and, respectively, said first detection circuit input, said second detection circuit input, said first detection circuit output and said second detection circuit output.

3. A detector as claimed in Claim 2, in which a source of selectable potentials, its

potential being changeable to provide said electric control signal; said first and second switching elements including first and second transistors respectively of the same conductivity type, each having its base electrode connected to said source of selectable potentials, its collector electrode connected to said common point of connection, and its emitter electrode direct current conductively coupled to a different one of said first and said second detection circuit inputs; and said third and fourth switching elements including, respectively, first and second unidirectionally conductive devices connecting said common point of connection to, respectively, said first and said second detection circuit outputs and poled to jointly conduct the combined collector currents of said first and second transistors.

4. A detector as claimed in Claim 2, comprising a source of selectable potentials, its potential being changeable to provide said electric control signal; said first and second switching elements including first and second transistors, respectively, of the same conductivity type, each having its base electrode connected to said source of selectable potentials, its emitter electrode direct current conductively coupled to said point of common connection, and its collector electrode connected to a different one of said first and said second detection circuit outputs; and said third and fourth switching elements including, respectively, first and second unidirectionally conductive devices connecting said common point of connection to, respectively, said first and said second detection circuit inputs and poled to jointly conduct the combined emitter currents of said first and second transistors.

5. A detector as claimed in Claim 2, comprising first and second sources of selectable potentials, the potential of at least said first source of selectable potential being changeable to provide said electric control signal; said first and second switching elements including first and second transistors, respectively, each having its base electrode connected to said first source of selectable potentials, its collector electrode connected to said common point of connection and its emitter electrode direct current conductively coupled to a different one of said first and said second detection circuit inputs; and said third and fourth switching elements including third and fourth transistors respectively, each having its base electrode connected to said second source of selectable potentials, its emitter electrode direct current conductively coupled to said common point of connection and its collector electrode connected to a different one of said detection circuit outputs, said first, said second, said third and said fourth transistors all being of the same conductivity type.

6. A detector as claimed in Claim 1, comprising first, second, third and fourth switching elements responsive to said electric control



- signal to place them into non-conduction during normal operation of said detector and into conduction to inactivate said detector, said first switching element connected between said first input and said first output of said detection apparatus, said second switching element connected between said first input and said second output of said detection apparatus, said third switching element connected between said second input and said first output of said detection apparatus and said fourth switching element connected between said second input and said second output of said detection apparatus.
- 5 7. A detector as claimed in Claim 6, comprising a source of selectable potentials, its potential being changable to provide said electric control signal, and said first, second, third and fourth switching elements including
- 10 first, second, third and fourth transistors, respectively, of the same conductivity type, each having its base electrode connected to said source of selectable potentials, the emitter
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electrodes of said first and said second transistors being direct current conductively coupled to said first detection circuit input, the emitter electrodes of said third and said fourth transistors being direct current conductively coupled to said second detection circuit input, the collector electrodes of said first, and said fourth transistors being connected to said first detection circuit output and the collector electrodes of said second and said third transistors being connected to said second detection circuit output.

8. A detector having inactivating circuitry therefor constituted, connected and operable substantially as hereinbefore described with reference to elements 49—54 in the accompanying drawings.

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