Description

The invention relates to a switched-mode power supply circuit for converting a DC input voltage to a DC output voltage, comprising a series arrangement of a controllable power switch and an inductive element coupled between the input voltage terminals, control means for rendering the power switch alternately conducting a non-conducting, a rectifier coupled to the inductive element for making the output voltage available, the inductive element and a capacitor coupled thereto forming a part of a resonant circuit in the periods of time when the switch and the rectifier are currentless, in which resonant circuit a voltage oscillation is then present and means for interrupting the oscillation present in the resonant circuit.

Such switched-mode power supply circuits including a resonant circuit are known. Examples are described in Netherlands Patent Application 8702339 (PHN 11.470) in the name of the Applicant. The output voltage can be maintained substantially constant in spite of possible variations of the input voltage and/or of a load connected to the output voltage, for example, because the frequency of the control signals applied to the controllable switch is controlled as a function of this output voltage. The control signals may originate from an oscillator, or, in a different manner, the circuit may be self-oscillating.

In the German Patent Application DE-A 35 43 299 a power supply has been described comprising means for interrupting the oscillation present in a resonant circuit. The purpose of interrupting the oscillation is the demagnetization of a transformer.

According to the invention a power supply circuit of the type described above is characterized in that the means are adapted to interrupt the oscillation at an instant when the voltage across the inductive element or the current through the capacitor is substantially zero.

Due to this measure the oscillation is interrupted at a high signal level, namely at an instant when either the current through the inductance, or the voltage across the capacitor and hence the energy stored in the relevant element has an extreme value. During the interruption these quantities approximately maintain their extreme value, whereafter the oscillation is resumed from this value. As will be apparent from the further description, such an interruption has a number of advantages. For example, free oscillations, which would otherwise occur, can be eliminated so that the energy dissipated by the circuit is reduced. The means for interrupting the oscillation may be synchronizing means, the successive final instants of the interruption being periodically located with respect to time. In this way the circuit always operates at the same frequency, which may be desirable. In one embodiment the circuit can thus be synchronized by means of these means, whilst free oscillations do not occur and the energy which is dissipated by turning on the power switch can be reduced in the manner as described in the said Patent Application. In another embodiment, the circuit being a DC flyback converter which operates in a discontinuous mode, thus in which the current through the inductance becomes zero during the occurrence of the oscillation the turn-on losses are reduced due to the interruption according to the invention, whilst the circuit is synchronized in another, known manner.

If the invention is used in a picture display device, the circuit may be advantageously characterized in that the said instants succeed one another at the same frequency as a line deflection signal which is active in the picture display device, or at a multiple of this frequency. As a result, a disturbance which is caused by switching the various switching elements of the circuit is stationary with respect to the line deflection. If the disturbance is visible on a display screen, it is not very troublesome.

The circuit according to the invention is advantageously characterized in that the means for interrupting the oscillation constitute a clamping circuit for maintaining the voltage across the inductive element substantially zero at and after an instant when this voltage has become substantially zero. This measure ensures that the voltage across the capacitor does not substantially vary during the interruption. Preferably, the clamping circuit comprises a unidirectional current-conducting element which is arranged in series with a second switch, the series arrangement formed being arranged in parallel to the inductive element. This ensures that the interruption commences at the correct instant, which is safe for the capacitor because there occurs no voltage step.

In another embodiment the circuit is characterized in that the means for interrupting the oscillation comprise a second controllable switch arranged in series with the capacitor for interrupting the current path of the capacitor at an instant when the current therethrough is substantially zero. However, such an embodiment can only be realized in practice if the capacitance across the inductive element is small with respect to that of the capacitor of the resonant circuit.

The invention will now be described in greater detail, by way of example, with reference to the accompanying drawings in which

Fig. 1 shows the circuit diagram of a first embodiment of the circuit according to the invention,

Fig. 2 shows waveforms occurring therein,

Fig. 3 shows the circuit diagram of a second embodiment of the circuit according to the invention,

Fig. 4 shows waveforms occurring in this second embodiment,

Fig. 5 shows waveforms occurring in the first embodiment of the circuit in the case of variations of the input voltage and/or the load,

Fig. 6 shows a more detailed circuit diagram of an embodiment of the circuit according to the principle of Fig. 1,

Fig. 7 shows waveforms occurring in the circuit of Fig. 6 and

Fig. 8 shows the circuit diagram of a third embodiment of the circuit according to the invention.

The power supply circuit of Fig. 1 comprises a controllable power switch in the form of an NPN power switching transistor Tr whose collector is connected to an inductance L and whose emitter is connected to ground. The other end of element L is connected to the positive rail of a DC input voltage source V_I whose negative rail is also connected to ground and which is, for example a mains rectifier. The anode of a rectifier D, the anode of a diode D1 and a capacitor C are also connected to the collector of transistor Tr. A second controllable switch S is arranged between the cathode of diode D1 and the said positive rail and a smoothing capacitor C_o and a load represented by a resistor R are arranged between the cathode of rectifier D and the same rail. The terminal of capacitor C which is not connected to the collector is connected to ground. The base lead of transistor Tr incorporates known control means (not shown) for turning the transistor alternately on and off. The control means of switch S are not shown either. In operation, a DC voltage V_o is present across the parallel arrangement of elements C_o and R, which voltage is the output voltage of the circuit of Fig. 1 and the voltage $V_I + V_o$ is present at the junction point of elements D, C_o and R.

Fig. 2a shows the variation of the voltage V across inductance L and Fig. 2b shows the variation of the current I through L. Transistor Tr is turned on before an instant t_o. The voltage at the collector is substantially zero, so that voltage V is substantially equal to V_I, whilst current I increases linearly so that energy is stored in inductance L. The transistor is turned off at instant t_o so that the voltage at the collector increases in accordance with a sine function of time, whilst voltage V decreases in accordance with the same function and whilst current I varies in accordance with a cosine function of time. These functions are determined by the tuning frequency of the resonant circuit constituted by inductance L and capacitor C. At an instant t_1 voltage V reaches the value of zero and current I is maximal. Until instant t_1 the state of switch S, i.e. conducting or non-conducting, is irrelevant because the voltage at the anode of diode D1 is lower than V_I. Therefore, if switch S is conducting at instant t_1 or at an instant before t_1, current I does not start flowing through diode D1 and switch S until after this instant. Diode D1 and switch S constitute a clamping circuit by which the voltage at the collector of transistor Tr is clamped substantially at the value V_I, whilst voltage V becomes substantially zero because the voltage drop across elements D1 and S is very low, and whilst current I remains substantially at the value which it had at the time of t_1. As a result, the oscillation is interrupted. This state is maintained as long as switch S remains conducting.

At an instant t_2 switch S is blocked and the oscillation is resumed. Current I again flows to capacitor C. The voltage thereacross increases above the value V_I so that voltage V becomes negative in accordance with the sine function, whilst current I decreases in accordance with the cosine function. The voltage across capacitor C continues to increase until the value $V_I + V_o$ is reached at an instant t_3, which causes rectifier D to conduct. Voltage V then remains equal to $-V_o$, whilst current I decreases linearly and flows to capacitor C_o for recharging it, more specifically until the value of zero is reached at an instant t_4. Element L then no longer has any energy. After instant t_4 rectifier D conveys no current so that inductance L and capacitor C again constitute a resonant circuit. The capacitor is now discharged in the inductance in accordance with the same cosine function as before and current I has the negative polarity. Voltage V increases from the value $-V_o$ in accordance with the same sine function as before. At an instant t_5 voltage V passes the value of zero and at an instant t_6 current I becomes zero whilst voltage V reaches the value V_o and whilst the voltage at the collector of transistor Tr assumes the value $V_I - V_o$. This is the lowest possible value of this voltage. At instant t_6 transistor Tr is turned on, for example in the way as described in Netherlands Patent Application 8502339 (PHN 11.470) in the name of the Applicant. The text of this Application is incorporated herein by reference. The collector current of the transistor flows through inductance L and this current increases in accordance with a linear function of time. This is the same situation as before instant t_o.

It is apparent from the foregoing that the duration of the time interval between t_1 and t_2 in which the oscillation is interrupted is determined by the location of the instant t_2 at which switch S is blocked. This instant is a synchronizing instant and it corresponds to the trailing edge of a pulse applied to switch S. The leading edge of this pulse

may occur at any instant which is located at or after the instant at which the voltage at the collector of transistor Tr comes below the value V_i, i.e. instant being one period earlier than instant t_5 in Fig. 2, and before or at instant t_1. In the absence of a periodically occurring synchronizing pulse the interval between t_1 and t_2 is reduced to zero and the circuit has a natural frequency which is determined, for example by an oscillator which is incorporated in the control means of transistor Tr. In another manner, the circuit of Fig. 1 may form part of a self-oscillating supply circuit which is free running in the absence of a synchronizing pulse. It appears that in the case of synchronization the instants located in Fig.2 after instant t_1 are delayed so that the oscillation period is longer and consequently the frequency is lower than would be the case in the event of free oscillation.

In the embodiment of Fig.3 in which the same elements as those in Fig. 1 are denoted by the same symbols, the conductivity direction of diode D1 is reversed with respect to that in Fig. 1. In this case the conductance of switch S is of influence for interrupting the oscillation which is present during the turn-off time of transistor Tr when the voltage at the collector of transistor Tr becomes lower than V_i, i.e. at instant t_5. The leading edge of the synchronizing pulse may thus occur at any instant which is located at or after instant t_1 and before or at instant t_5, whilst the trailing edge occurs at the synchronizing instant. Figs. 4a and 4b show for the embodiment of Fig. 3 variations similar to those shown in Figs. 2a and 2b.

Both embodiments have advantages and drawbacks. It is apparent from Figs. 2b and 4b that as compared with the embodiment of Fig. 3, the embodiment of Fig. 1 has the drawback that the current flowing during the interruption has a larger intensity resulting in the dissipation losses caused by this current in inductance L, switch S and diode D1 being higher. On the other hand the first embodiment is safer. If switch S becomes defective and remains permanently open, the circuit is not synchronizable in either case so that a higher frequency is caused without further consequences occurring, but if the switch constitutes a permanent short circuit, no detrimental effect will occur in the first-mentioned case. No replenishing energy is supplied to capacitor C_o so that the energy stored therein will disappear soon. In the second case transistor Tr is permanently turned on, which may be very harmful for the transistor. In the embodiment of Fig. 1 a safety provision (not shown) may be added ensuring that switch S will conduct as long as, for example a too high output voltage occurs. For this purpose the circuit comprises known means for comparing the relevant quantity with a predetermined limit value and for controlling switch S when this value is exceeded.

In the embodiments described the interruption of the oscillation by means of the clamping circuit with elements D1 and S is used for synchronizing the power supply circuit at a high signal level. It will be noted that in the embodiment of Fig. 3 the interruption can be utilized for another purpose. In a circuit according to Fig. 3 the oscillation would subsist in the absence of elements D1 and S after the instant at which rectifier D becomes currentless, i.e. the instant corresponding to t_4 in Fig. 4, more specifically in accordance with ever the same sinusoidal variation and with a decreasing amplitude. The oscillation would then end at the instant when transistor Tr is turned on by means of a control signal, for example by the control means described in the above-mentioned Patent Application, which means can be utilized for synchronizing the circuit. However, this will generally not take place at a moment when the voltage at the collector of transistor Tr has a minimum value and which corresponds to, for example t_5 in Fig. 4 so that high turn-on losses are caused. To reduce these losses, the clamping circuit with elements D1 and S can be used for interrupting the oscillation at the instant when the voltage at the collector has a minimum value, which voltage is maintained at the then assumed value $V_i - V_o$, whilst current I remains zero, more specifically until the instant when transistor Tr is turned on by the control means.

Fig. 5a shows the variation of the collector-emitter voltage V_{ce} of transistor Tr for the embodiment of Fig. 1, and Fig. 5b shows the variation of the magnetizing current I for the same embodiment. The solid lines apply to the nominal case, i.e. the case where both the input voltage V_i and the load R have the values calculated during the design. The broken lines apply to a larger load, i.e. a lower value of resistor R at nominal input voltage and the dotted lines apply to a nominal load at a decreased input voltage. It appears from the plotted curves that a larger load causes a longer conductivity time for rectifier D and also for transistor Tr and a larger amplitude for current I and that in the case of a lower input voltage transistor Tr is conducting for a longer period, whilst current I has the same amplitude as in the nominal case. In Figs. 5a and b the reference Sy indicates the synchronizing instant.

Fig. 6 shows the relevant part of a practical embodiment of a power supply circuit in accordance with the principle of Fig. 1. In Fig. 6 inductance L is replaced by a transformer T, a primary winding L1 of which is arranged in series with transistor Tr. The series circuit formed is arranged between the rails of voltage V_i and capacitor C is arranged parallel to the collector-emitter path of transistor Tr. A secondary winding L2 of trans-

former T is connected to ground at one end and is connected at the other end to the same elements D1 and D as in Fig. 1. The winding sense of windings L1 and L2, denoted, as usual, by means of dots, as well as the conductivity direction of rectifier D are such that a current flows through the one winding whilst the other winding does not convey a current ("flyback" effect). Switch S is formed with a field effect transistor whose gate is connected to an output of a driver circuit Dr, whose drain is connected to the cathode of diode D1 and whose source is connected to ground. The input of circuit Dr is connected to an output Q of a flipflop FF. A second secondary winding L3 of transformer T has the opposite winding sense with respect to winding L2. Winding L3 is connected to ground at one end and at the other end to a doublesided limiter constituted by a resistor R1 and two diodes D2 and D3. Free oscillations caused by the spread of transformer T are somewhat integrated by means of a capacitor C1 and the signal obtained is amplified by means of an amplifier A whose output is connected to the set input S of flipflop FF. The synchronizing signal for controlling switch S is applied to the reset input R of flipflop FF. Capacitor C_o and load R are connected between the cathode of rectifier D and ground which is DC isolated from the input voltage V_i by means of transformer T.

The circuit of Fig. 6 is used, for example in a picture display device, for example a television receiver for supplying a number of circuits which are connected to the direct voltage V_o which is present across capacitor C_o. Other, secondary windings not shown in Fig. 6 may be provided on the core of transformer T for generating other supply voltages. One of these voltages is the EHT for the final anode of a picture display tube. A ripple voltage which is caused by switching of the switching elements of the circuit of Fig. 6 is present on these voltages, and particularly on the EHT. The disturbance caused thereby will be stationary and will therefore not be very troublesome in the event that the disturbance is visible on the display screen of the display tube if the synchronizing signal applied to flipflop FF is derived from a line deflection signal which is active in the picture display device and if it has the same frequency as this signal or a multiple of this frequency. This measure precludes the use of a filter for reducing the switching ripple on the EHT lead. Voltage V_o and the possible other output voltages of the circuit of Fig. 6 can be stabilized in known manner against variations of the input voltage and/or the various loads, for example by controlling the conductivity time of transistor Tr as a function of voltage V_o.

Some voltage variations in the circuit of Fig. 6 are shown: these are the variations of the voltage across winding L1 (Fig. 7a), at the input S of flipflop FF (Fig. 7b), at the input R of the flipflop (Fig. 7c) and at the output Q of the flipflop (Fig. 7d). It is apparent therefrom that the flipflop is set at the instant during the turn-off time of transistor Tr when the voltage of Fig. 7a passes the value of zero, which would result in the transistor S being turned on in the absence of diode D1. This situation is maintained until the zero crossing of the voltage across winding L2 during the subsequent conductivity time of transistor Tr, whereafter a current flows through diode D1 and transistor S, which interrupts the oscillation across the resonant circuit constituted by the various inductances and capacitances. The voltage pulse of Fig. 7b terminates at the instant of commencement of the interruption, but this has no influence on the voltage of Fig. 7d so that transistor S remains turned on. At the instant Sy when the leading edge of the synchronizing pulse occurs, flipflop FF is reset so that the voltage of Fig. 7d becomes low, which results in transistor S being turned off and the oscillation being resumed.

Modifications of the circuits shown in Figs. 1 and 3 can be conceived. For example, capacitor C may be arranged parallel to inductance L in Figs. 1 and 3, or to winding L1 or L2 in Fig. 6. Also the terminal of capacitor C which is not connected to rectifier D may be connected to the negative rail instead of to the positive rail of voltage V_i. In this case the circuit operates as an "up-converter", in which the output voltage V_o, dependent on the conductivity time of transistor Tr with respect to the period, is equal to or higher than the input voltage V_i, instead of the flyback converter of Figs. 1, 3 and 6 in which voltage V_o is equal to or lower than voltage Vi.

Another modification is shown in Fig. 8. Compared with Fig. 1, switch S is not arranged parallel to inductance L but in series with capacitor C. Such a modification can only be realized in practice if the capacitance across inductance L is small with respect to that of capacitor C. The oscillation during the turn-off time of transistor Tr is interrupted because switch S is rendered non-conducting by suitable control means, more specifically at an instant when the current flowing through inductance L and capacitor C is zero, but preferably not at the instant when the voltage at the collector of transistor Tr has the maximum value but at the later instant when this voltage has its minimum value. After this instant the current remains zero, whilst the said voltage remains at the value $V_i - V_o$ assumed at this instant and whilst the voltage V across inductance L remains at the value V_o. This situation is maintained until transistor Tr is turned on again. Fig. 8 shows the variation of the voltage at the collector. It may be noted that in the modification of Fig. 8 the energy which is dissipated by

turning on the transistor is minimum and that free oscillations, which would otherwise occur after instant t_6, are eliminated. As was the case with the circuit of Fig. 3, the interruption of the oscillation may be used in the case of the embodiment of Fig. 8 for minimizing the dissipated energy instead of for synchronizing purposes.

Claims

1. A switched-mode power supply circuit for converting a DC input voltage (V_i)into a DC output voltage (V_o), comprising a series arrangement of a controllable power switch (T_r) and an inductive element (L) coupled between the input voltage terminals, control means for rendering the power switch alternately conducting and non-conducting, a rectifier (D) coupled to the inductive element for making the output voltage available, the inductive element and a capacitor (C) coupled thereto forming a part of a resonant circuit in the periods of time when the switch and the rectifier are currentless, in which resonant circuit a voltage oscillation is then present, and means (S, D_1) for interrupting the oscillation present in the resonant circuit, characterized in that the means are adapted to interrupt the oscillation at an instant when the voltage across the inductive element (L) or the current through the capacitor (C) is substantially zero.

2. A circuit as claimed in Claim 1, characterized in that the means for interrupting the oscillation are synchronizing means, whilst the successive final instants of the interruption being periodically located with respect to time.

3. A circuit as claimed in Claim 2 for use in a picture display device, characterized in that the said instants succeed one another at the same frequency as a line deflection signal which is active in the picture display device, or at a multiple of said frequency.

4. A circuit as claimed in Claim 1, characterized in that the means for interrupting the oscillation constitute a clamping circuit for maintaining the voltage across the inductive element (L) substantially zero at and after an instant when said voltage has become substantially zero.

5. A circuit as claimed in Claim 4, characterized in that the clamping circuit comprises a unidirectional current conducting element (D_1) which is arranged in series with a second switch (S), the series arrangement formed being arranged in parallel to the inductive element.

6. A circuit as claimed in Claim 4, characterized in that the instant at which the clamping circuit starts to be operative is located shortly before a turn-on instant of the power switch.

7. A circuit as claimed in Claims 5 and 6, characterized in that a pulse applied to the second controllable switch (S) for rendering said switch conducting has a leading edge which occurs simultaneously with or after the instant when the voltage across the inductive element (L) becomes zero after a turn-off instant of the power switched (T_r), but not later than the zero crossing of the said voltage before the subsequent turn-on instant of the power switch, and a trailing edge which does not occur earlier than the last-mentioned zero crossing.

8. A circuit as claimed in Claim 4, characterized in that the instant when the clamping circuit starts to be operative is located shortly after a turn-off instant of the power switch (T_r).

9. A circuit as claimed in Claims 5 and 8, characterized in that a pulse applied to the second controllable switch (S) for rendering said switch conducting has a leading edge which occurs simultaneously with or after the instant when the voltage across the inductive element (L) becomes zero before a turn-on instant of the power switch, but not later than the zero crossing of said voltage after the subsequent turn-off instant of the power switch (T_r), and a trailing edge which does not occur earlier than the last-mentioned zero crossing.

10. A circuit as claimed in Claim 9, characterized by a bistable element (FF) for applying the control pulse to the second controllable switch (S), the edges of a set pulse applied to the bistable element each time occurring during a zero crossing of the voltage across the inductive element (L) and the leading edge of a reset pulse also applied to the bistable element occurring at the final instant of the interruption.

11. A circuit as claimed in Claim 8, characterized by means (L_3, R_1, D_2, D_3, C_1, A) for comparing a quantity occurring in the circuit with a predetermined limit value and for activating the clamping circuit when said limit value is exceeded.

12. A circuit as claimed in Claim 1, characterized in that the means for interrupting the oscillation

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turning on the transistor is minimum and that free oscillations, which would otherwise occur after instant t_5, are eliminated. As was the case with the circuit of Fig. 3, the interruption of the oscillation may be used in the case of the embodiment of Fig. 8 for minimizing the dissipated energy instead of for synchronizing purposes.

Claims

1. A switched-mode power supply circuit for converting a DC input voltage (V_i) into a DC output voltage (V_o), comprising a series arrangement of a controllable power switch (T_r) and an inductive element (L) coupled between the input voltage terminals, control means for rendering the power switch alternately conducting and non-conducting, a rectifier (D) coupled to the inductive element for making the output voltage available, the inductive element and a capacitor (C) coupled thereto forming a part of a resonant circuit in the periods of time when the switch and the rectifier are currentless, in which resonant circuit a voltage oscillation is then present, and means (S, D_1) for interrupting the oscillation present in the resonant circuit, characterized in that the means are adapted to interrupt the oscillation at an instant when the voltage across the inductive element (L) or the current through the capacitor (C) is substantially zero.

2. A circuit as claimed in Claim 1, characterized in that the means for interrupting the oscillation are synchronizing means, whilst the successive final instants of the interruption being periodically located with respect to time.

3. A circuit as claimed in Claim 2 for use in a picture display device, characterized in that the said instants succeed one another at the same frequency as a line deflection signal which is active in the picture display device, or at a multiple of said frequency.

4. A circuit as claimed in Claim 1, characterized in that the means for interrupting the oscillation constitute a clamping circuit for maintaining the voltage across the inductive element (L) substantially zero at and after an instant when said voltage has become substantially zero.

5. A circuit as claimed in Claim 4, characterized in that the clamping circuit comprises a unidirectional current conducting element (D_1) which is arranged in series with a second switch (S), the series arrangement formed being arranged in parallel to the inductive element.

6. A circuit as claimed in Claim 4, characterized in that the instant at which the clamping circuit starts to be operative is located shortly before a turn-on instant of the power switch.

7. A circuit as claimed in Claims 5 and 6, characterized in that a pulse applied to the second controllable switch (S) for rendering said switch conducting has a leading edge which occurs simultaneously with or after the instant when the voltage across the inductive element (L) becomes zero after a turn-off instant of the power switched (T_r), but not later than the zero crossing of the said voltage before the subsequent turn-on instant of the power switch, and a trailing edge which does not occur earlier than the last-mentioned zero crossing.

8. A circuit as claimed in Claim 4, characterized in that the instant when the clamping circuit starts to be operative is located shortly after a turn-off instant of the power switch (T_r).

9. A circuit as claimed in Claims 5 and 8, characterized in that a pulse applied to the second controllable switch (S) for rendering said switch conducting has a leading edge which occurs simultaneously with or after the instant when the voltage across the inductive element (L) becomes zero before a turn-on instant of the power switch, but not later than the zero crossing of said voltage after the subsequent turn-off instant of the power switch (T_r), and a trailing edge which does not occur earlier than the last-mentioned zero crossing.

10. A circuit as claimed in Claim 9, characterized by a bistable element (FF) for applying the control pulse to the second controllable switch (S), the edges of a set pulse applied to the bistable element each time occurring during a zero crossing of the voltage across the inductive element (L) and the leading edge of a reset pulse also applied to the bistable element occurring at the final instant of the interruption.

11. A circuit as claimed in Claim 8, characterized by means (L_3, R_1, D_2, D_3, C_1, A) for comparing a quantity occurring in the circuit with a predetermined limit value and for activating the clamping circuit when said limit value is exceeded.

12. A circuit as claimed in Claim 1, characterized in that the means for interrupting the oscillation

comprise a second controllable switch (S) arranged in series with the capacitor (C) for interrupting the current path of the capacitor at an instant when the current therethrough is substantially zero.

13. A circuit as claimed in Claim 12, characterized in that the second controllable switch (S) is blocked at an instant when the voltage across the power switch substantially has a minimum value.

14. A circuit as claimed in Claim 1, characterized in that the control means of the power switch (T_r) drive said switch in the conducting state at an instant when the voltage thereacross substantially has a minimum value.

Patentansprüche

1. Geschaltete Speisespannungsschaltung zum Umwandeln einer Eingangsgleichspannung (V_i) in eine Ausgangsgleichspannung (V_o) mit einer zwischen die Klemmen der Eingangsspannung gekoppelten Reihenschaltung aus einem steuerbaren Leistungsschalter (T_r) und einem induktiven Element (L), mit Steuermitteln um den Leistungsschalter wechselweise in den leitenden bzw. nicht-leitenden Zustand zu bringen, mit einem mit dem induktiven Element gekoppelten Gleichrichter (D) um die Ausgangsspannung zur Verfügung zu stellen, wobei bei stromlosem Schalter und Gleichrichter das induktive Element und ein damit gekoppelter Kondensator (C) einen Teil eines Schwingkreises bilden, in dem es dann eine Spannungsschwingung gibt, und mit Mitteln (S, D_1) zum Unterbrechen der in dem Schwingkreis vorhandenen Schwingung, dadurch gekennzeichnet, daß die Mittel dazu vorgesehen sind, die Schwingung zu einem Zeitpunkt zu unterbrechen, an dem die Spannung an dem induktiven Element (L) oder der Strom durch den Kondensator (C) nahezu Null ist.

2. Schaltungsanordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Mittel zum Unterbrechen der Schwingung Synchronisiermittel sind, wobei die aufeinanderfolgenden Endzeitpunkte der Unterbrechung periodisch in der Zeit liegen.

3. Schaltungsanordnung nach Anspruch 2 zum Gebrauch in einer Bildwiedergabeanordnung, dadurch gekennzeichnet, daß die genannten Zeitpunkte mit derselben Frequenz wie ein in der Bildwiedergabeanordnung wirksames Horizontal-Ablenksignal oder mit einem Vielfachen dieser Frequenz aufeinander folgen.

4. Schaltungsanordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Mittel zum Unterbrechen der Schwingung eine Klemmschaltung bilden zum Einhalten der Spannung am dem induktiven Element (L) auf dem Wert von nahezu Null und nach einem Zeitpunkt, an dem diese Spannung nahezu Nul geworden ist.

5. Schaltungsanordnung nach Anspruch 4, dadurch gekennzeichnet, daß die Klemmschaltung ein in nur einer Richtung leitendes Element (D_1) aufweist, das mit einem zweiten Schalter (S) in Reihe liegt, wobei die gebildete Reihenschaltung zu dem induktiven Element parallel liegt.

6. Schaltungsanordnung nach Anspruch 4, dadurch gekennzeichnet, daß der Zeitpunkt, an dem die Klemmschaltung wirksam wird, kurz vor einem Einschaltzeitpunkt des Leistungsschalters liegt.

7. Schaltungsanordnung nach Anspruch 5 und 6, dadurch gekennzeichnet, daß ein dem zweiten steuerbaren Schalter (S) zugeführter Impuls um diesen Schalter in dem leitenden Zustand zu halten, eine Vorderflanke hat, die gleichzeitig mit oder nach dem Zeitpunkt auftritt, an dem die Spannung an dem induktiven Element (L) Null wird nach einem Abschaltzeitpunkt des Leistungsschalters (T_r), aber nicht später als der Nulldurchgang der genannten Spannung vor dem nachfolgenden Einschaltzeitpunkt des Leistungsschalters, und eine Rückflanke, die nicht früher als der letztgenannte Nulldurchgang auftritt.

8. Schaltungsanordnung nach Anspruch 4, dadurch gekennzeichnet, daß der Zeitpunkt, an dem die Klemmschaltung wirksam wird kurz hinter einem Abschaltzeitpunkt des Leistungsschalters (T_r) liegt.

9. Schaltungsanordnung nach Anspruch 5 und 8, dadurch gekennzeichnet, daß ein dem zweiten steuerbaren Schalter (S) zugeführte Impuls um diesen Schalter in dem leitenden Zustand zu halten eine Vorderflanke hat, die gleichzeitig mit oder nach dem Zeitpunkt auftritt, an dem die Spannung am induktiven Element (L) Null wird vor einem Einschaltzeitpunkt des Leistungsschalters, aber nicht später als der Nulldurchgang der genannten Spannung nach dem nachfolgenden Abschaltzeitpunkt des Leistungsschalters, und eine Rückflanke, die nicht

früher auftritt als der letztgenannte Nulldurchgang.

Schaltungsanordnung nach Anspruch 9, dadurch gekennzeichnet, daß ein bistabiles Element (FF) vorgesehen ist zum Zuführen des Steuerimpulses zu dem zweiten steuerbaren Schalter (S), wobei die Flanken eines dem bistabilen Element zugeführten Stellimpulses jeweils während eines Nulldurchgangs der Spannung am induktiven Element (L) auftreten und wobei die Vorderflanke eines dem bistabilen Element ebenfalls zugeführten Rückstellimpulses zu dem Endzeitpunkt der Unterbrechung auftritt.

11. Schaltungsanordnung nach Anspruch 8, dadurch gekennzeichnet, daß Mittel (L_3, R_1, D_2, D_3, C_1, A) vorgesehen sind zum Vergleichen einer in der Schaltungsanordnung auftretenden Größe mit einem vorbestimmten Grenzwert und zum Aktivieren der Klemmschaltung, wenn der genannte Grenzwert überschritten wird.

12. Schaltungsanordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Mittel zum Unterbrechen der Schwingung einen mit dem Kondensator (C) in Reihe liegenden zweiten steuerbaren Schalter (S) aufweisen zum Unterbrechen des Strompfades des Kondensators zu einem Zeitpunkt, an dem der Strom durch denselben nahezu Null ist.

13. Schaltungsanordnung nach Anspruch 12, dadurch gekennzeichnet, daß der zweite steuerbare Schalter (S) zu einem Zeitpunkt gesperrt wird, an dem die Spannung an dem Leistungsschalter im wesentlichen einen Maximalwert aufweist.

14. Schaltungsanordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Steuermittel des Leistungsschalters (T_r) den genannten Schalter in den leitenden Zustand bringen, wenn die Spannung daran im wesentlichen einen Minimalwert hat.

Revendications

1. Circuit d'alimentation à découpage pour convertir une tension continue d'entrée (V_i) en une tension continue de sortie (V_o), comportant un montage série d'un commutateur de puissance commandable (T_r) et d'un élément inductif (L), montage série qui est couplé entre les bornes de tension d'entrée, des moyens de commande pour mettre le commutateur de puissance alternativement en état de conduction et en état de blocage, un redresseur (D) couplé à l'élément inductif pour rendre disponible la tension de sortie, l'élément inductif et un condensateur (C) couplé à celui-ci faisant partie, dans les intervalles de temps où le commutateur et le redresseur sont sans courant, d'un circuit résonnant dans lequel se produit alors une oscillation de tension, et des moyens (S, D_1) pour interrompre l'oscillation se produisant dans le circuit résonnant, caractérisé en ce que les moyens sont agencés pour interrompre l'oscillation à un instant où la tension aux bornes de l'élément inductif (L) ou le courant traversant le condensateur (C) sont sensiblement nuls.

2. Circuit selon la revendication 1, caractérisé en ce que les moyens pour interrompre l'oscillation sont des moyens de synchronisation, tandis que les instants finaux successifs de l'interruption sont situés périodiquement dans le temps.

3. Circuit selon la revendication 2, destiné à être utilisé dans un dispositif de reproduction d'images, caractérisé en ce que lesdits instants se succèdent à la même fréquence que celle d'un signal de déviation de ligne actif dans le dispositif de reproduction d'image, ou à un multiple de cette fréquence.

4. Circuit selon la revendication 1, caractérisé en ce que les moyens pour interrompre l'oscillation constituent un circuit de calage pour maintenir la tension aux bornes de l'élément inductif (L) sensiblement nulle à un instant où cette tension est devenue sensiblement égale à zéro ou après cet instant.

5. Circuit selon la revendication 4, caractérisé en ce que le circuit de calage comporte un élément (D_1) conducteur de courant dans un seul sens, disposé en série avec un second commutateur (S), le montage série formé étant disposé en parallèle avec l'élément inductif.

6. Circuit selon la revendication 4, caractérisé en ce que l'instant où le circuit de calage commence à être actif se situe peu de temps avant un instant de mise en conduction du commutateur de puissance.

7. Circuit selon les revendications 5 et 6, caractérisé en ce qu'une impulsion appliquée au second commutateur commandable (S) pour rendre conducteur ce commutateur présente un flanc avant qui apparaît simultanément avec ou après l'instant où la tension aux bornes de

* C L M S *

l'élément inductif (L) devient nulle après un instant de mise en état de blocage du commutateur de puissance (Tr), mais non plus tard que le passage par zéro de ladite tension avant l'instant suivant de mise en état de conduction du commutateur de puissance, et un flanc arrière qui n'apparaît pas plus tôt que le passage par zéro mentionné en dernier lieu.

8. Circuit selon la revendication 4, caractérisé en ce que l'instant où le circuit de calage commence à être actif se situe peu de temps après un instant de mise en état de blocage du commutateur de puissance (T_r).

9. Circuit selon les revendications 5 et 8, caractérisé en ce qu'une impulsion appliquée au second commutateur commandable (S) pour rendre celui-ci conducteur présente un flanc avant qui apparaît simultanément avec ou après l'instant où la tension aux bornes de l'élément inductif (L) devient nulle avant un instant de mise en conduction du commutateur de puissance, mais non plus tard que le passage par zéro de cette tension après l'instant suivant de mise en état de blocage du commutateur de puissance (T_r) et un flanc arrière qui n'apparaît pas plus tôt que le passage par zéro cité en dernier lieu.

10. Circuit selon la revendication 9, caractérisé par un élément bistable (FF) pour appliquer l'impulsion de commande au second commutateur commandable (S), les flancs d'une impulsion d'activation appliquée à l'élément bistable apparaissant chaque fois pendant un passage par zéro de la tension aux bornes de l'élément inductif (L) et le flanc avant d'une impulsion de remise à zéro, également appliquée à l'élément bistable, apparaissant à l'instant final de l'interruption.

11. Circuit selon la revendication 8, caractérisé par des moyens (L_3, R_1, D_2, D_3, C_1, A) pour comparer une quantité, apparaissant dans le circuit, avec une valeur limite prédéterminée et pour activer le circuit de calage lorsque cette valeur limite est dépassée.

12. Circuit selon la revendication 1, caractérisé en ce que les moyens pour interrompre l'oscillation comportent un second commutateur commandable (S), disposé en série avec le condensateur (C), pour interrompre le trajet de courant du condensateur à un instant où le courant à travers celui-ci est sensiblement égal à zéro.

13. Circuit selon la revendication 12, caractérisé en ce que le second commutateur commandable (S) est bloqué à un instant où la tension aux bornes du commutateur de puissance a sensiblement une valeur minimale.

14. Circuit selon la revendication 1, caractérisé en ce que les moyens de commande du commutateur de puissance (T_r) mettent ledit commutateur en état de conduction à un instant où la tension aux bornes de celui-ci a sensiblement une valeur minimale.