

METHOD AND APPARATUS FOR QUICKLY INITIATING MEMORY
ACCESSES IN A MULTIPROCESSOR CACHE COHERENT
ABSTRACT OF THE DISCLOSURE

In a computer system including a packet-switched bus, a method for requesting transactions such that memory accesses are initiated quickly. A master transmits a first portion of a transaction request packet having multiple portion. A memory controller receives the first portion of the transaction request, which includes a row address portion of a memory address. The memory controller initiates a memory access by applying a row address strobe signal to the row of the memory location in response to receiving the first portion of the request packet, and the master transmits any remaining portion of the transaction request. After the full memory address has been received, it is determined whether data stored at the memory location is to be read from a source other than the memory location. The memory controller aborts the memory access by inhibiting assertion of a column access strobe signal to the memory location if the data is to be read from a source other than the memory location.

(FIGURE 1)