CLAIMS

[CLAIM 1]

A method comprising:

forming a semiconductor structure having a semiconductor device, the forming comprising:

forming a channel layer, the channel layer comprising a Group III-V material;

forming a barrier layer on the channel layer, the barrier layer comprising a Group III-V material,

forming a vertically recessed source region and a vertically recessed drain region, the vertically recessed source region and the vertically recessed drain region passing through the barrier layer and into the channel layer;

growing a doped Group III-V layer in the vertically recessed source region and the vertically recessed drain region, the grown doped Group III-V layer comprising the same material as the channel layer, the doped Group III-V layer extending over a side of the vertically recessed source region and an opposing side of the vertically recessed drain region and extending continuously over the Group III-V barrier layer from the side of the vertically recessed source region to the opposing side of the vertically recessed drain region;

removing a portion of the grown doped Group III-V layer to expose a gate region over a surface of the barrier layer; and

forming a gate for the semiconductor device over the exposed gate region.

[CLAIM 2]

The method of claim 1, wherein the semiconductor device is formed in a device region and wherein a portion of the grown doped Group III-V layer is outside of the device region.

[CLAIM 3]

The method of claim 1, further comprising forming a dielectric structure over the grown doped Group III-V layer and over the gate.

[CLAIM 4]

The method of claim 1, wherein the semiconductor device is formed in a device region, and

wherein a portion of the doped Group III-V layer on the barrier layer outside of the device region is single crystal material.

[CLAIM 5]

The method of claim 1, wherein the semiconductor device is formed in a device region, and

wherein the grown doped Group III-V layer in direct contact with a passivation layer disposed over the Group III-V material of the barrier layer of the semiconductor device and the Group III-V material in a region outside of the device region is polycrystal while the Group III-V material in contact with the vertically recessed source region and the vertically recessed drain region is single crystal.

[CLAIM 6]

The method of claim 1, wherein the doped Group III-V layer in contact with the vertically recessed source region and the vertically recessed drain region and the barrier layer is single crystal material.

[CLAIM 7]

The method of claim 1, wherein the semiconductor device is formed in a device region, and

wherein the doped Group III-V layer outside of the device region is polycrystalline material.

[CLAIM 8]

The method of claim 1, wherein the channel layer and the grown doped Group III-V layer are single crystal material.

[CLAIM 9]

The method of claim 1, wherein the channel layer and the doped Group III-V layer comprise GaN.

[CLAIM 10]

The method of claim 1, wherein the barrier layer comprises $Al_xGa_{1-x}N$ here x is between 0 and 1.

[CLAIM 11]

The method of claim 1, wherein the gate region is etched selectively through the doped Group III-V layer to stop on the Group III-V barrier layer.

[CLAIM 12]

The method of claim 1, wherein the gate region is etched selectively through the doped Group III-V layer to stop on the barrier layer comprising $Sc_yAl_{1-y}N$ where y is between 0 and 0.5.

[CLAIM 13]

The method of claim 1, wherein the semiconductor device is formed in a device region,

wherein a portion of the grown doped Group III-V layer in a region outside of the device region is monitored by measuring instrumentation during the growth of the grown doped Group III-V layer, and

wherein the doped Group III-V layer is grown as single crystal material in the region outside the device region.

[CLAIM 14]

The method of claim 13, further comprising forming a dielectric structure over the grown doped Group III-V layer and over the gate, and

wherein the dielectric structure provides a passivation layer.

[CLAIM 15]

The method of claim 1, wherein the semiconductor device has an extrinsic drain region and wherein the doped Group III-V layer extends into the extrinsic drain region of the semiconductor device.

[CLAIM 16]

A method comprising:

forming a semiconductor structure having a semiconductor device, disposed in a device region, the forming comprising:

forming a channel layer, the channel layer comprising a Group III-V material;

forming a barrier layer on the channel layer, the barrier layer comprising a Group III-V material;

forming a dielectric layer on the barrier layer, the dielectric layer exposing a source region and a drain region of the semiconductor device;

etching a vertically recessed source region and a vertically recessed drain regions in the exposed source region and the exposed drain region, the vertically recessed source region and the vertically recessed drain region passing through the barrier layer and into the channel layer;

growing a doped Group III-V layer in the vertically recessed source region and the vertically recessed drain region and over the dielectric layer, the grown doped Group III-V layer comprising the same material as the channel layer, the doped Group III-V layer extending over a side of the vertically recessed source region and an opposing side of the vertically recessed drain region and extending

continuously over the dielectric layer from the side of the vertically recessed source region to the opposing side of the vertically recessed drain region and outside the device region;

removing a portion of the doped Group III-V layer over the barrier layer;

forming an opening in the dielectric layer to expose a gate region over a surface of the barrier layer; and

forming a gate for the semiconductor device in the opening.