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TITLE: METHOD AND APPARATUS FOR REDUCING PARASITIC BIPOLAR CURRENT IN A SILICON-ON-INSULATOR TRANSISTOR

Field of the Invention

The present invention relates to silicon-on-insulator field effect transistors, and more particularly to reduction of parasitic bipolar current in such FET's.

Background of Invention

Silicon-on-insulator ("SOI") field effect transistors ("FET's"), particularly wide SOI FET's in pass gate applications, suffer a parasitic bipolar current, the effects of which are most severe when the circuit is initially turned on after being idle for a long period of time, i.e. a time in the range of milliseconds. This is because the floating body of the SOI FET can develop a body charge over time. The amount of such body charge will depend on the

potentials at the source, drain, and gate terminal electrodes of the SOI FET. The maximum amount of charging occurs when the gate is completely turned off and both the source and drain electrode are biased at the highest potential vdd. During the subsequent switching of the source or drain electrode of the SOI FET, the accumulated body charge will be discharged by means of a transient bipolar current. This parasitic current degrades performance, including noise and timing performance. See, for example, C. Chuang, P.Lu, and C. Anderson, SOI for Digital CMOS VLSI: Design Considerations and Advances, Proceedings of the IEEE, v. 86, No. 4, April 1998, p. 689 - 720, which is hereby incorporated by reference (discussing the nature of and occasion for the parasitic current in connection with the description therein of figures 1 and 2), and C. Hsieh et al., Methods to Enhance SOI SRAM Cell Stability, U.S. Patent No. 5,774,411, which is hereby incorporated by reference (discussing, in the Background of the Invention section, the parasitic, lateral, bipolar transistor formed by the source, drain and channel, i.e., floating body, region of an FET). Pass gates are particularly susceptible to parasitic bipolar current because it is not uncommon in pass gate applications for both the source and drain of a pass gate to be driven to a relatively high voltage level, and because it is not uncommon for pass gates

to be relatively wide.

A number of circuit structures are known for mitigating this problem in a variety of contexts. For example, for a number of applications, including pass gates, it is known to connect the SOI NFET body to the NFET gate. Id. at p. 706. This has the beneficial effect of minimizing Vt loss (aka "dynamic Vt control"), improving drive, and suppressing leakage, but is disadvantageous from the standpoint of area increase and incompatibility with bulk design.

It is also known to actively bias the body of SOI NFET and PFET devices in an inverting output stage of a driver. Id. at 709 (showing a network of FET's responsive to the input to and output from the SOI output stage). Such an arrangement also has the beneficial effect of minimizing Vt loss, improving drive, and suppressing leakage, but has disadvantages of more expensive fabrication process, significantly larger area for the extra diode and capacitor, and increasing input capacitance (which slows down the circuit). It is also known to discharge the body of a SOI FET responsive to a signal timed to occur shortly before the gate of the FET is selected (hereinafter, a "pre-discharge signal"), or responsive to the accumulated charge on the body. This discharging has the possible benefit of reducing parasitic bipolar current during functional, initial cycle switching, provided that the

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discharging is early enough or that the discharge device is large enough with respect to the charge on the body to sufficiently discharge the body during the discharging interval before the gate is selected. In addition to these limitations, it also disadvantageously requires that a timing signal be generated for the pre-discharge signal.

Therefore, although there are known circuits and techniques for mitigating parasitic, bipolar current in an insulated body FET, because of the disadvantages described above, and others, a need remains for improved methods and structures for mitigating such parasitic, bipolar current.

Summary of the Invention

In a first form, an apparatus for reducing parasitic bipolar current in a field effect transistor ("FET") includes an insulated body NFET, having a body disposed, at least in part, below a gate electrode of the insulated body NFET Body-charge control circuitry is coupled to the gate of the NFET and to the body. The body-charge control circuitry includes a body-charge control FET, with first and second conducting electrodes and a gate electrode, has its first

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conducting electrode electrically coupled to the body of the insulated body NFET and its second conducting electrode electrically coupled to an electrical sink. The body-charge control circuitry also includes an inverter, having its input electrically coupled to the insulated body NFET gate, and its output electrically coupled to the body-charge control NFET gate, so that when a voltage applied to the insulated body NFET gate is above a certain first voltage level, the inverter output voltage tends to turn off the body-charge control FET and electrically isolate the body from the sink, thereby permitting a charge to accumulate on the body. Conversely, when the voltage applied to the insulated body NFET gate electrode is below a certain second voltage level, the inverter output voltage tends to turn on the body-charge control FET and electrically couple the body to the sink, thereby discharging at least a portion of any charge accumulated on the body.

In an additional aspect, the apparatus includes a SOI PFET. If the SOI PFET is susceptible to parasitic bipolar current the apparatus includes a second body-charge control circuitry, for the PFET. The second body-charge control circuitry isolates the PFET body when the PFET is on, and discharges the body when the PFET is off.

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(Note that in the case of an insulated body PFET, the term "discharge" is herein used differently than in the case of an insulated body NFET. For the PFET, negative charge may accumulate on the insulated body when the body is isolated; whereas for the NFET positive charge may accumulate when the NFET body is isolated. Therefore, for the PFET, negative charge is discharged. But for the NFET, positive charge is discharged.)

In another form, a method includes steps for reducing parasitic bipolar current in a NFET having an insulated body, the body being disposed, at least in part, below a gate electrode of the NFET. In one step, the body of the insulated body NFET is electrically isolated, responsive to a voltage applied to the insulated body NFET gate electrode being above a certain first voltage level. This permits a charge to accumulate on the body, lowering the threshold voltage for the insulated body NFET.

In another step, at least a portion of the charge on the body of the insulated body NFET is electrically discharged, responsive to the voltage applied to the insulated body NFET gate electrode being below a certain second voltage level. This discharging reduces parasitic bipolar current which would otherwise occur upon turning the NFET back on if the body had charged up during the time when the NFET was off.

In another aspect, the discharging includes electrically coupling the insulated NFET

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body to a sink having a voltage lower than a voltage level of the accumulated charge. Furthermore, the SOI FET body is thus coupled to the sink whenever the SOI FET gate electrode voltage is below the certain second voltage level.

In another form, a method includes steps for reducing parasitic bipolar current in a PFET having an insulated body, the body being disposed, at least in part, below a gate electrode of the PFET. The body of the insulated body PFET is discharged, responsive to a voltage applied to the insulated body PFET gate electrode being above a certain first voltage level. Also, the body of the insulated body PFET is electrically isolated, responsive to the voltage applied to the insulated body PFET gate electrode being below a certain second voltage level. The discharging of the PFET body while the PFET is off reduces parasitic bipolar current which could otherwise occur upon turning the PFET back on if certain conditions occurred during the time when the PFET was off.

While the invention has been shown and described with reference to particular embodiments thereof, it will be understood by those skilled in the art

that the foregoing and other changes in form and detail may be made therein without departing from the spirit and scope of the invention.

Brief Description of the Drawings

FIG. 1 is a cross section of an SOI NFET.

FIG. 2 is a schematic of an embodiment of the present invention, having a single, controlled NFET, and circuitry for controlling discharge of the NFET body.

FIG. 2a is a schematic of an embodiment of the present invention, having a single controlled PFET, and circuitry for controlling discharge of the PFET body.

FIG's 3 through 5 are voltage responses for a number of different circuit configurations.

FIG. 6 is a schematic for a dual gate embodiment of the present invention.

FIG. 7 is a schematic for a different dual gate embodiment of the present invention.

Detailed Description

Referring to FIG. 1, a cross section of an SOI CMOS NFET is shown. The SOI NFET has a body contact (not shown in FIG.1). Numerous methods and structures are known for forming such a body contact for CMOS FET's. See, for example, Beyer, et al., Method of Forming a SOI Transistor Having a Self-Aligned Body Contact, U.S. Pat. No. 5,405,795; and Beyer, et al., SOI Transistor Having a Self-Aligned Body Contact, U.S. Pat. No. 5,729,039, which are hereby incorporated by reference.

Referring now to FIG. 2, SOI NFET 210 has its source electrode connected to circuit element 220 at node "net1" and its drain connected to circuit element 230 at node "net2". Circuit elements 220 and 230 represent other circuitry, such as other FET's, resistors, termination's, etc. For example, the FET 210 could be a pass gate, or it could be a logic device in one leg of a NOR circuit, or in one branch of a multiplexer circuit. The FET 210 could be for shorting a pin in circuitry 220 to a pin in circuitry 230, when it is active.

The CMOS NFET 210 body is connected at node 240 to the drain electrode of CMOS NFET 250. The NFET 250 has its source grounded. Its gate is connected to CMOS inverter 260 output. The input to inverter 260 is connected to the gate of NFET 210, which is also connected to a "select" line, on which a voltage is impressed to control the gate 210. When the "Select" voltage, applied to the gate of NFET 210 and the input of inverter 260, goes high, this tends to drive the inverter 260 output low. The inverter output going low

tends to turn off NFET 250. With body-charge control NFET 250 thus tending to be off, this tends to isolate the body of NFET 210, allowing it to accumulate charge and thereby lowering the FET 210 threshold voltage.

When the voltage impressed on the select line goes low, the NFET 210 is deselected, and the output of inverter 260 goes high, tending to turn on NFET 250. With body-charge control NFET 250 tending to be on this tends to ground the body of SOI NFET 210. This body-charge control of the NFET 210 body prevents a buildup of charge on the body which could otherwise occur if the voltage were high on the source and drain of NFET 210. The lack of charge buildup tends to prevent initial cycle parasitic current that would otherwise occur upon applying a high signal to the select line of the NFET 210 if a charge had built up on the body.

Thus, the embodiment described provides the beneficial effect of lowering threshold voltage in a floating body SOI FET during activation, and transition to activation of NFET 210, while also achieving the benefit of no charge buildup in a grounded body FET during deactivation, and transition between deactivation and activation. Furthermore, these benefits are achieved with a relatively small number of elements, e.g., inverter 260 and NFET 250. Still further, the benefits are achieved with the inverter 260 and NFET 250 being responsive solely to voltage applied to the NFET 210 gate, that is, without circuitry for

generating a pre-discharge signal timed to occur in advance of activating the NFET 210 gate.

In a still further advantage, since the body of FET 210 is discharged throughout substantially the entire interval when the gate of FET 210 is deselected, the discharging is not limited to occurring solely during a relatively shorter pre-discharge interval timed immediately before the gate is selected. Thus, the invention is advantageous in that it is relatively insensitive to the fabrication quality of the body contact. Similarly, the discharge (aka body-charge control) FET 250 may be relatively smaller than would be required for a short discharge interval. For example, it has been empirically determined that the FET's of the inverter 260 and the body-charge control FET 250 may each be 1/10 the size of the insulated body FET 210.

Referring now to FIG. 2A, another embodiment is shown for an insulated body FET 270, where the FET is a p-type FET. Control circuitry is coupled to the body and the gate of the insulated body PFET, for controlling charge on the body responsive to a voltage applied to the gate electrode. The control circuitry includes a body-charge control PFET 280. The PFET

280 first conducting electrode is electrically coupled to the body of the insulated body PFET 270. The body-charge control PFET 280 second conducting electrode is electrically coupled to an electrical source.

The control circuitry also includes an inverter 260. The inverter input is electrically coupled to the body-charge control PFET 280 gate electrode. The inverter output is electrically coupled to the insulated body PFET 270 gate electrode, so that when the voltage applied to the charge-control PFET 280 gate electrode is above a high voltage level, this tends to turn off the body-charge control PFET 280 and electrically isolate the body of the PFET 270 from the source, thereby permitting a charge to accumulate on the body. When the voltage applied to the body-charge control PFET 280 gate electrode is below a low voltage level, this tends to turn on the body-charge control PFET 280 and electrically couple the body to the source, thereby discharging at least a portion of any charge accumulated on the body.

Results of simulations are shown in FIG's 3-5.

In FIG. 3, the voltage for the curve shown as "controlled body passgate" is measured from net1 to ground for the circuit of FIG. 2. For the curve labeled "plain passgate," the voltage shown is net1 to ground for a circuit such as FIG. 2, but wherein the inverter 260 and body-charge control FET 250 are omitted, and the body of FET 210 is floating. For both curves, the FET 210 is not selected, and the falling voltage at net1 is caused by switching internal to circuit block 220. Also in both cases, it is assumed that both net1 and net2 were high for some time before the switching, thereby aggravating the parasitic current of FET 210. The comparison indicates improved switching speed for the controlled body passgate. That is, the plain passgate switching is degraded by parasitic bipolar current

In FIG. 4, the voltage for the curve shown as "controlled body passgate" is measured from net2 to ground for the circuit of FIG. 2. For the curve labeled "passgate with body grounded," the voltage shown is net2 to ground for a circuit such as FIG. 2, but wherein the inverter 260 and body-charge control FET 250 are omitted, and the body of FET 210 is directly grounded. For both curves, the falling voltage at net2 is caused by switching FET 210. A high-to low transition propagates from net1 to net2. Also in both cases, it is assumed that both net1 and net2 were high for some time before the switching, thereby aggravating the parasitic current of FET 210. The comparison indicates the controlled body passgate provides somewhat faster switching with no degradation in overshoot.

In FIG. 5, the voltage for the curve shown as "controlled body passgate" is measured from net2 to ground for the circuit of FIG. 2. For the curve labeled "passgate with body floating," the voltage shown is net2 to ground for a circuit such as FIG. 2, but wherein the inverter 260 and body-charge control FET 250 are omitted, and the body of FET 210 is floating. For both curves, the falling voltage at net2 is caused by switching FET 210. Also in both cases, it is assumed that both net1 and net2 were high for some time before the switching, thereby aggravating the parasitic current of FET 210. The comparison indicates comparable switching speed, and an improvement in overshoot for the controlled body passgate.

FIG. 6 shows a PFET/NFET pair of passgates 610 and 670, with body-charge control circuitry, similar to the single passgate/body control circuitry of FIG. 2. In conventional applications of a PFET/NFET passgate pair, an inverter is provided for select control of the gate of the PFET. This inverter (inverter 660 in FIG. 6) conventionally provided for the PFET gate select control can be used for body-charge control circuitry as well, so that in comparison with conventional dual passgate/passgate control circuitry, the body-charge control circuitry requires only adding a body-charge control FET 650 and 680 for each of the respective passgate FET's 610 and 670.

FIG. 7 shows a PFET/NFET pair of passgates 710 and 770, with body-charge

control circuitry, similar to the dual passgate/body control circuitry of FIG. 6. The FIG. 7 embodiment is for an instance wherein the PFET passgate 770 is fabricated in a manner so as to reduce the PFET's susceptibility to parasitic bipolar current. In such an instance the body-charge control FET 680 of FIG. 6 may be omitted. Just as previously stated, note that in conventional applications of a PFET/NFET passgate pair, an inverter is provided for select control of the gate of the PFET. This inverter (inverter 760 in FIG. 7) conventionally provided for the PFET gate select control can be used for body-charge control circuitry as well, so that in comparison with conventional dual passgate/passgate control circuitry, the body-charge control circuitry of FIG. 7 requires only adding a body-charge control FET 750 for the passgate FET 710.

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Claims

What is claimed is:

1. An apparatus for reducing parasitic bipolar current in a field effect transistor ("FET"), comprising:

an insulated body FET, having a body disposed, at least in part, near a gate electrode of the insulated body FET;

control circuitry coupled to the body and the gate of the insulated body FET, for controlling charge on the body responsive to a voltage applied to the gate electrode.

2. The apparatus of claim 1, wherein the control circuitry comprises:

a body-charge control FET, having first and second conducting electrodes and a gate electrode, wherein the body-charge control FET first conducting electrode is electrically coupled to the body of the insulated body FET and the body-charge control FET second conducting electrode is electrically coupled to an electrical sink; and

an inverter having an inverter input electrically coupled to the insulated body FET gate electrode, and an inverter output electrically coupled to the body-charge control FET gate electrode, so that the voltage applied to the insulated body FET gate electrode being

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above a certain first voltage level tends to drive the inverter output voltage low, turn off the body-charge control FET and electrically isolate the body from the sink, thereby permitting a charge to accumulate on the body, and the voltage applied to the insulated body FET gate electrode being below a certain second voltage level tends to drive the inverter output voltage high, turn on the body-charge control FET and electrically couple the body to the sink, thereby discharging at least a portion of any charge accumulated on the body,

3. The apparatus of claim 2, wherein the insulated body FET couples first circuitry to second circuitry.

4. The apparatus of claim 3, wherein the insulated body FET is a logic device in one leg of a logic circuit.

5. The apparatus of claim 3, wherein the insulated body FET is a logic device in one branch of a multiplexer circuit.

6. The apparatus of claim 2, wherein the insulated body FET is an NFET, the apparatus comprising:

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a second insulated body FET, having a body disposed, at least in part, near a gate electrode of the second insulated body FET, wherein the second insulated body FET is a PFET; and

second control circuitry coupled to the body of the second insulated body FET, for controlling charge thereon responsive to a voltage applied to the gate electrode of the second insulated body FET.

7. The apparatus of claim 6, wherein the second control circuitry comprises a second body-charge control FET, the second body-charge control FET being a PFET having first and second conducting electrodes and a gate electrode, wherein the second body-charge control FET first conducting electrode is electrically coupled to the body of the second insulated body FET, the second body-charge control FET second conducting electrode is electrically coupled to an electrical source, and the second body-charge control FET gate electrode is coupled to the gate electrode of the first insulated body FET, so that the voltage applied to the second insulated body FET gate electrode being above a certain first voltage level tends to

turn on the second body-charge control FET and electrically couple the second insulated body FET body to the source, thereby tending to discharge the body, and the voltage applied to the second insulated body FET gate electrode being below a certain second voltage level tends to turn off the second body-charge control FET and electrically isolate the second

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insulated body FET body from the source, thereby permitting a charge to accumulate on the body.

8. A method for reducing parasitic bipolar current in an n-type, field effect transistor ("NFET") having an insulated body, the body being disposed, at least in part, near a gate electrode of the NFET, comprising the steps of:

a) electrically isolating the body of the insulated body NFET, responsive to a voltage applied to the insulated body NFET gate electrode being above a certain first voltage level, thereby permitting a charge to accumulate on the body; and

b) discharging at least a portion of any charge on the body of the insulated body NFET, responsive to the voltage applied to the insulated body NFET gate electrode being below a certain second voltage level.

9. The method of claim 8, wherein step b) comprises electrically coupling the insulated body NFET body to a sink, the sink having a voltage lower than a voltage level of the accumulated charge, wherein the insulated body NFET body is thus coupled to the sink whenever the insulated body NFET gate electrode voltage is below the certain second voltage level.

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10. A method for reducing parasitic bipolar current in a p-type, field effect transistor ("PFET") having an insulated body, the body being disposed, at least in part, near a gate electrode of the PFET, comprising the steps of:

a) discharging the body of the insulated body NFET, responsive to a voltage applied to the insulated body PFET gate electrode being above a certain first voltage level; and

b) electrically isolating the body of the insulated body PFET, responsive to the voltage applied to the insulated body PFET gate electrode being below a certain second voltage level.

11. The method of claim 10, wherein step a) comprises electrically coupling the insulated body PFET body to a voltage source whenever the insulated body PFET gate electrode voltage is above the certain first voltage level

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12. An apparatus for reducing parasitic bipolar current in a field effect transistor ("FET"), comprising:

an insulated body FET, the FET being a p-type FET having a body disposed, at least in part, near a gate electrode of the insulated body PFET;

control circuitry coupled to the body and the gate of the insulated body PFET, for controlling charge on the body responsive to a voltage applied to the gate electrode, wherein the control circuitry comprises:

a body-charge control PFET, having first and second conducting electrodes and a gate electrode, wherein the body-charge control PFET first conducting electrode is electrically coupled to the body of the insulated body PFET and the body-charge control PFET second conducting electrode is electrically coupled to an electrical source; and

an inverter having an inverter input electrically coupled to the body-charge control PFET gate electrode, and an inverter output

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electrically coupled to the insulated body PFET gate electrode, so that the voltage applied to the charge-control PFET gate electrode being above a certain first voltage level tends to turn off the body-charge control PFET and electrically isolate the body from the source, thereby permitting a charge to accumulate on the body, and the voltage applied to the body-charge control PFET gate electrode being below a certain second voltage level tends to turn on the body-charge control PFET and electrically couple the body to the source, thereby discharging at least a portion of any charge accumulated on the body.

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