

CLAIMS

1. An encoder for encoding input data utilizing a binary symmetry-invariant product code including D data bits and P parity bits in each dimension, the encoder comprising circuitry including:
 - a half-size data array including D rows each having storage for H bits of input data, wherein D is an integer equal to $2 \times H + 1$, and wherein the encoder is configured to access bits of each row of the binary symmetry-invariant product code by reading a first H-bit data word from a selected one of the D rows of the half-size data array and a second H-bit data word across H different rows of the half-size data array;
 - a register configured to receive the bits of each row of the binary symmetry-invariant product code and to rotate the bits as needed to obtain the rows of the binary symmetry-invariant product code;
 - a row parity generator coupled to the register and configured to generate row parity for each row of the binary symmetry-invariant product code; and
 - a column parity generator configured to generate, based on row parity generated by the row parity generator, column parities for the P parity bits of all rows of the binary symmetry-invariant product code.
2. The encoder of Claim 1, wherein the binary symmetry-invariant product code is a half product code (HPC).
3. The encoder of Claim 1, wherein the half-size data array comprises a plurality of shift registers.
4. The encoder of Claim 1, wherein the encoder is configured to shift bits between rows of the half-size data array and to recirculate the first H-bit data word read from the half-size data array back into the half-size data array.
5. The encoder of Claim 4, wherein the encoder forms all rows of the binary symmetry-invariant product code by reading a same set of bit storage locations within the half-size data array.
6. The encoder of Claim 1, wherein the encoder is configured to pack the half-size data array with H bits of input data at a time.
7. The encoder of Claim 1, wherein the encoder is configured to output D sets of encoded data each including H data bits and P parity bits.
8. The encoder of Claim 7, wherein the encoder is further configured to output $P \times (P-1)/2$ cross-parity bits.
9. A data storage system, comprising:
 - a non-volatile memory system; and
 - a controller coupled to a non-volatile memory system, wherein the controller includes the encoder of any of Claims 1 to 8.

10. A data communication system, comprising:
 - the encoder of any of Claims 1 to 8; and
 - a modulator configured to receive encoded data from the encoder, modulate the encoded data, and output the modulated encoded data on a communication channel.
11. A method of encoding a binary symmetry-invariant product code including D data bits and P parity bits in each dimension, the method comprising:
 - packing input data in a half-size data array including D rows each having storage for H bits of input data, wherein D is an integer equal to $2 \times H + 1$;
 - iteratively accessing bits of each row of the binary symmetry-invariant product code by reading a first H-bit data word from a selected one of the D rows of the half-size data array and a second H-bit data word across H different rows of the half-size data array;
 - rotating the bits of each row of the binary symmetry-invariant product code as needed to obtain the rows of the binary symmetry-invariant product code;
 - generating row parity for each row of the binary symmetry-invariant product code and generating, based on row parity generated by the row parity generator, column parities for the P parity bits of all rows of the binary symmetry-invariant product code; and
 - outputting the first H-bit data words, row parities, and column parities.
12. The method of Claim 11, wherein the binary symmetry-invariant product code is a half product code (HPC).
13. The method of Claim 11, wherein packing the half-size data array comprises packing a plurality of shift registers.
14. The method of Claim 11, and further comprising:
 - shifting bits between rows of the half-size data array; and
 - recirculating the first H-bit data word accessed from the half-size data array back into the half-size data array.
15. The method of Claim 14, wherein the accessing includes forming all rows of the binary symmetry-invariant product code by reading a same set of bit storage locations within the half-size data array.
16. The method of Claim 11, wherein the packing includes packing the half-size data array with H bits of input data at a time.

17. The method of Claim 11, wherein outputting the column parities includes outputting $P \times (P-1)/2$ cross-parity bits.
18. The method of Claim 11, and further comprising storing the first H-bit data words, row parities, and column parities in a non-volatile memory system.
19. The method of Claim 11 and further comprising:
modulating encoded data including the first H-bit data words, row parities, and column parities and
transmitting the modulated encoded data on a communication channel.
20. A computer program comprising program code means adapted to perform the method of any of claims 11 to 19 when said program is run on a computer.