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Figure 1: Cross-sectional view of a portion of an Integrated Circuit

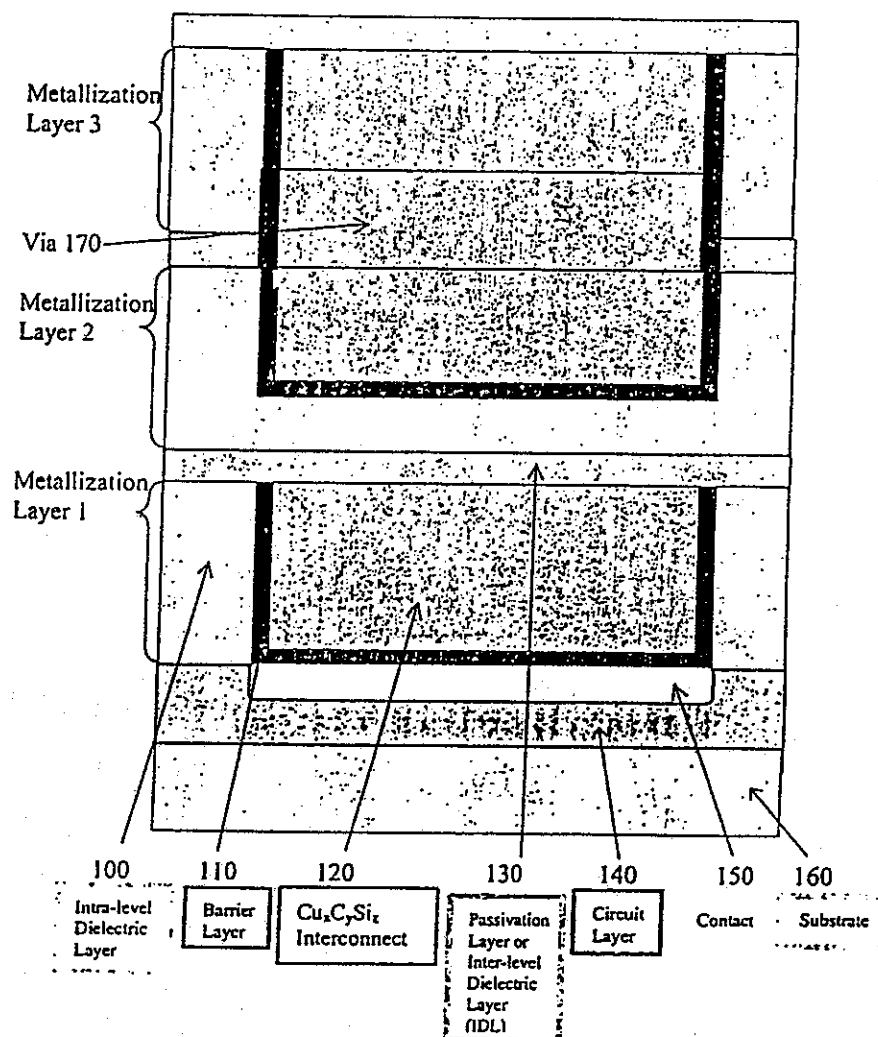
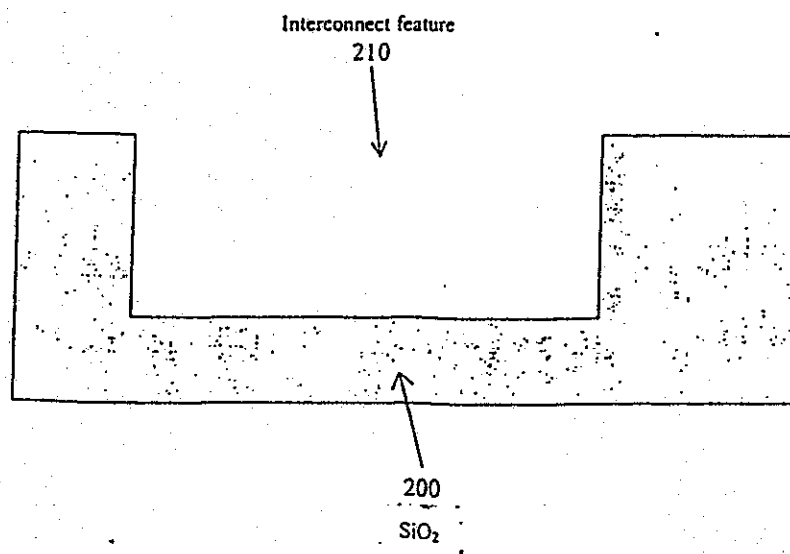


Figure 2: Pattern e.g. Damascene Trenches



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Figure 3: Deposit barrier (e.g. TaN) and seed (e.g. Cu) into interconnect feature followed by electroplated carbon doped copper (e.g. Cu_xC_y)

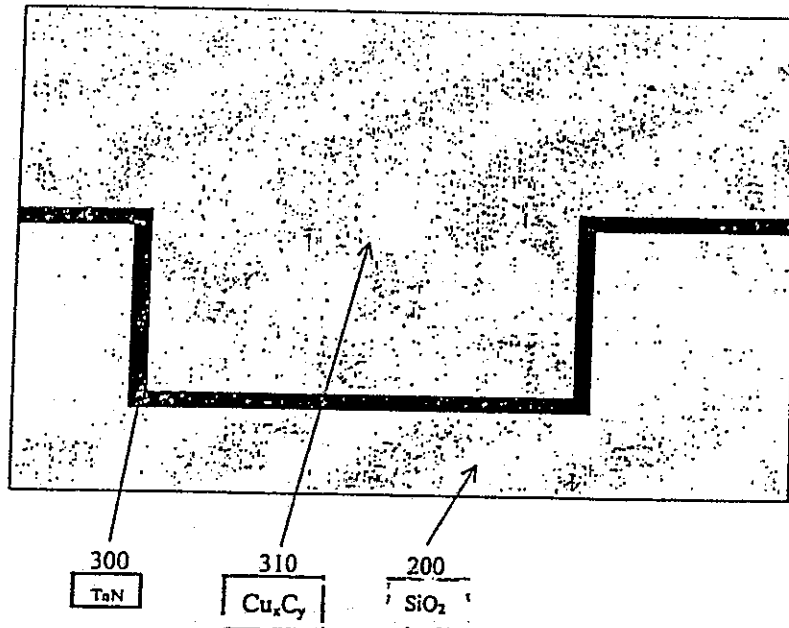
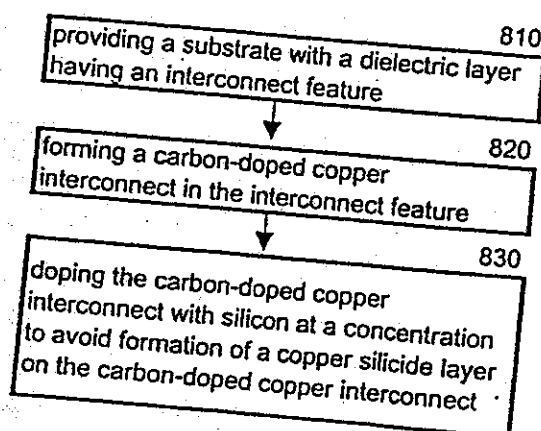


Figure 8



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Figure 4: Excess carbon doped copper (e.g. Cu_xC_y) is polished off the wafer surface

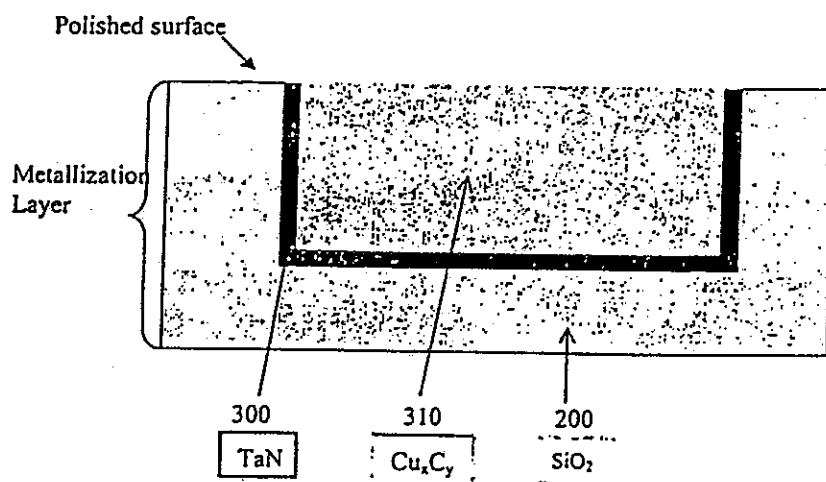


Figure 5: Cu_xC_y surface is cleaned with a plasma (e.g. NH_3) then exposed to silane before depositing silicon nitride

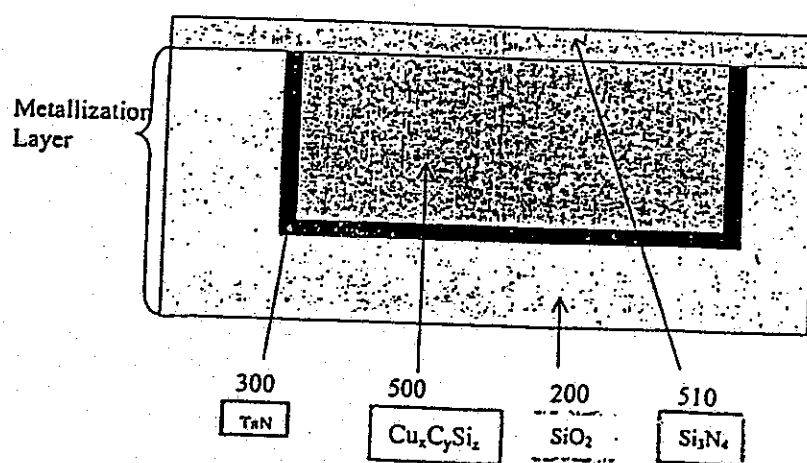
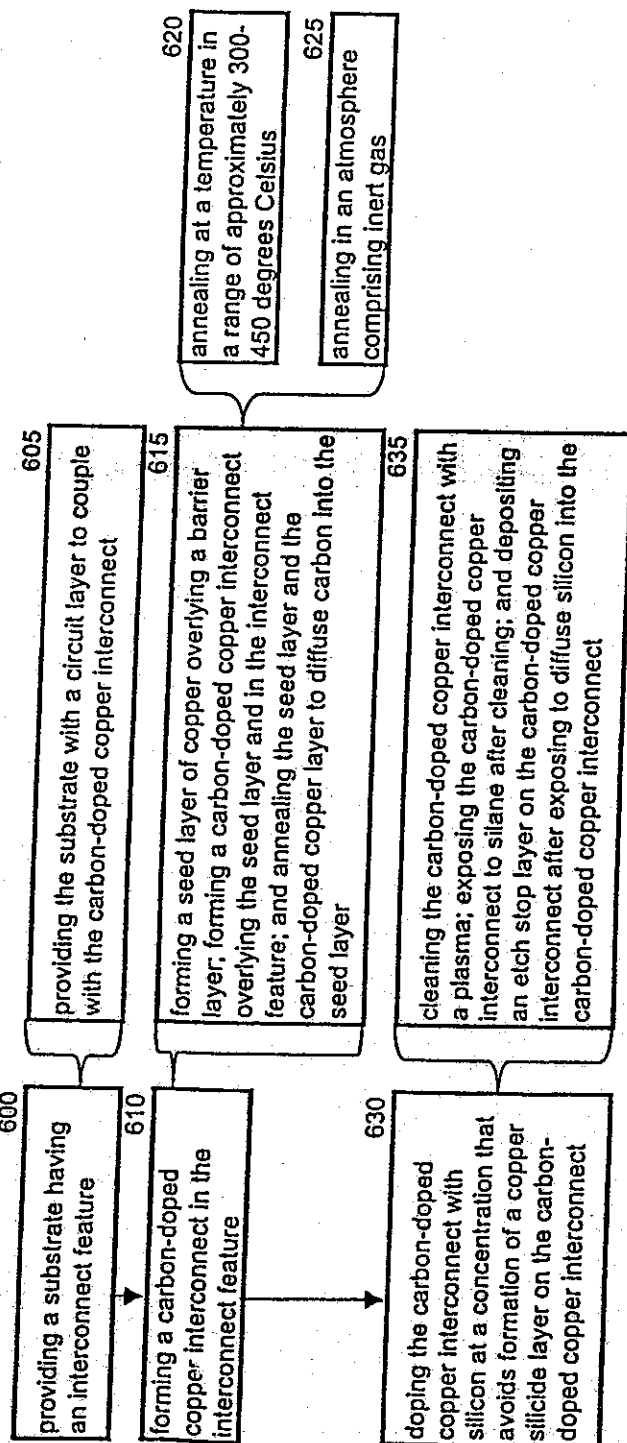


Figure 6



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Figure 7

