DESCRIPTION

CAPACITORLESS ONE TRANSISTOR DRAM CELL, INTEGRATED CIRCUITRY COMPRISING AN ARRAY OF CAPACITORLESS ONE TRANSISTOR DRAM CELLS, AND METHODS OF FORMING LINES OF CAPACITORLESS ONE TRANSISTOR DRAM CELLS

TECHNICAL FIELD

This invention relates to capacitorless one transistor DRAM cells, to integrated circuitry comprising an array of capacitorless one transistor DRAM cells, and to methods of forming lines of capacitorless one transistor DRAM cells.

BACKGROUND ART

Semiconductor memories, such as dynamic random access memory (DRAMs), are widely used in computer systems for storing data. A DRAM cell typically includes an access field effect transistor (FET) and a storage capacitor. The access FET allows the transfer of data charges to and from the storage capacitor during reading and writing operations. Data charges on the storage capacitor are periodically refreshed during a refresh operation.

Capacitorless one transistor DRAM cells have also been developed. One type of such cell utilizes a floating body effect of a semiconductor-on-insulator transistor, for example as disclosed in U.S. Patent No. 6,969,662. Such memory cell might comprise a partially depleted or a fully depleted silicon-on-insulator transistor (or transistor formed in bulk substrate material) having a channel which is disposed adjacent to the body and separated therefrom by a gate dielectric. The body region of the transistor is electrically floating in view of insulation or a non-conductive region disposed beneath the body region. The state of the memory cell is determined by the concentration of charge within the body region of the semiconductor-on-insulator transistor.

While the invention was motivated in addressing the above identified issues, it is in no way so limited. The invention is only limited by the accompanying claims as literally worded, without interpretative or other

limiting reference to the specification, and in accordance with the doctrine of equivalents.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic top plan view of a semiconductor substrate in process in accordance with an aspect of the invention.

Fig. 2 is a diagrammatic section view taken through line 2-2 in Fig. 1.

Fig. 3 is a view of the Fig. 1 substrate at a processing step subsequent to that shown by Fig. 1.

Fig. 4 is a diagrammatic section view taken through line 4-4 in Fig. 3.

Fig. 5 is a view of the Fig. 4 substrate at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 5 substrate at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a view of the Fig. 6 substrate at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 7 substrate at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is a diagrammatic perspective view of the Fig. 8 substrate.

Fig. 10 is a diagrammatic top plan view of the Figs. 8 and 9 substrate, with Fig. 8 being taken through line 8-8 in Fig. 10.

Fig. 11 is a view of the Fig. 8 substrate at a processing step subsequent to that shown by Fig. 8.

Fig. 12 is a diagrammatic sectional view of an alternate embodiment substrate to that of Fig. 11.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The discussion proceeds initially with exemplary methods of forming a line of capacitorless one transistor DRAM cells. Aspects of the invention also include capacitorless one transistor DRAM cells, and integrated circuitry comprising an array of capacitorless one transistor DRAM cells, independent of the method of manufacture.

Referring to Figs. 1 and 2, a substrate (preferably a semiconductor substrate) is indicated generally with reference numeral 10. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Substrate 10 comprises a base substrate 12, for example bulk monocrystalline silicon. However, substrate 10 might comprise another substrate, whether existing or yet-to-be developed, and for example comprise a semiconductor-on-insulator substrate.

Substrate 10 is formed to comprise exemplary lines 14, 16 of spaced islands 20 of semiconductive material 18. Lines 14, 16 are shown as being essentially straight linear, although curved, jagged, angled or other shaped lines are of course contemplated. An exemplary preferred semiconductive material 18 is monocrystalline silicon, for example fabricated of exemplary bulk semiconductor substrate material 12. By way of example only, an exemplary manner of forming depicted islands 20 is by existing or yet-to-be developed trench and refill techniques of forming insulative material 22 laterally about islands 20. An exemplary preferred material includes one or a combination of silicon dioxide and/or silicon nitride. Insulative material 22 elevationally beneath islands 20 can be fabricated, for example, by ion implanting oxygen atoms into bulk substrate material 12 to a peak implant depth immediately beneath islands 20, and forming silicon dioxide therefrom. Alternately by way of example only and although less preferred, insulative material 22 might be deposited, island openings 20 etched therein, and which are subsequently filled with a semiconductive material, for example monocrystalline and/or polycrystalline silicon. Further alternately, of course, one or more techniques could be utilized whereby laterally opposing trenches are made into semiconductor substrate 12, followed by laterally undercut etching beneath islands 20, and wherein the undercut volume is subsequently filled with one or more insulative materials. Regardless, in one exemplary implementation insulative material 22 can be

considered as received laterally about and beneath respective islands 20, and contacting semiconductive material 18 of such islands. The discussion proceeds for ease of description relative to a method of forming a line of capacitorless one transistor DRAM cells relative to line 14 of spaced islands 20 of semiconductive material 18.

Referring to Figs. 3 and 4, a word line 24 is formed, which is common to and extends over line 14 of spaced islands 20. Word line 24 is formed over a floating body region 26 of the respective spaced islands 20. Word line 24 is spaced apart from and capacitively coupled to body region 26, for example by/through exemplary depicted dielectric layer 28. Such might comprise any suitable dielectric, with silicon dioxide thermally grown from preferred silicon semiconductive material 18 being but one example. An exemplary preferred thickness range for material(s) 28 is from 12 Angstroms to 100 Angstroms. Further by way of example only, an exemplary preferred depth for material 18 is from 500 Angstroms to 1,000 Angstroms. Word line 24 preferably comprises any one or combination of refractory metals, refractory metal silicides, and/or conductively doped semiconductive materials such as polycrystalline silicon. An insulative cap 30 is received over word line 24, with silicon nitride and/or silicon dioxide being exemplary materials. For purposes of the continuing discussion, word line 24 can be considered as comprising an end 32 in the exemplary Fig. 3 depiction. For purposes of the continuing discussion, floating body region 26 can be considered as having a base 34, with insulative material 22 being received thereagainst. An exemplary preferred thickness range for insulative material 22 beneath base 34 in but one implementation is from 500 Angstroms to 3,000 Angstroms.

Referring to Fig. 5, insulative material 36 is formed over the sidewalls of word lines/gates 24. Such might be comprised of a single material, or one or more materials for example with each of the depicted regions 36 comprising two or more layers of different insulative materials. Exemplary preferred materials include silicon dioxide, silicon nitride, silicon oxynitride, hafnium dioxide, and/or aluminum oxide. An exemplary preferred thickness range for material 36 is from 50 Angstroms to 150 Angstroms. Such might be formed by thermal growth or deposition over the sidewalls of the material of word line 24, as one example. Alternately by way of example only, such

might be formed by deposition and a subsequent maskless anisotropic spacer etch.

A conductive layer 38 has been formed over and spaced from word line 24, for example spaced therefrom by insulative/dielectric materials 30 and 36. Exemplary preferred materials for layer 38 include titanium nitride, polysilicon (p-type or n-type), aluminum, and cobalt silicide, with an exemplary preferred thickness range for layer 38 being from 50 Angstroms to 500 Angstroms.

Referring to Fig. 6, a masking block 40 has been formed over conductive layer 38 and word line 24. By way of example only, a preferred material for masking block 40 includes photoresist. For purposes of the continuing discussion, masking block 40 can be considered as having spaced opposing lateral edges 42 at least proximate where block 40 is received relative to conductive layer 38.

Referring to Fig. 7, masking block 40 has been heated effective to move opposing lateral edges 42 laterally outward further away from one another over conductive layer 38. An exemplary technique for doing so includes heating patterned photoresist masking block 40 at 150°C to from one to three minutes. In the exemplary preferred embodiment, opposing lateral edges 42 are moved laterally outward a distance substantially equal to the lateral thickness of material 38 outwardly of the lateral extent of word line 24 where masking block 40 is patterned initially to substantially coincide with that of the pattern from which word line 24 and insulative capping material 30 thereover are patterned.

Referring to Figs. 8-10, conductive layer 38 has been etched using masking block 40 (not shown) as a mask to form a pair of interconnected gate lines 44, 46 which are common to and extend over line 14 of spaced islands 20 along and laterally adjacent the opposing sides of word line 24, with pair of gate lines 44, 46 being received over respective floating body regions 26 of the respective spaced islands 20. Such provides but one exemplary preferred method of patterning a conductive layer 38 into a pair of gate lines which are common to and extend over the line of spaced islands along and laterally adjacent the opposing sides of the word line. For purposes of the continuing discussion, pair of gate lines 44, 46 can be considered as comprising respective ends 48, 50 proximate word line

end 32. In one exemplary implementation, the patterning of layer 38 results in word line end 32 not being longitudinally co-located with either of gate line ends 48, 50, for example as shown. In one preferred implementation, the patterning of conductive layer 38 results in word line 24 extending longitudinally beyond respective ends 48, 50 of pair of gate lines 44, 46, for example as shown. Regardless, in one preferred implementation, the patterning forms pair of gate lines 44, 46 to be shorter in length than the length of word line 24.

Referring to Figs. 9 and 10, a first conductive contact 52 is formed to word line 24, and a second conductive contact 54 is formed to pair of gate lines 44, 46. Accordingly different first and second conductive contacts are associated with the respective gate lines 44, 46 and word line 24 in a most preferred embodiment so that such can be separately controlled as recognized by people of skill in the art, and for example as described below. Contacts 52 and 54 are only diagrammatically indicated with dashed circles in Figs. 9 and 10 as such would likely be formed to the exemplary depicted locations through subsequently deposited dielectric material (not shown for clarity in the drawings.) In one exemplary preferred implementation, first conductive contact 52 is formed to some portion of word line 24 extending longitudinally beyond respective ends 48, 50 of pair of gate lines 44, 46, for example as shown.

Referring to Fig. 11, respective pairs of spaced source/drain regions 60, 62 are formed within semiconductive material 18 of islands 20 laterally outward of interconnected pair of gate lines 44, 46. Accordingly, typically and preferably, such source/drain regions are formed after the patterning of conductive layer 38. Regardless, Fig. 11 depicts an exemplary fabricated capacitorless one transistor DRAM cell 75.

In one aspect, the invention contemplates a capacitorless one transistor DRAM cell independent of the method of manufacture, and independent of whether a plurality of such DRAM cells are fabricated, although fabricating a plurality of such is preferred and would be typical. Such a DRAM cell comprises a pair of spaced source/drain regions received within semiconductive material. The above-described regions 60, 62 and formed within exemplary islands 20 of semiconductive material 18 are but exemplary constructions. An electrically floating body region is disposed

between the source/drain regions within the semiconductive material. Further by way of example only, the exemplary cell is depicted as not being fully depleted, with semiconductive material directly beneath source/drain regions 60, 62 also comprising electrically floating body region/material.

A first gate is spaced apart from and capacitively coupled to the body region between the source/drain regions. That portion of word line 24 received over an individual island 20 is but one exemplary such first gate. A pair of opposing conductively interconnected second gates is spaced from and received laterally outward of the first gate. The second gates are spaced from and capacitively coupled to the body region laterally outward of the first gate and between the pair of source/drain regions. By way of example only, second gates 44, 46 constitute an exemplary pair of such second gates. In one depicted and preferred implementation, second gates 44, 46 are conductively interconnected to one another by conductive material (i.e., a conductive material region 70) extending elevationally over first gate 24 between pair of second gates 44, 46. Pair of second gates 44, 46 might be conductively interconnected by another manner, for example and by way of example only by a separate conductive layer formed over initially isolated second gates 44, 46. In such instance, such conductive layer might be the same or different from that of material or materials from which gates 44, 46 are made. Further of course, gates 44 and 46 do not need to be of the same composition, but are preferably.

In one preferred implementation, a capacitorless one transistor DRAM cell comprises a substrate comprising an island of semiconductive material. Insulative material is received laterally about and beneath the island and contacts semiconductive material of the island. A pair of spaced source/drain regions is received within the island semiconductive material. An electrically floating body region is disposed between the source/drain regions within the island semiconductive material. A first gate is spaced apart from and capacitively coupled to the island body region between the island's source/drain regions. A pair of conductive second gates is spaced from and received laterally outward of the first gates, with the second gates being spaced from and capacitively coupled to the body region laterally outward of the first gate and between the pair of source/drain regions. Such

might be encompassed in any of the above-described methods and structures.

Fig. 12 depicts an exemplary additional implementation and embodiment alternate and corresponding to that of Fig. 11. Like numerals from the first-described embodiment have been utilized where appropriate, with differences being indicated with the suffix "a" or with different numerals. In Fig. 12, insulative material 22a is preferably received laterally about and beneath respective islands 20 and contacts semiconductive material 18 of such islands. Conductively doped semiconductive material 80 is received laterally about and beneath respective islands 20 outwardly of insulative material 22a. Exemplary preferred material 80 is conductively doped p-type or n-type polycrystalline silicon. Preferably, insulative material 22a has a thickness no greater than 200 Angstroms both beneath island 20 and intermediate the lateral sidewalls of island 20 and conductively doped semiconductive material 80. A more preferred such thickness range for material 22a is from 50 Angstroms to 150 Angstroms. The construction of Fig. 12 might, of course, be fabricated by any existing or yet-to-be developed methods.

People of skill in the art will appreciate and develop various operational voltages for writing, reading, refreshing, and/or holding data within the above-depicted exemplary DRAM cell, and in integrated circuitry comprising an array of such DRAM cells. By way of example only, the below chart depicts exemplary operating voltages, where V_i is the first gate voltage, V_{cs} (conductive spacers) are voltages for the pair of second gates, V_t is the threshold voltage, V_S is the source voltage, and V_D is the drain voltage. Further by way of example only where conductive surrounding semiconductive material 80 in the Fig. 12 embodiment is utilized, such would preferably be maintained constant at some suitable exemplary fixed voltage of -3V to -10V. A preferred, non-limiting, reason for utilizing surround conductively doped semiconductive material 80 is to establish and maintain the same potential of both sides of preferred poly of the transistor so that charge collects at the walls of the structure by the dielectric capacitance.

Exemplary Operating Voltages

	V_i	V_{cs}	V_t	V_D	V_S
Write	-3V to -10V	-2.5V	High	1.8V/0V	Float/0V
Hold Data	-3V to -10 V	0V	High	Float/Float	Float/0V
Read	2.5V	2.5V	0.5V	0.1V/0.1V	0V/0V
Re-Write	-3V to -10V	-2.5V	High	1.8V/0V	Float/0V
Hold Data	-3V to -10V	0V	High	Float/Float	Float/0V

Exemplary techniques and construction for the operation of capacitorless one transistor DRAM cells are disclosed, by way of example, in U.S. Patent No. 6,969,662; U.S. Patent Application Publication Nos. 2005/0017240 and 2005/0063224; Kuo et al., "A Capacitorless Double-Gate DRAM Gate Cell Design For High Density Applications", IEDM, IEEE 2002, pp. 843-846 and Yoshida et al., "A Capacitorless 1 T-DRAM Technology Using Gate-Induced Drain-Leakage (GIDL) Current For Low-Power And High-Speed Embedded Memory", IEEE Transactions on Electron Devices, Vol. 53, No. 4, April 2006, pp. 692-697. The disclosures of U.S. Patent Nos. 5,714,786; 6,005,273; 6,090,693; and 7,005,710 are herein incorporated by reference.

CLAIMS

What is claimed is:

1. A capacitorless one transistor DRAM cell, comprising:

a pair of spaced source/drain regions received within semiconductive material;

an electrically floating body region disposed between the source/drain regions within the semiconductive material;

a first gate spaced apart from and capacitively coupled to the body region between the source/drain regions; and

a pair of opposing conductively interconnected second gates spaced from and received laterally outward of the first gate, the second gates being spaced from and capacitively coupled to the body region laterally outward of the first gate and between the pair of source/drain regions.

2. The DRAM cell of claim 1 wherein the pair of second gates is conductively interconnected by conductive material extending elevationally over the first gate between the pair of second gates.

3. The DRAM cell of claim 1 wherein the first gate is separated from the second gates by at least two insulative materials.

4. The DRAM cell of claim 1 wherein the floating body region has a base, an insulative layer being received against the base, the insulative layer having a thickness of from 500 Angstroms to 3,000 Angstroms.

5. The DRAM cell of claim 1 wherein:

the floating body region has a base, an insulative layer being received against the base; and

conductively doped semiconductive material received against the insulative layer beneath the base.

6. The DRAM cell of claim 5 wherein the insulative layer has a thickness no greater than 200 Angstroms intermediate the base and the conductively doped semiconductive material.

7. A capacitorless one transistor DRAM cell, comprising:

a substrate comprising an island of semiconductive material;

insulative material received laterally about and beneath the island and contacting semiconductive material of the island;

a pair of spaced source/drain regions received within the island semiconductive material;

an electrically floating body region disposed between the source/drain regions within the island semiconductive material;

a first gate spaced apart from and capacitively coupled to the island body region between the island source/drain regions; and

a pair of conductive second gates spaced from and received laterally outward of the first gate, the second gates being spaced from and capacitively coupled to the body region laterally outward of the first gate and between the pair of source/drain regions.

8. The DRAM cell of claim 7 comprising conductively doped semiconductive material received laterally about and beneath the island outwardly of the insulative material.

9. The DRAM cell of claim 8 wherein the insulative material has a thickness no greater than 200 Angstroms beneath the island.

10. The DRAM cell of claim 8 wherein the insulative material has a thickness no greater than 200 Angstroms intermediate lateral sidewalls of the island and the conductively doped semiconductive material.

11. The DRAM cell of claim 8 wherein the insulative material has a thickness no greater than 200 Angstroms beneath the island and intermediate lateral sidewalls of the island and the conductively doped semiconductive material.

12. The DRAM cell of claim 8 wherein the insulative material has a thickness from 50 Angstroms to 150 Angstroms beneath the island.

13. The DRAM cell of claim 8 wherein the insulative material has a thickness from 50 Angstroms to 150 Angstroms intermediate lateral sidewalls of the island and the conductively doped semiconductive material.

14. Integrated circuitry comprising an array of capacitorless one transistor DRAM cells, comprising:

a line of spaced islands of semiconductive material received within a substrate; and

individual capacitorless one transistor DRAM cells being received relative to individual of the spaced islands, the individual cells comprising:

a pair of source/drain regions received within the semiconductive material of the respective island;

an electrically floating body region disposed between the source/drain regions within the semiconductive material of the respective island;

a first gate comprised of a word line which is common to and extends over the line of spaced islands between the respective pairs of source/drain regions, the word line being spaced apart from and capacitively coupled to the respective body regions of the respective islands between the respective pairs of source/drain regions; and

a pair of opposing conductively interconnected second gates spaced from the first gate and received laterally outward of the first gate, the second gates being spaced from and capacitively coupled to the respective body regions laterally outward of the respective first gates and between the respective pairs of source/drain regions of the respective islands, the pairs of opposing interconnected second gates comprising a conductive line which is common to the line of spaced islands and is received elevationally and laterally over and along the word line.

15. The integrated circuitry of claim 14 comprising a first conductive contact connected to the word line and a different second conductive contact connected to the conductive line.

16. The integrated circuitry of claim 14 wherein the word line is longer in length than the conductive line.

17. The integrated circuitry of claim 14 wherein the conductive line has an end and the word line has an end proximate the conductive line end, said word line end and said conductive line end not being longitudinally co-located.

18. The integrated circuitry of claim 17 wherein the word line is longer in length than the conductive line.

19. The integrated circuitry of claim 17 wherein the word line end is received longitudinally outward of the conductive line end.

20. The integrated circuitry of claim 19 wherein the word line is longer in length than the conductive line.

21. The integrated circuitry of claim 14 comprising insulative material received laterally about and beneath the respective islands and contacting semiconductive material of the respective islands; and

conductively doped semiconductive material received laterally about and beneath the island outwardly of the insulative material.

22. The integrated circuitry of claim 21 wherein the insulative material has a thickness no greater than 200 Angstroms beneath the respective islands and intermediate lateral sidewalls of the respective islands and the conductively doped semiconductive material.

23. A method of forming a line of capacitorless one transistor DRAM cells, comprising:

forming a line of spaced islands of semiconductive material relative to a substrate;

forming a word line which is common to and extends over the line of spaced islands, the word line being formed over an electrically floating body region of the respective spaced islands;

forming a conductive layer over and spaced from the word line;

patterning the conductive layer into a pair of gate lines which are common to and extend over the line of spaced islands along and laterally adjacent opposing sides of the word line, the pair of gates lines being received over respective floating body regions of the respective spaced islands, the patterning forming the pair of gate lines to be shorter in length than length of the word line; and

forming respective pairs of spaced source/drain regions within the semiconductive material of the respective islands, the pairs of spaced source/drain regions being received laterally outward of the pair of gate lines.

24. The method of claim 23 wherein the source/drain regions are formed after said patterning.

25. The method of claim 23 comprising forming a first conductive contact to the word line and a second conductive contact to the pair of gate lines.

26. The method of claim 23 wherein the word line is formed to have an end and the patterning forms a respective end of the pair of gate lines that is proximate the word line end, the patterning resulting in the word line end not being longitudinally co-located with either of said gate line ends.

27. The method of claim 23 wherein the patterning comprises:

forming a masking block over the conductive layer and the word line, the masking block having spaced opposing lateral edges;

after forming the masking block, heating the masking block effective to move the opposing lateral edges laterally outward further away from one another over the conductive layer; and

after the heating, etching the conductive layer using the masking block as a mask to form said pair of gate lines.

28. The method of claim 27 wherein the word line is formed to have an end and the patterning forms a respective end of the pair of gate lines

that is proximate the word line end, the patterning resulting in the word line end not being longitudinally co-located with either of said gate line ends.

29. The method of claim 23 comprising:

providing insulative material laterally about and beneath the respective islands and contacting semiconductive material of the respective islands; and

providing conductively doped semiconductive material laterally about and beneath the island outwardly of the insulative material.

30. A method of forming a line of capacitorless one transistor DRAM cells, comprising:

forming a line of spaced islands of semiconductive material relative to a substrate;

forming a word line which is common to and extends over the line of spaced islands, the word line being formed over an electrically floating body region of the respective spaced islands and comprising an end;

forming a conductive layer over and spaced from the word line;

patterning the conductive layer into a pair of gate lines which are common to and extend over the line of spaced islands along and laterally adjacent opposing sides of the word line, the pair of gates lines being received over respective floating body regions of the respective spaced islands, the patterning forming respective ends of the pair of gate lines proximate the word line end, the patterning resulting in the word line extending longitudinally beyond the respective ends of the pair of gate lines; and

forming respective pairs of spaced source/drain regions within the semiconductive material of the respective islands, the pairs of spaced source/drain regions being received laterally outward of the pair of gate lines.

31. The method of claim 30 wherein the patterning comprises:

forming a masking block over the conductive layer and the word line, the masking block having spaced opposing lateral edges;

after forming the masking block, heating the masking block effective

to move the opposing lateral edges laterally outward further away from one another over the conductive layer; and

after the heating, etching the conductive layer using the masking block as a mask to form said pair of gate lines.

32. The method of claim 30 comprising forming a first conductive contact to the word line and a second conductive contact to the pair of gate lines.

33. The method of claim 32 comprising forming the first conductive contact to some portion of the word line extending longitudinally beyond the respective ends of the pair of gate lines.

34. The method of claim 30 comprising:

providing insulative material laterally about and beneath the respective islands and contacting semiconductive material of the respective islands; and

providing conductively doped semiconductive material laterally about and beneath the island outwardly of the insulative material.

35. A method of forming a line of capacitorless one transistor DRAM cells, comprising:

forming a line of spaced islands of semiconductive material relative to a substrate;

forming a word line which is common to and extends over the line of spaced islands, the word line being formed over an electrically floating body region of the respective spaced islands;

forming a conductive layer over and spaced from the word line;

forming a masking block over the conductive layer and the word line, the masking block having spaced opposing lateral edges;

after forming the masking block, heating the masking block effective to move the opposing lateral edges laterally outward further away from one another over the conductive layer;

after the heating, etching the conductive layer using the masking block as a mask to form a pair of interconnected gate lines which are

common to and extend over the line of spaced islands along and laterally adjacent opposing sides of the word line, the pair of gates lines being received over respective floating body regions of the respective spaced islands; and

forming respective pairs of spaced source/drain regions within the semiconductive material of the respective islands, the pairs of spaced source/drain regions being received laterally outward of the interconnected pair of gate lines.

36. The method of claim 35 comprising forming the masking block to comprise photoresist.

37. The method of claim 35 wherein the source/drain regions are formed after said patterning.

38. The method of claim 35 comprising forming a first conductive contact to the word line and a second conductive contact to the pair of gate lines.

39. The method of claim 38 comprising forming the first conductive contact to some portion of the word line extending longitudinally beyond the respective ends of the pair of gate lines.