

Voltage Measuring Method, Electrical Test Method and Apparatus,
Semiconductor Device manufacturing Method and Device Substrate
Manufacturing Method



159159

BACKGROUND OF THE INVENTION



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5 1. Technical Field of the Invention

The present invention relates to a voltage measuring method for reading a value of a voltage applied to a pixel electrode by operating each of the pixels possessed by a semiconductor device, and to a method for conducting a test as to whether a pixel region normally operates or not by using the voltage measuring
10 method. Particularly, the invention relates to a non-contact voltage measuring method and electrical test method, and non-contact electrical test apparatus using the same. The invention also relates to a manufacturing method for a semiconductor device including a test process using the test method, and to a semiconductor device manufactured by the use of the semiconductor device
15 manufacturing method. Furthermore, the invention relates to a manufacturing method for a device substrate including a test process by using the test method.

Meanwhile, the invention relates, in an OLED panel having an organic light-emitting device (OLED) sealed between the substrate and a cover member, to a voltage measuring method for reading a value of a voltage applied to the pixel
20 electrode by operating the pixel prior to forming OLEDs, and to a method for testing as to whether the pixel region normally operates or not by using the voltage measuring method. Particularly, the invention relates to a noncontact electric test method and to a noncontact electric test apparatus using the same.

In the description, the OLED panel mounted with an IC or the like including

a controller is referred to as an OLED module. Meanwhile, the OLED panel and the OLED module are referred collectively to as a light-emitting device.

2. Description of the Related Art

Recently, the technology for forming TFTs on a substrate has markedly
5 advanced. The development has been proceeded for the application to the active-matrix electronic display. Particularly, the TFT using a polysilicon film has a high field-effect mobility (called also mobility) than that of the TFT using an amorphous silicon film, hence enabling high-speed operation. Consequently, the control of pixels, conventionally done by a drive circuit provided outside the substrate, can be
10 made on a drive circuit formed on the same substrate as the pixels.

With such an active-matrix electronic display, various merits are available including manufacture cost reduction, electronic display size reduction, yield improvement and throughput reduction by fabricating various circuits and elements on the same substrate.

15 Of among the electronic displays, studies have actively made on the active-matrix light-emitting device having light-emitting elements of OLEDs.

The OLED, spontaneous to emit light, is high in visibility, optimal in thickness reduction because of not requiring a backlight as required in the liquid crystal display (LCD), and limitless in its viewing angle. Consequently, the light-emitting
20 devices using OLEDs has drawn attentions as display devices replacing the CRTs and LCDs.

The OLED has a layer containing an organic compound (organic light-emitting material) to obtain electroluminescence caused by applying an electric field (hereinafter, described as organic light-emitting layer), an anode layer and a cathode
25 layer. In the description, every layer provided between the anode and the cathode

of an OLED is defined as an organic light-emitting layer. The organic light-emitting layer includes, concretely, a light-emitting layer, a hole injection layer, an electron injection layer, a hole transport layer and an electron transport layer. The electroluminescence on organic compound includes light emission (fluorescence) of upon returning from a singlet excitation state to the ground state and light emission (phosphorescence) of upon returning from a triplet excitation state to the ground state.

The organic light-emitting layer acceleratedly deteriorates due to heat, light, moisture, oxygen and the like. In manufacturing an active-matrix light emitting device, generally OLEDs are formed after forming interconnections and TFTs in a pixel region at comparatively high process temperature in the manufacturing process.

After forming the OLEDs, the substrate having the OLEDs (OLED panel) and a cover member are bonded together in a manner not to expose the OLEDs to the outside air and then sealed (packaged) by a seal member or the like.

After enhancing hermetical sealability by a process of packaging or the like, a connector (FPC, TAB or the like) is attached to allow the connection of between the terminal extended from the elements or circuits formed on the substrate and an external signal terminal. Thus, an active-matrix light-emitting device is completed.

In the active-matrix light-emitting device, the voltage applied from a pair of electrodes of the OLED to the organic light-emitting layer is controlled by the TFT provided on each pixel. Consequently, when there is a point a certain trouble occurs (faulty point), e.g. the TFT possessed by the pixel region does not function as a switch element or the interconnection is disconnected or short-circuited, a predetermined voltage cannot be applied to the organic light-emitting layer

possessed by the OLED. In such a case, the pixel cannot make display at a desired tonal level.

In the active-matrix liquid crystal display placed under mass production prior to the active-matrix light-emitting device, interconnections and TFTs are formed in a pixel region before completing a liquid crystal display by filling a liquid crystal between a panel having a pixel region (liquid crystal panel) and a substrate having a counter electrode. Thereafter, charge is stored on the capacitor possessed by each pixel. By measuring the amount of charge on a pixel-by-pixel basis, a test is conducted as to whether there is a defect in the pixel region or not.

However, the light-emitting device, in many cases, has two or more TFTs on each pixel. There is a case that one of the electrodes of the OLED (pixel electrode) and the capacitor are connected together through the TFT. In this case, even by measuring the amount of the charge stored on the capacitor, it is difficult to test whether or not there is a defect in the interconnections between the capacitors and pixel electrodes and in all the TFTs.

Meanwhile, when the OLED panel before attached with a connector is tested for electric operation, there is a need to use a fine pin (probe) on the terminal or interconnection of the OLED panel in order to flow current or apply voltage. However, the direct use of a probe on the interconnection or terminal might cause a flaw on the interconnection or terminal to produce fine dust. The dust caused in the test process unfavorably forms a cause to lower the yield in the subsequent processes.

The actual display made on a completed light-emitting device makes it possible to confirm whether there is a defect or not. However, there is a necessity, for even an OLED panel actually not provided as a product, to complete as a light-emitting device by forming OLEDs, packaging and attaching connectors in order to

discriminate it from the normal product. In the case the OLED panel is defective, it is impossible to suppress time and cost because of the wastefulness in the OLED forming process, packaging process and connector attaching process. Meanwhile, where a multi-dividable substrate is used to form OLED panels, the process of
5 packaging and attaching connectors is wasteful, thus similarly making impossible to suppress time and cost.

In view of the foregoing problem, it is a problem of the present invention to establish an electric test method (hereinafter, merely test method) capable of confirming as to whether there is a trouble generated on an interconnection or TFT
10 in a pixel region before completing a light-emitting device, toward the mass production of active-matrix light-emitting devices, and to provide an electric test apparatus (hereinafter, merely test apparatus) using the test method. Furthermore, it is a problem to establish a simpler test method in a manufacturing process for a light-emitting device without the necessity to use a probe on an interconnection or
15 terminal, and to provide a test apparatus using the test method. Furthermore, it is a problem to provide a method for manufacturing a semiconductor device by using the electric test method, and a semiconductor device manufactured by using the manufacturing method.

The present inventor has considered that, by the use of electromagnetic
20 induction, voltage is to be applied, without contact, to the interconnection possessed by a pixel region of a substrate forming TFTs and pixel electrodes (hereinafter referred to as device-substrate) without the use of a probe thereon. By applying a voltage to the interconnection, each pixel is operated to apply voltage to the pixel electrode.

25 In the description, to operate a pixel means to apply a voltage to an element or interconnection possessed by the pixel, i.e. to control the voltage on the pixel

electrode.

The voltage applied to the pixel electrode is read in value, without contact, by the use of electrostatic induction. From the read value, it is possible to determine an operating state and furthermore a normality/abnormality of each pixel, in other
5 words, whether each pixel normally operates or not. In the description, the pixel a voltage can be desirably applied to the pixel electrode thereof is determined normal. Conversely, the pixel a voltage cannot be desirably applied to the pixel electrode is determined abnormal.

Specifically, there include the following two schemes, which one may be
10 used.

In the first scheme, separately prepared is a testing substrate with which the device substrate is to be tested. The testing substrate has a primary coil while the device substrate as a subject-of-test has a secondary coil.

Each of the primary and secondary coils can be formed by patterning a
15 conductive film formed on the substrate. In the invention, the primary and secondary coils use coils without a magnetic member at a center thereof instead of coils having a magnetic member at the center to provide a magnetic path.

The primary coil possessed by the testing substrate and the secondary coil possessed by the device substrate are superposed together through a constant
20 spacing. By applying an alternating current voltage to between two terminals possessed by the primary coil, an electromagnetic force is caused between two terminals possessed by the secondary coil.

The spacing is desirably smaller. The primary coil and the secondary coil are as near as possible as long as the spacing is to be controlled.

25 In the description, voltage is applied to a coil means that the voltage is applied to between the terminals of the coil. In the description, signal is applied to a coil

means that the voltage of the signal is applied to the two terminals possessed by the coil.

The alternating current voltage caused as an electromagnetic force on the secondary coil is rectified on the device substrate and then smoothened. This is
5 used as a direct current voltage to operate the drive circuit or pixel possessed by the device substrate (hereinafter, referred to as power voltage). Meanwhile, the waveform of the alternating current voltage caused as an electromotive force on the secondary coil is shaped into a desired form by a waveform shaper circuit or the like. This is used as a signal having a voltage to operate the drive circuit or pixel
10 possessed by the device substrate (hereinafter, referred to as drive signal). The alternating current voltage generated on the secondary coil may be used as it is as a drive signal without shaping its waveform in the waveform shaper circuit.

The voltage or power voltage of a generated drive signal is supplied to the drive circuit or pixel formed on the device substrate. By supplying the drive-signal
15 voltage or power voltage, the drive circuit or pixel makes certain operation.

The drive-signal voltage or power voltage is determined in its value such that, where the drive circuit or pixel is normal, the voltage applied to the pixel electrode possessed by the pixel is given an alternating current voltage.

By supplying a drive-signal voltage or power voltage, the voltage applied to the
20 pixel electrode is influenced in its value depending upon an operating state of the drive circuit or pixel.

The drive-signal voltage or power voltage may be supplied only to the pixels formed on the device substrate. In this case, by supplying a drive-signal voltage or power voltage, the voltage applied to the pixel electrode is influenced in its value
25 depending upon an operating state of the pixel.

The electrode (testing electrode) for reading, without contact, a voltage

generated on the pixel electrode is superposed with the pixel electrode through a constant spacing. The spacing is preferably smaller. The pixel electrode and the testing electrode are preferably as near as possible as long as the spacing is to be controlled. The testing substrate may have a testing electrode.

5 The voltage generated on the testing electrode due to electrostatic induction is influenced by a value of the voltage applied to the pixel electrode. Accordingly, a voltage being applied to the pixel electrode can be calculated from a voltage generated on the testing electrode. As a result, the value of a voltage applied to the pixel electrode can be read out, without contact. Furthermore, by using the voltage
10 generated on the testing electrode, the operating state of a pixel can be grasped. It is possible to confirm an operating state thereof and determine a normality/abnormality.

In the second scheme, separately prepared are a testing substrate (first testing substrate) to apply, without contact, a voltage to the interconnection possessed by
15 the pixel region of the device substrate and a testing substrate (second testing substrate) to read, without contact, a value of the voltage applied to the pixel electrode by using electrostatic induction.

The first testing substrate has a primary coil while the device substrate as a subject-of-test has a secondary coil.

20 The primary and secondary coils each can be formed by patterning a conductive film formed on a insulation film. In the invention, the primary and secondary coils use coils not having a magnetic member at a center instead of coils having a magnetic member at the center to provide a magnetic path.

The primary coil possessed by the first testing substrate and the secondary coil
25 possessed by the device substrate are superposed together through a constant spacing. By applying an alternating current voltage to between the two terminals

possessed by the primary coil, an electromotive force is caused at between the two terminals possessed by the secondary coil.

The spacing is preferably smaller. The primary coil and the secondary coil are preferably as near as possible as long as the spacing is to be controlled.

5 In the description, voltage is applied to a coil means that the voltage is applied to between the terminals of the coil. In the description, signal is applied to a coil means that the voltage of the signal is applied to the two terminals possessed by the coil.

The alternating current voltage caused as an electromagnetic force on the
10 secondary coil is rectified in the device substrate and then smoothened. This is used as a power voltage to operate the drive circuit or pixel possessed by the device substrate. Meanwhile, the waveform of the alternating current voltage caused as an electromotive force on the secondary coil is shaped into a desired form by a waveform shaper circuit or the like. This is used as a drive signal having a voltage
15 to operate the drive circuit or pixel possessed by the device substrate. The alternating current voltage generated on the secondary coil may be used as it is as a drive signal without shaping the waveform in the waveform shaper circuit.

The voltage or power voltage of a generated drive signal is supplied to the drive circuit or pixel formed on the device substrate. By supplying the drive-signal
20 voltage or power voltage, the drive circuit or pixel makes certain operation.

The drive-signal voltage or power voltage is determined in its value such that, where the drive circuit or pixel is normal, the voltage applied to the pixel electrode possessed by the pixel is given an alternating current voltage.

By supplying a drive-signal voltage or power voltage, the voltage applied to the
25 pixel electrode is influenced in its value depending upon an operating state of the drive circuit or pixel.

The drive-signal voltage or power voltage may be supplied only to the pixels possessed by the device substrate. In this case, by supplying a drive-signal voltage or power voltage, the voltage applied to the pixel electrode is influenced in its value depending upon an operating state of the pixel.

5 On the other hand, the second testing substrate has an electrode (testing electrode) for reading, without contact, a voltage generated on the pixel electrode. The testing electrode is superposed with the pixel electrode through a constant spacing. The spacing is desirably smaller. The pixel electrode and the testing electrode are preferably as near as possible as long as the spacing is to be
10 controlled.

The active-matrix semiconductor device has a plurality of pixel electrodes arranged in a matrix form in the pixel region. In the invention, by changing the position of the second testing substrate relatively to the device substrate, one or a plurality of pixel electrodes superposed with one testing electrode is changed in
15 position in plurality of times. Specifically, by rotating the testing electrode on a plane parallel with the device substrate, it is possible to change the position of the pixel electrodes superposed with the testing electrode. Each time, monitored is a value of the voltage generated on the testing electrode.

The voltage generated on the testing substrate due to electrostatic induction
20 has as the information an operating state of the pixel, and influenced by a value of the voltage applied to the pixel electrode being superposed with the testing electrode.

Then, stored are values of the voltage generated on the testing electrode obtained through monitoring in plurality of times, and positional data of one or a
25 plurality of pixel electrodes superposed with the testing electrode upon monitoring. By the use of restoring algorithm (e.g. Fourier transformation method) for restoring

a two-dimensional distribution from one-dimensional data used in CT (computed tomography), it is possible to obtain a relative value of a voltage being applied to the pixels from the stored data. Namely, it can be resultingly considered possible to read, without contact, a value of the voltage being applied to the pixel electrodes.

- 5 From the relative value of the voltage being applied to the pixels, it is possible to determine an operating state of each pixel. From the operating state, normality/abnormality can be determined.

The restoring algorithm includes, representatively, a Fourier transformation method using successive approximation and projection section theorem, and a
10 superposition integration method. The invention may use a restoring algorithm of other than these.

Note that, in the first or second scheme, pixel operating state may be screened into a plurality of ranks depending on an operating state, instead of selection into the two of normality and abnormality at all times.

- 15 Meanwhile, in the first and second schemes, in the case that the drive circuit has a defect but the pixel does not have a defect, varied is a value of the voltage to be applied to the pixel electrode. Accordingly, the drive circuit can also be determined for its normality/abnormality.

In the semiconductor device using the test method of the invention, the
20 transistor used in the pixel may be a transistor formed using single-crystal silicon, or a thin-film transistor using polysilicon or amorphous silicon. Otherwise, it may be a transistor using an organic semiconductor.

It is possible for a practitioner to properly determine a criterion whether a pixel is considered not in a normal operation depending upon about what degree an
25 operating state of the pixel differs from an operating state of the normal pixel.

The invention, by the above structure, can detect a defective point and

determine a normality/abnormality of a pixel without the use of a probe directly on the interconnection. It is accordingly possible to prevent against the yield lowering in the following processes due to the fine dust caused upon using a probe. Furthermore, because the normality/abnormality in every pattern forming process
5 can be determined by one test process, the test process can be simplified.

The invention is applicable not only to a light-emitting device but also to a liquid crystal display or other semiconductor devices.

Now, the structure of the invention will be explained.

The present invention concerns a method of measuring a voltage
10 comprising:

applying, without contact, a voltage to an interconnection or circuit element possessed by a pixel to thereby apply a voltage to a pixel electrode possessed by the pixel; and

reading, without contact, the voltage applied to the pixel electrode.

15 The present invention concerns a method of measuring a voltage comprising:

applying, without contact, a voltage to interconnections or circuit elements respectively possessed by a plurality of pixels to thereby apply voltages to pixel electrodes respectively possessed by the pixels; and

20 reading, without contact, a sum of the voltages applied to the pixel electrodes respectively possessed by the pixels.

The invention concerns a method of measuring a voltage comprising:

applying a first alternating current voltage to between two terminals possessed by a first coil;

25 superposing the first coil and a second coil together through a constant spacing;

applying a third alternating current voltage to a pixel electrode possessed by a pixel by using a second alternating current voltage generated between two terminals possessed by the second coil;

superposing the pixel electrode and the testing electrode together through a
5 constant spacing; and

calculating the voltage applied to the pixel electrode from a fourth alternating current voltage generated on the testing electrode.

The invention concerns a method of measuring a voltage comprising:

applying a first alternating current voltage to between two terminals possessed
10 by a first coil;

superposing the first coil and a second coil together through a constant spacing;

rectifying or waveform-shaping a second alternating current voltage caused between two terminals possessed by the second coil and applying it to an
15 interconnection or circuit element possessed by a pixel, to thereby applying a third alternating current voltage to a pixel electrode possessed by the pixel;

superposing the pixel electrode and a testing electrode together through a constant spacing; and

calculating the voltage applied to the pixel electrode from a fourth alternating
20 current voltage generated on the testing electrode.

The invention concerns a method of measuring a voltage comprising:

applying a first alternating current voltage to between two terminals possessed by a first coil;

superposing the first coil and a second coil together through a constant
25 spacing;

applying a third alternating current voltage to pixel electrodes respectively

possessed by a plurality of pixels by using a second alternating current voltage caused between two terminals possessed by the second coil;

superposing the pixel electrodes possessed by the pixels and the testing electrode together through a constant spacing; and

5 calculating a sum of voltages applied to the pixel electrodes respectively possessed by the pixels from a fourth alternating current voltage generated on the testing electrode.

The invention concerns a method of measuring a voltage comprising:

10 applying a first alternating current voltage to between two terminals possessed by a first coil;

superposing the first coil and a second coil together through a constant spacing;

15 rectifying or waveform-shaping a second alternating current voltage caused between two terminals possessed by the second coil and applying it to interconnections or circuit elements respectively possessed by a plurality of pixels, to thereby applying a third alternating current voltage to pixel electrodes respectively possessed by the pixels;

superposing the pixel electrodes respectively possessed by the pixels and a testing electrode together through a constant spacing; and

20 calculating a sum of the voltages applied to the pixel electrodes respectively possessed by the pixels from a fourth alternating current voltage generated on the testing electrode.

In the invention, the first coil and the second coil may have interconnections formed on a same plane and each of the interconnections is in a vortex form.

25 In the invention, the first coil and the testing electrode may be formed on a first insulation surface,

the second coil and the pixel electrode being formed on a second insulation surface.

In the invention, a spacing between the first insulation surface and the second insulation surface may be controlled by flowing a fluid between the first insulation
5 surface and the second insulation surface.

In the invention, the pixel may be determined for a normality/abnormality by using a voltage applied to the pixel electrode obtained using the voltage measuring method or a sum thereof.

The invention concerns an apparatus for electrically testing pixels possessed
10 by a semiconductor device, the electrical test apparatus comprising:

a primary coil;

means for superposing the primary coil and a secondary coil possessed by the semiconductor device together through a constant spacing;

means for superposing a pixel electrode possessed by the pixel and a testing
15 electrode together through a constant spacing;

means for applying an alternating current voltage to between two terminals possessed by the primary coil; and

means for confirming an operating state of the pixel from an alternating current voltage generated on the testing electrode.

20 The invention concerns an apparatus for electrically testing pixels possessed by a semiconductor device, the electric test apparatus comprising:

a primary coil;

means for superposing the primary coil and a secondary coil possessed by the semiconductor device together through a constant spacing;

25 means for superposing a pixel electrode possessed by the pixel and a testing electrode together through a constant spacing;

means for applying an alternating current voltage to between two terminals possessed by the primary coil; and

means for confirming an operating state of the pixel from an alternating current voltage generated on the testing electrode;

5 whereby the alternating current voltage generated on the testing electrode has, as information, an operating state of the pixel.

In the invention, the spacing between the primary coil and the secondary coil may be controlled by flowing a fluid between the primary coil and the secondary coil.

10 In the invention, the first coil may have an interconnection formed on a same plane and the interconnection be in a vortex form.

The invention concerns a method for manufacturing a semiconductor device comprising:

forming a pixel electrode and an interconnection or circuit element;

15 applying, without contact, a voltage to the interconnection or circuit element to thereby applying a voltage to the pixel electrode; and

reading, without contact, the voltage applied to the pixel electrode.

The invention concerns a method for manufacturing a semiconductor device comprising:

20 forming a pixel electrode, an interconnection or circuit element, a first coil and a second coil;

applying a first alternating current voltage to between two terminals possessed by the first coil;

25 superposing the first coil and the second coil together through a constant spacing;

applying a third alternating current voltage to the pixel electrode by using a

second alternating current voltage caused between two terminals possessed by the second coil;

superposing the pixel electrode and a testing electrode together through a constant spacing; and

5 calculating the voltage applied to the pixel electrode from a fourth alternating current voltage generated on the testing electrode.

The invention concerns a method for manufacturing a semiconductor device comprising:

forming a pixel electrode, an interconnection or circuit element, a first coil and
10 a second coil;

applying a first alternating current voltage to between two terminals possessed by the first coil;

superposing the first coil and the second coil together through a constant spacing;

15 rectifying or waveform-shaping a second alternating current voltage caused between two terminals possessed by the second coil and applying it to an interconnection or circuit element, to thereby applying a third alternating current voltage to the pixel electrode;

superposing the pixel electrode and a testing electrode together through a
20 constant spacing; and

calculating the voltage applied to the pixel electrode from a fourth alternating current voltage generated on the testing electrode.

The invention concerns a method of measuring a voltage comprising:

applying a voltage to an interconnection or circuit element for controlling a
25 voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with an arbitrary part or all

of the pixel electrodes through a spacing; and

calculating a voltage applied to each of the pixel electrodes from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

5 The invention concerns a method of measuring a voltage comprising:

applying, without contact, a voltage to an interconnection or circuit element for controlling a voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing; and

10 calculating a voltage applied to each of the pixel electrodes from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

The invention concerns a method of measuring a voltage comprising:

15 applying a first alternating current voltage to between two terminals possessed by a first coil;

superposing the first coil and a second coil together through a spacing;

applying a second alternating current voltage caused between two terminals possessed by the second coil to an interconnection or circuit element for controlling a voltage to be applied to a plurality of pixel electrodes;

20 moving a testing electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing; and

calculating a voltage applied to each of the pixel electrodes from a third alternating current voltage generated on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

25 The invention concerns a method of measuring a voltage comprising:

applying a first alternating current voltage to between two terminals possessed

by a first coil;

superposing the first coil and a second coil together through a spacing;

rectifying or waveform-shaping a second alternating current voltage caused
between two terminals possessed by the second coil and applying it to an
5 interconnection or circuit element for controlling a voltage to be applied to a
plurality of pixel electrodes;

moving a testing electrode while being superposed with an arbitrary part or all
of the pixel electrodes through a spacing; and

calculating a voltage applied to each of the pixel electrodes from a third
10 alternating current voltage generated on the testing electrode and a position of the
testing electrode relative to the pixel electrodes.

In the invention, the first coil and the second coil may have interconnections
formed on a same plane and the interconnections be in a vortex form.

In the invention, the spacing between the first coil and the second coil may be
15 controlled by flowing a fluid between the first coil and the second coil.

In the invention, the voltage on each of the pixel electrodes may be calculated
using a Fourier transformation method using successive approximation and
projection section theorem or a superposition integration method.

The invention concerns an electrical test method comprising:

20 applying a voltage to an interconnection or circuit element for controlling a
voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with an arbitrary part or all
of the pixel electrodes through a spacing; and

confirming an operating state of the interconnection or circuit element from
25 a voltage on the testing electrode and a position of the testing electrode relative to
the pixel electrodes.

The invention concerns an electrical test method comprising:

applying, without contact, a voltage to an interconnection or circuit element for controlling a voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with an arbitrary part or all
5 of the pixel electrodes through a spacing; and

confirming an operating state of the interconnection or circuit element from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

The invention concerns an electrical test method comprising:

10 applying a voltage to an interconnection or circuit element for controlling a voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing; and

determining a distribution of a voltage to be applied to the pixel electrodes
15 from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

The invention concerns an electrical test method comprising:

applying, without contact, a voltage to an interconnection or circuit element for controlling a voltage to be applied to a plurality of pixel electrodes;

20 moving a testing electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing; and

determining a distribution of a voltage to be applied to the pixel electrodes from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

25 The invention concerns an electrical test method comprising:

applying a voltage to an interconnection or circuit element for controlling a

voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing;

determining a distribution of a voltage to be applied to the pixel electrodes
5 from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes; and

confirming an operating state of the interconnection or circuit element from the voltage distribution.

The invention concerns an electrical test method comprising:

10 applying, without contact, a voltage to an interconnection or circuit element for controlling a voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing;

determining a distribution of a voltage to be applied to the pixel electrodes
15 from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes; and

confirming an operating state of the interconnection or circuit element from the voltage distribution.

The invention concerns an electrical test method comprising:

20 applying a first alternating current voltage to between two terminals possessed by a first coil;

superposing the first coil and a second coil together through a spacing;

applying a second alternating current voltage caused between two terminals possessed by the second coil to an interconnection or circuit element for controlling
25 a voltage to be applied to a plurality of pixel electrodes;

moving a test electrode while being superposed with an arbitrary part or all of

the pixel electrodes through a spacing; and

confirming an operating state of the interconnection or circuit element from a third alternating current voltage generated on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

5 The invention concerns an electrical test method comprising:

applying a first alternating current voltage to between two terminals possessed by a first coil;

superposing the first coil and a second coil together through a spacing;

applying a second alternating current voltage caused between two terminals
10 possessed by the second coil to an interconnection or circuit element for controlling a voltage to be applied to a plurality of pixel electrodes;

moving a test electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing;

determining a distribution of a voltage to be applied to the pixel electrodes
15 from a third alternating current voltage generated on the testing electrode and a position of the testing electrode relative to the pixel electrodes; and

confirming an operating state of the interconnection or circuit element from the voltage distribution.

The invention concerns an electrical test method comprising:

20 applying a first alternating current voltage to between two terminals possessed by a first coil;

— superposing the first coil and a second coil together through a spacing;

rectifying or waveform-shaping a second alternating current voltage caused between two terminals possessed by the second coil and applying it to an
25 interconnection or circuit element for controlling a voltage to be applied to the pixel electrodes;

moving a test electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing; and

confirming an operating state of the interconnection or circuit element from a third alternating current voltage generated on the testing electrode and a position
5 of the testing electrode relative to the pixel electrodes.

The invention concerns an electrical test method comprising:

applying a first alternating current voltage to between two terminals possessed by a first coil;

superposing the first coil and a second coil together through a spacing;

10 rectifying or waveform-shaping a second alternating current voltage caused between two terminals possessed by the second coil and applying it to an interconnection or circuit element for controlling a voltage to be applied to the pixel electrodes;

moving a test electrode while being superposed with an arbitrary part or all of
15 the pixel electrodes through a spacing; and

determining a distribution of a voltage to be applied to the pixel electrodes from a third alternating current voltage generated on the testing electrode and a position of the testing electrode relative to the pixel electrodes; and

confirming an operating state of the interconnection or circuit element from
20 the voltage distribution.

In the invention, the first coil and the second coil may have interconnections formed on a same plane and the interconnections be in a vortex form.

In the invention, the spacing between the first coil and the second coil may be controlled by flowing a fluid between the primary coil and the secondary coil.

25 The invention concerns an apparatus for electrically testing a plurality of pixels possessed by a device substrate, the electrical test apparatus comprising:

a primary coil;

means for superposing the primary coil and a secondary coil possessed by the device substrate together through a spacing;

means for superposing an arbitrary part or all of pixel electrodes respectively
5 possessed by the pixels with a testing electrode through a spacing;

means for changing a position of the testing electrode relative to the pixel electrodes possessed by the pixels;

means for applying an alternating current voltage to between two terminals possessed by the primary coil; and

10 means for confirming an operating state of each of the pixels from an alternating current voltage generated on the testing electrode.

The invention concerns an apparatus for electrically testing a plurality of pixels possessed by a device substrate, the electrical test apparatus comprising:

a primary coil;

15 means for superposing the primary coil and a secondary coil possessed by the device substrate through a spacing;

means for changing, while superposing an arbitrary part or all of pixel electrodes respectively possessed by the pixels with a testing electrode through a spacing, a position of the testing electrode relative to the pixel electrodes possessed
20 by the pixels;

means for applying an alternating current voltage to between two terminals possessed by the primary coil; and

means for confirming an operating state of each of the pixels from an alternating current voltage generated on the testing electrode.

25 In the invention, the spacing between the primary coil and the secondary coil may be controlled by flowing a fluid between the primary coil and the secondary

coil.

In the invention, the first coil may have interconnections formed on a same plane and the interconnections be in a vortex form.

The invention concerns a method for manufacturing a semiconductor device
5 comprising:

forming an interconnection or circuit element, and pixel electrode to be supplied with a voltage through the interconnection or circuit element;

applying a voltage to the interconnection or circuit element;

moving a test electrode while superposing an arbitrary part or all of the pixel
10 electrodes through a spacing; and

calculating voltages applied to the pixel electrodes respectively possessed by the pixels due to a voltage applied to each of the pixel electrodes, from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

15 The invention concerns a method for manufacturing a semiconductor device comprising:

forming an interconnection or circuit element, and pixel electrode to be supplied with a voltage through the interconnection or circuit element;

applying, without contact, a voltage to the interconnection or circuit
20 element;

moving a test electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing; and

calculating voltages applied to the pixel electrodes respectively possessed by the pixels due to a voltage applied to each of the pixel electrodes, from a voltage on
25 the testing electrode and a position of the testing electrode relative to the pixel electrodes.

The invention concerns a method for manufacturing a device substrate comprising:

forming an interconnection or circuit element, and pixel electrode to be supplied with a voltage through the interconnection or circuit element;

5 applying a voltage to the interconnection or circuit element;

moving a test electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing; and

calculating voltages applied to the pixel electrodes respectively possessed by the pixels due to a voltage applied to each of the pixel electrodes, from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

The invention concerns a method for manufacturing a device substrate comprising:

forming an interconnection or circuit element, and pixel electrode to be
15 supplied with a voltage through the interconnection or circuit element;

applying, without contact, a voltage to the interconnection or circuit element;

moving a test electrode while being superposed with an arbitrary part or all of the pixel electrodes through a spacing; and

20 calculating voltages applied to the pixel electrodes respectively possessed by the pixels due to a voltage applied to each of the pixel electrodes, from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a top view of a testing substrate of the present invention;

Fig. 2 is a top view of a device substrate of the present invention;

Fig. 3 is a block diagram of the testing substrate and device substrate of the present invention;

5 Figs. 4A and 4B are magnifying views of the coils of the present invention;

Fig. 5 is a perspective view of the testing substrate and device substrate during test of the present invention;

Figs. 6A and 6B are magnifying view of the superposed coils and magnifying view of the superposed pixel electrodes and testing electrodes, respectively, of the present invention;

Fig. 7 is a circuit diagram of the testing substrate and device substrate during test of the present invention;

Figs. 8A and 8B are top views of a testing substrate of the present invention;

15 Fig. 9 is a block diagram of the testing substrate and device substrate of the present invention;

Fig. 10 is a perspective view of the testing substrate and device substrate during test of the present invention;

Figs. 11A and 11B are views showing a manner of superposition between the testing electrodes and the pixel electrodes upon rotating the testing electrodes of the present invention;

Fig. 12 is a view showing a manner of superposition between the pixel electrode possessed by a faulty pixel and the testing electrode of the present invention;

25 Fig. 13 is a block diagram showing a configuration of a test apparatus in Embodiment 1;

Fig. 14 is a block diagram showing a configuration of a testing apparatus in Embodiment 2;

Fig. 15 is a circuit diagram of a signal processing circuit of Embodiment 3;

Fig. 16 is a circuit diagram of a signal processing circuit of Embodiment 4;

5 Fig. 17 is a circuit diagram of a waveform shaper circuit of Embodiment 5;

Fig. 18 is a circuit diagram of a rectifier circuit of Embodiment 6;

Figs. 19A and 19B show a change in time of a pulse signal rectified from an alternating current of Embodiment 6;

10 Figs. 20A-20C show a change in time of a direct current signal generated by adding pulses together of Embodiment 6;

Figs. 21A-21C are circuit diagrams of a rectifier circuit of Embodiment 6;

Fig. 22 is a block diagram of an OLED panel of a light-emitting device of Embodiment 7;

Fig. 23 is a top view of a large-sized substrate of Embodiment 8;

15 Fig. 24 is a top view of a large-sized substrate of Embodiment 8;

Fig. 25 is a flowchart showing a flow of a test process of Embodiment 9;

Figs. 26A and 26B are top and sectional views of coils, respectively, of Embodiment 10; and

20 Fig. 27 is a figure showing an operating state of the pixels based on each function of Embodiment 11.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[Embodiment Mode 1]

Fig. 1 shows a top view of a testing substrate on which test is to be conducted according to the invention using a first structure. Fig. 2 shows a top view of a device

substrate to be tested.

The testing substrate as shown in Fig. 1 has, on a substrate 100, a primary coil formed region 101, an external input buffer 102, a connector connecting part 103 and a testing electrode 104. Note that, in the present description, the testing
5 substrate includes the substrate 100, the primary coil formed region 101, and the other circuits or all the circuit elements formed on the substrate 100.

The primary coil formed region 101 possessed by the testing substrate is not limited in the number and arrangement to the structure shown in Fig. 1. It is possible for a designer to arbitrary determine the number and arrangement of the
10 primary coil formed regions 101.

Although the testing substrate shown in Fig. 1 has test electrodes 104 and primary coil formed region 101, the invention is not limited to such a structure. Testing electrodes may be prepared separately from the testing substrate having a primary coil formed region. By separately providing a testing substrate having a
15 primary coil formed region and testing electrodes, a distance between the testing substrate and the testing electrodes can be determined regardless of the distance of between the primary coil and the secondary coil. Meanwhile, during a test process, the arrangement of testing electrodes can be freely changed relatively to the device substrate.

20 The device substrate shown in Fig. 2 has, on a substrate 110, a signal line drive circuit 111, a scanning line drive circuit 112, a pixel region 113, an extended interconnection 114, a connector connecting part 115, a waveform shaper circuit or rectifier circuit 116 and a secondary coil formed region 117. In the present description, the device substrate includes the substrate 110 and all the circuits or
25 circuit elements formed on the substrate 110. The extended interconnection 114 is an interconnection to supply a drive signal and power voltage to the pixel region

and drive circuit possessed by the device substrate.

Note that the secondary coil formed region 117 of the device substrate is not limited in the number and arrangement to the structure shown in Fig. 2. It is possible for a designer to arbitrary determine the number and arrangement of the
5 secondary coil formed regions 117.

An FPC, TAB or the like is connected to the connector connecting part 115 in the process after a test process. The device substrate after completing a test process is cut along the line A-A' such that the secondary coil formed in the secondary coil formed region 117 is physically and electrically separated from the
10 connector connecting part 115.

Now, explanation will be made on the operation of the device substrate and testing substrate in a test process. In order to facilitate understanding of the signal flow in a test process, the configuration of the device substrate and testing substrate shown in Figs. 1 and 2 is shown in a block diagram of Fig. 3, which will be explained
15 with reference to Figs. 1 and 2.

On a testing substrate 203, a testing alternating current signal is inputted from a signal source 201 or alternating current power source 202 to an external input buffer 102 through a connector connected to the connector connecting part 103. The testing alternating current signal is buffer-amplified in the external input buffer
20 102 and inputted to the primary coil formed region 101.

Although, in Figs. 1, 2 and 3, the input alternating current signal after buffer-amplified in the external input buffer 102 is inputted to the primary coil formed region 101, the invention is not limited to such a structure. An alternating current signal may be directly inputted to the primary coil formed region 101 without
25 providing an external input buffer 102.

A plurality of primary coils are formed in the primary coil formed region 101.

An alternating current signal is inputted to the two terminals of the primary coil.

Meanwhile, in a secondary coil formed region 117 possessed by the device substrate 204, a plurality of secondary coils are formed correspondingly to the primary coils possessed by the primary coil formed region 101. When an alternating
5 current signal is inputted to the primary coil, an alternating current voltage as an electromotive force occurs due to electromagnetic induction at between the two terminals possessed by the secondary coil.

The alternating current voltage generated on the secondary coil is supplied to the waveform shaper circuit 116a or the rectifier circuit 116b. The waveform shaper
10 circuit 116a or rectifier circuit 116b shapes or rectifies the alternating current voltage to generate a drive signal or power voltage.

The generated drive signal voltage or power voltage is supplied to the extended interconnection 114. The provided drive signal voltage or power voltage is supplied to the signal line drive circuit 111, scanning line drive circuit 112 and
15 pixel region 113 through the extended interconnection 114.

The alternating current voltage generated on the secondary coil may be inputted as a drive signal to the pixel region 113 directly instead of through the waveform shaper circuit 116a or rectifier circuit 116b.

The pixel region 113 is formed with a plurality of pixels wherein each pixel is
20 formed with a pixel electrode. The signal line drive circuit and scanning line drive circuit is not limited in the number to that shown in Figs. 1 and 2.

The operation of the signal line drive circuit 111, scanning line drive circuit 112 and pixel region 113 applies a voltage to the pixel electrode of each pixel.

Note that the device substrate as a subject-of-test not necessarily requires drive
25 circuits such as the signal line drive circuit 111 and the scanning line drive circuit 112. Drive signal voltage or power voltage may be applied only to the pixel region

113.

However, it is vital to set a drive signal voltage or power voltage to such a value that the voltage applied to the pixel electrode is given an alternating current voltage.

5 The pixel electrode of a pixel is superposed with the testing electrode 104 through a constant spacing. When the pixel normally operates to apply an alternating current voltage to the pixel electrode, an electromotive force generates on the testing electrode 104. The alternating current voltage, or electromotive force, generated on the testing electrode 104 has a pixel operating state as
10 information. From the alternating current voltage generated on the testing electrode 104, a pixel operating state possessed by the pixel region can be confirmed, to determine a normality/abnormality thereof or specify a faulty point.

Now, explanation will be made on a detailed structure of the primary coil and secondary coil (hereinafter, referred collectively as coil).

15 Fig. 4 shows a magnifying view of the coil. The coil shown in Fig. 4A is in a form having a line depicting a curve of spiral. The coil shown in Fig. 4B is in a form having a line depicting a squared spiral.

Concerning the coil used in the invention, the entire line possessed by the coil is satisfactorily formed on the same plane and the line possessed by the coil is in a
20 spiral form. Accordingly, the line possessed by the coil may depict a curve line or a squared form as viewed vertically to the plane the coil is formed.

It is possible for a designer to appropriately determine a coil with the number of turns, line width and on-substrate area. However, it is required to properly set the number and design of coils to the semiconductor device standard. There is also
25 a necessity to properly set, to the semiconductor device standard, a waveform, frequency and amplitude of an alternating current signal for test to be inputted to

the primary coil formed region.

Fig. 5 shows a perspective view that the device substrate 204 is superposed with the testing substrate 203. Note that shown is the case that the testing substrate 203 shown in Fig. 1 has, as a primary coil, a coil as shown in Fig. 4A while the device substrate shown in Fig. 2 has, as a secondary coil, a coil as shown in Fig. 4A. The connector 205 is connected to the connector connecting part 103.

As shown in Fig. 5, the primary coil formed region 101 possessed by the testing substrate 203 is superposed with the secondary coil formed region 117 possessed by the device substrate 204 through a constant spacing. The spacing is desirably smaller. The primary coil formed region 101 and the secondary coil formed region 117 possessed by the device substrate 204 are preferably as near as possible as long as the spacing is to be controlled.

Meanwhile, the testing electrode 104 and the pixel electrode possessed by the pixel region 113 are superposed together through a constant spacing. The spacing is desirably smaller. The testing electrode 104 and the pixel electrode possessed by the pixel region 113 are preferably as near as possible as long as the spacing is to be controlled.

The spacing between the testing substrate 203 and the device substrate 204 may be maintained by fixing the both substrates. Otherwise, the spacing may be held by fixing either one of the device substrate 204 or the testing substrate 203, to use a constant flow rate or pressure of fluid between the testing substrate 203 and the device substrate 204. The fluid can, representatively, use a gas or a liquid. Besides, a fluid such as a viscous gel can be used.

Fig. 6A shows a magnifying view of a part where the primary coil formed region 101 and the secondary coil formed region 117 are superposed together. 206 shows a primary coil and 207 a secondary coil.

Although in Fig. 6A the primary coil 206 and the secondary coil 207 are the same in direction of line spiral turn, the invention is not limited to that structure. The primary coil and the secondary coil may be reverse in spiral turn direction. Meanwhile, it is possible for a designer to properly set a spacing (L_{gap}) between the
5 primary coil and the secondary coil.

Fig. 6B shows a magnifying view of a part where the pixel electrode 208 possessed by the pixel and the testing electrode 104 are superposed together. In Fig. 6B, one testing electrode 104 is superposed with a plurality of pixel electrodes at the same time. The testing electrode may be formed by one conductive film or by a
10 plurality of electrically connected conductive films.

A capacitance is formed by superposing the testing electrode 104 and the pixel electrode 208 together. When an alternating current voltage is applied to the pixel electrode 208 in a state shown in Fig. 6B, an electromotive force generates on the testing electrode 104.

15 Fig. 7 shows a circuit diagram where superposing together the pixel electrode 208 of the device substrate and the testing electrode 104 of the testing substrate 104. Note that the pixel structure shown in Fig. 7 is a mere one example and hence the number and kind of interconnections and elements possessed by the pixel and their connections are not limited to the configuration shown in Fig. 7. Meanwhile,
20 although Fig. 7 shows a pixel configuration of a light-emitting device, the invention can be applied to other semiconductor devices. Specifically, the test method of the invention can be used to a semiconductor device provided that an alternating current voltage can be applied to the pixel electrode by controlling the application voltage to the interconnection or element.

25 The light-emitting device shown in Fig. 7 has signal lines S1 to Sx in the number of x, power lines V1 to Vx in the number of x, and scanning lines in the

number of y. Each pixel 802 has one signal line, one power line and one scanning line. Furthermore, the pixel 802 has a switching TFT 803, a driving TFT 804 and storage capacitor 805.

806 is a capacitance formed by superposing together the testing electrode 104
5 and the pixel electrode 208.

The switching TFT 803 has a gate electrode connected to any one of the scanning lines G1 to Gy. The switching TFT 803 has source and drain regions one of which is connected to any one of the signal lines S1 to Sx while the other to a gate electrode of the driving TFT 804. The driving TFT 804 has source and drain
10 regions one of which is connected to any one of the power lines V1 to Vx while the other to the pixel electrode.

The storage capacitor 805 has two electrodes connected to the gate electrode of the driving TFT 804 and the power line, respectively.

In the pixel shown in Fig. 7, an alternating current drive signal voltage is being
15 applied to the power line V1 to Vx. Accordingly, in the case the pixel is normal, the switching TFT 803 can be turned on by controlling the voltage applied to the scanning line while the driving TFT 804 can be turned on by controlling the voltage applied to the signal line. As a result, an alternating current drive signal voltage is applied to the pixel electrode.

20 By applying an alternating current drive signal voltage to the pixel electrode, an alternating current voltage generates on the testing electrode 104 overlapped with the pixel electrode. The generated alternating current voltage is supplied as an output 807 to a rear-staged circuit.

In the pixel shown in Fig. 7, the pixel electrodes of the pixels having the same
25 scanning line are superposed with the same testing electrode. However, the testing electrode is not limited to the arrangement form shown in Fig. 7. The pixels having

the pixel electrode overlapped with the testing electrode can be arbitrarily selected. For example, concerning the pixels shown in Fig. 7, the pixel electrodes of the pixels having the same signal line may be connected to the same testing electrode.

The rear-staged circuit, received the output 807, determines a
5 normality/abnormality of the pixel from the alternating current voltage generated on the testing electrode.

According to semiconductor-device drive method or testing-electrode arrangement, there are cases of simultaneously applying a voltage to a plurality of pixel electrodes, superposed with one testing electrode and sequential application
10 and arbitrary application.

Where simultaneously applying an alternating current voltage to a plurality of pixel electrodes, the alternating current voltage generated on the testing electrode differs in waveform between normal operation of all the pixels and not normal operation in at least one of the pixels. Namely, the alternating current voltage
15 generated on the testing electrode possesses, as information, an operating state of all the pixels having these pixel electrodes.

Meanwhile, where alternating current voltages are sequentially applied to a plurality of pixel electrodes, the testing electrode has a sequential addition with alternating voltages each having, as information, an operating state of each pixel.
20 Consequently, where all the pixels are normal, the sequential operation of the pixels provides a monotonous change of the alternating current voltage generated on the testing electrode. Conversely, when any one of the pixels is abnormal, the sequential operation of the pixels provides non-monotonous change in the alternating current voltage generated on the testing electrode. Accordingly, there
25 is difference in alternating current voltage waveform generated on the testing electrode between normal operation of all the pixels and abnormal operation of at

least one of the pixels.

Incidentally, by comparing an alternating current voltage actually generated on the testing electrode with an alternating current voltage generated on the testing electrode of a pixel already confirmed normal, it is possible to confirm an operating
5 state of the pixel and determine a normality/abnormality of the same. However, the alternating current voltage as a reference of comparison is not necessarily based on a pixel already confirmed normal. By comparing between the alternating current voltages respectively generated on testing electrodes, a pixel may be determined for operating state and normality/abnormality. Also, a pixel may be confirmed for
10 operating state and determined for normality/abnormality by comparison with an alternating current voltage value calculated through simulation.

Although in Fig. 7 the testing electrode and the pixel electrodes are superposed together with every pixel possessed by the pixel region, the invention is not limited to that. The testing electrode and the pixel electrode may be superposed
15 only with the arbitrarily selected pixels, to conduct test for an operating state only on the arbitrarily selected pixels.

Although this embodiment mode explained the example that the device substrate has the signal line drive circuit and scanning line drive circuit as a drive circuit, the device substrate to be tested in the invention is not limited to that.
20 Even where the device substrate has a pixel region only, test can be conducted with using the test method of the invention. Meanwhile, for a single device called TEG or evaluation circuit composited with such a single device, it is possible to confirm an operating state by using the test method or apparatus of the invention.

The invention, by the above structure, can determine a normality/abnormality
25 without the use of a probe directly on the interconnection. It is, accordingly, possible to prevent against the yield lowering in the subsequent process due to fine

dust caused upon using a probe. Furthermore, because the a normality/abnormality in all pattern forming processes can be determined by one test process, the test process can be simplified.

[Embodiment Mode 2]

5 Fig. 8 shows a top view of first and second testing substrates to conduct a test according to the invention using a second configuration. Concerning a device substrate to be used in this embodiment, reference can be made to Fig. 2 in Embodiment Mode 1.

10 A first testing substrate shown in Fig. 8A has, on a substrate 6100, a primary coil formed region 6101, an external input buffer 6102 and a connector connecting part 6103 for the first testing substrate. In the description, the first testing substrate includes the substrate 6100, the primary coil formed region 6101 and all the other circuits or circuit elements formed on the substrate 6100. Note that the external input buffer 6102 may not necessarily be provided.

15 The primary coil formed region 6101 possessed by the first testing substrate is not limited in the number and arrangement to the structure shown in Fig. 8A. It is possible for a designer to arbitrary determine the number and arrangement of the primary coil formed regions 6101.

20 A second testing substrate shown in Fig. 8B has, on a substrate 6120, a plurality of testing electrodes 6121 and a connector connecting part 6122 for the second testing substrate. In the description, the second testing substrate includes the substrate 6120, testing electrodes 6121, the connector connecting part 6122 for the second testing substrate and all the other circuits or circuit elements formed on the substrate 6100.

25 The number and arrangement of the testing electrodes 6121 possessed by the

second testing substrate is not limited to the structure shown in Fig. 8B. It is possible for a designer to arbitrarily determine the number and arrangement of the testing electrodes 6121.

Now, explanation will be made on the operation of the device substrate and testing substrate in a test process. In order to facilitate understanding of the signal flow in a test process, the configuration of the device substrate shown in Figs. 8 and 2 and first and second testing substrates is shown in a block diagram of Fig. 9, which will be explained with reference to Figs. 8 and 2.

On the first testing substrate 6203, a testing alternating current signal is inputted from a signal source 201 or alternating current power source 202 to an external input buffer 6102 through a connector connected to the connector connecting part 6103. The testing alternating current signal is buffer-amplified in the external input buffer 6102 and inputted to the primary coil formed region 6101.

Incidentally, in Figs. 2, 8 and 9, the input alternating current signal after buffer-amplified in the external input buffer 6102 is inputted to the primary coil formed region 6101. However, the invention is not limited to this structure. The alternating current signal may be directly inputted to the primary coil formed region 6101 without providing an external input buffer 6102.

A plurality of primary coils are formed in the primary coil formed region 6101. An alternating current signal is inputted to the two terminals of the primary coil.

Meanwhile, in a secondary coil formed region 117 possessed by the device substrate 204, a plurality of secondary coils are formed correspondingly to the primary coils possessed by the primary coil formed region 6101. When an alternating current signal is inputted to the primary coil, an alternating current voltage as an electromotive force generates due to electromagnetic induction at

between the two terminals possessed by the secondary coil.

The alternating current voltage generated on the secondary coil is supplied to the waveform shaper circuit 116a or the rectifier circuit 116b. The waveform shaper circuit 116a or the rectifier circuit 116b shapes or rectifies the alternating current
5 voltage to generate a drive signal or power voltage.

The generated drive signal voltage or power voltage is supplied to the extended interconnection 114. The provided drive signal voltage or power voltage is supplied to the signal line drive circuit 111, scanning line drive circuit 112 and pixel region 113 through the extended interconnection 114.

10 The alternating current voltage generated on the secondary coil may be inputted as a drive signal to the pixel region 113 directly instead of through the waveform shaper circuit 116a or rectifier circuit 116b.

The pixel region 113 is formed with a plurality of pixels wherein the pixel is formed with a pixel electrode. Note that the signal line drive circuit and scanning
15 line drive circuit is not limited in the number to that shown in Figs. 2 and 9.

The operation of the signal line drive circuit 111, scanning line drive circuit 112 and pixel region 113 applies a voltage to the pixel electrode of each pixel.

Note that the device substrate as a subject-of-test not necessarily requires drive circuits such as the signal line drive circuit 111 and the scanning line drive circuit
20 112. The drive signal voltage or power voltage may be applied only to the pixel region 113.

However, it is vital to set a drive signal voltage or power voltage to such a value that the voltage applied to the pixel electrode is given an alternating current voltage.

25 The pixel electrode of a pixel is superposed with the testing electrode 6121 through a constant spacing. When the pixel normally operates to apply an

alternating current voltage to the pixel electrode, an electromotive force generates on the testing electrode 6121. The alternating current voltage, or electromotive force, generated on the testing electrode 6121 has a pixel operating state as information. From the alternating current voltage generated on the testing
5 electrode 6121, an operating state of the pixel possessed by the pixel region can be confirmed, and a normality/abnormality thereof be determined or a faulty point be specified.

Incidentally, the first and second coils used in this embodiment are the same as those of Embodiment 1, and can use coils as shown in Figs. 4A and 4B.

10 Fig. 10 shows a perspective view that the device substrate 204 is superposed with the first testing substrate 6203 and second testing substrate 6205. Note that shown is the case that the first testing substrate 6203 shown in Fig. 8A has, as a primary coil, a coil as shown in Fig. 4A while the device substrate shown in Fig. 2 has, as a secondary coil, a coil as shown in Fig. 4A. The connector 6209 is
15 connected to the connector connecting part 6103 for the first testing substrate. Meanwhile, the connector 6210 is connected to the connector connecting part 6122 for the second testing substrate.

As shown in Fig. 10, the primary coil formed region 6101 possessed by the first testing substrate 6203 and the secondary coil formed region 117 possessed by the
20 device substrate 204 are superposed together through a constant spacing. The spacing is desirably smaller. The primary coil formed region 6101 and the secondary coil formed region 117 possessed by the device substrate 204 are preferably as near as possible as long as the spacing is to be controlled.

Meanwhile, the testing electrode 6121 possessed by the second testing
25 substrate 6205 and the pixel electrode possessed by the pixels of the pixel region 113 are superposed together through a constant spacing. The spacing is desirably

smaller. The testing electrode 6121 and the pixel electrode possessed by the pixels of the pixel region 113 are preferably as near as possible as long as the spacing is to be controlled.

The spacing between the first testing substrate 6203 and the device substrate 204 may be maintained by fixing the both substrates. Otherwise, the spacing may be held by fixing either one of the device substrate 204 or the first testing substrate 6203, to use a constant flow rate or pressure of fluid between the first testing substrate 6203 and the device substrate 204. The fluid can, representatively, use a gas or a liquid. Besides, a fluid such as a viscous gel can be used.

Similarly to Embodiment Mode 1, the primary coil and the secondary coil may be the same or opposite in direction of line spiral turn. Meanwhile, it is possible for a designer to properly set a spacing (L_{gap}) between the primary coil and the secondary coil. As for a manner of superposition between the primary coil and the secondary coil, reference can be made to Fig. 6A in Embodiment Mode 1.

Meanwhile, similarly to Embodiment Mode 1, one testing electrode 6121 is simultaneously superposed with a plurality of pixel electrodes. The testing electrode may be formed by one conductive film or by a plurality of electrically connected conductive films. As for a manner of superposition between the testing electrode and the pixel electrode, reference can be made to Fig. 6B in Embodiment Mode 1. A capacitance is formed by superposition of the testing electrode 6121 and the pixel electrode 208. When an alternating current voltage is applied to the pixel electrode 208, an electromotive force generates due to electrostatic induction on the testing electrode 6121.

Incidentally, in this embodiment mode, the pixel electrode 208 superposed with the testing electrodes 6121 is arbitrary in position. Furthermore, the positional relationship of the testing electrodes 6121 and the pixel electrodes 208 differs from

monitor to monitor.

Concerning a circuit diagram of upon superposing together the pixel electrode 208 of the device substrate and the testing electrode 6121 of the second testing substrate, reference can be made to Fig. 7 of Embodiment Mode 1. Note that, in the pixels shown in Fig. 7, the pixel electrodes of the pixels having the same scanning line are superposed with the same testing electrode. However, the testing electrode is not limited to the arrangement shown in Fig. 7. It is possible to arbitrary select the pixels having pixel electrodes superposed with the testing electrode.

Explanation is made on the positional relationship of between the testing electrodes 6121 and the pixel electrodes 208 during monitoring.

The designer is allowed to arbitrarily set the number of times of monitoring an alternating current voltage generated on the testing electrode 6121. The designer is also allowed to arbitrarily set the positional relationship between the testing electrodes 6121 and the pixel electrodes 208 during each monitor. It is, however, vital to fix a positional relationship for monitoring between the testing electrodes 6121 and the pixel electrodes 208 and set the number of times of monitoring so that an operating state on each pixel can be determined from the value of an alternating current voltage on the testing electrode 6121 obtained through all of monitoring.

Figs. 11A and 11B show a positional relationship of between the pixel electrodes 208 and the testing electrodes 6121 when the testing electrode 6121 is rotated, about a center of the pixel region as the center axis, on a plane parallel with a plane forming the pixel electrode 208. Explanation is herein made on an example having pixel electrodes in the number of 5 x 5 in the pixel region in order for easy understanding the explanation.

Fig. 11A shows a state prior to rotation (0°) wherein the pixel electrode 208,

every five, is superposed with the testing electrode 6121.

Fig. 11B shows a state that the testing electrodes 6121 are rotated 45 degrees counterclockwise about the center of the pixel region from the state of Fig. 11A. In this case, the testing electrode 6121 is superposed with a different pixel electrode
5 208 from that of Fig. 11A.

The alternating current voltage generated on each testing electrode 6121 differs in its amplitude and waveform depending upon the number of pixel electrodes superposed with the testing electrode 6121, an area of superposition with the pixel electrodes, and a value of an alternating current voltage applied to the
10 pixel electrode.

It is possible to previously calculate the number of pixel electrodes to be superposed with the testing electrode 6121 and the area of superposition with the pixel electrodes. It is also possible to previously obtain, by calculation or actual measurement, an amplitude and waveform of an alternating current voltage to be
15 applied to the pixel electrode where all the pixels are in normal operation.

Consequently, in the case that, for example, as shown in Fig. 12, a pixel electrode 208a of a poor pixel is included in the pixel electrodes 208 superposed with the testing electrode 6121, the amplitude and waveform of an alternating current voltage generated on the testing electrode 6121 is different from the case
20 all the pixels are in normal operation.

As the occupation ratio of the pixel electrodes of poor pixels to the pixel electrodes 208 superposed with the testing electrodes 6121 is higher, the amplitude and waveform of an alternating current voltage generated on the testing electrode 6121 departs from the case all the pixels are in normal operation. Consequently, it
25 is possible to calculate an occupation ratio of normally operating pixels of among the pixels whose pixel electrodes are superposed with one testing electrode 6121.

Furthermore, because the testing electrode 6121 is changed, plurality of times, in position relative to the pixel electrodes 208, it is possible to obtain an occupation ratio of normally operating pixels of among the pixels whose pixel electrodes are superposed with one testing electrode 6121. From the occupation ratio of normally
5 operating pixels obtained in each position of the testing electrode 6121, an operating state can be determined on a pixel-by-pixel basis. From the operating state, a normality/abnormality can be determined.

Incidentally, the simultaneous voltage application to a plurality of pixel electrodes superposed with one testing electrode includes sequential and arbitrary
10 applications depending upon semiconductor-device drive method and testing-electrode arrangement.

In the case of simultaneously selecting and operating a plurality of pixels, the alternating current voltage generated on the testing electrode differs in waveform between upon normal operation of all the pixels and not normal operation of at
15 least one of the pixels. Namely, the alternating current voltage generated on the testing electrode possesses, as information, an operating state of all the pixels.

Meanwhile, where sequentially selecting and operating a plurality of pixels, the testing electrode is generated with sequential addition of alternating current voltages each having, as information, an operating state of each pixel. Accordingly,
20 where sequentially operating a plurality of pixels normal in the all, monotonous is a change rate of an alternating current voltage generated on the testing electrode with respect to the overlap area of between the pixel electrodes of operative pixels and the testing electrode.

Conversely, where sequentially operating a plurality of pixels including an
25 abnormal pixel, not monotonous is a change rate of an alternating current voltage generated on the testing electrode with respect to the overlap area of between the

pixel electrodes of operative pixels and the testing electrode. Accordingly, the alternating current voltage generated on the testing electrode is different in waveform between upon normal operation of all the pixels and not normal operation of at least one of the pixels.

5 Incidentally, it is possible to confirm an operating state of a pixel and determine a normality/abnormality thereof by comparing between an alternating current voltage to be generated on the testing electrode in the case of using the pixels already confirmed normal and an alternating current voltage actually generated on the testing electrode. However, the alternating current voltage as a
10 reference of comparison must not be on the pixel already confirmed normal. By comparing between alternating current voltages generated on a plurality of testing electrodes, a pixel may be confirmed for its operating state and determined for its normality/abnormality. In this case, it is vital to compare them by taking into consideration the area of the pixel electrodes superposed with the testing electrode.
15 Meanwhile, by comparison with an alternating current voltage value calculated due to simulation, a pixel may be confirmed for its operating state and determined for a normality/abnormality thereof.

 Incidentally, although in Figs. 7, 11A and 11B the testing electrode and the pixel electrode are superposed together at all the pixels possessed by the pixel
20 section, the invention is not limited to that. The testing electrode and the pixel electrode may be superposed together at only arbitrarily selected pixels, to conduct a test for an operating state at only the arbitrarily selected pixels.

 Although this embodiment mode explained the example that the device substrate had a signal line drive circuit and scanning line drive circuit as a driving
25 circuit, the device circuit to be tested in the invention is not limited to that. Where the device substrate has a pixel region only, it is possible to conduct a test by the use

of the test method of the invention. Meanwhile, for a single device called TEG or evaluation circuit composited with such a single device, it is possible to confirm an operating state by using the test method or apparatus of the invention.

Note that the testing electrode may be directly controlled and moved without
5 fixing the testing electrode on a substrate.

The invention, by the above structure, can determine a normality/abnormality of the device substrate without the use of a probe directly on the interconnection. It is, accordingly, possible to prevent against the yield lowering in the subsequent process due to fine dust caused upon using a probe. Furthermore, because the
10 normality/abnormality in all the pattern forming processes can be determined by one test process, the test process can be simplified.

Now, explanations will be made on the embodiments of the present invention.

[Embodiment 1]

15 This embodiment explains a configuration of a test apparatus for confirming an operating state of pixels and determining a normality/abnormality thereof by comparing between alternating current voltages generated on a plurality of testing electrodes in Embodiment 1.

Fig. 13 shows a block diagram of a configuration of a test apparatus of this
20 embodiment.

A measurement start instruction is inputted as information from a man-machine I/F 305 to a measuring controller 306. The measuring controller 306 inputs an instruction to control the position of a device substrate 302 and testing substrate 301 as subjects-of-test, as information, to a handler I/F 307 in order to
25 start a measurement. The handler I/F 307 superposes together a pixel electrode

(not shown) possessed by the device substrate 302 and a testing electrode 303 possessed by the testing substrate 301, through a constant spacing.

The measuring controller 306 inputs a measurement start instruction, as information, to a measuring sequencer 308. Thereupon, the measuring sequencer 308 controls a panel display sequencer 309 to select a position of a pixel of a subject-of-test, and inputs the position, as information, from the panel display sequencer 309 to a coil driver 310. An RF carrier 311, having a signal source and alternating current power source, can supply an alternating current voltage to a rear-staged circuit. The measuring sequencer 308 controls the RF carrier 311 to input an alternating current voltage to the coil driver 310.

The coil driver 310 uses the input alternating current voltage to supply an external input buffer 311 with an alternating current voltage for operating the pixel of a subject-of-test. The external input buffer 311 buffer-amplifies the supplied alternating current voltage and provides it to a primary coil formed region 304.

By providing the primary coil formed region 304 with the alternating current voltage, the pixel of a subject-of-test possessed by the device substrate 302 operates. The alternating current voltage is applied to the pixel electrode of that pixel. Incidentally, the operation of the device substrate of upon providing an alternating current voltage to the primary coil formed region was concretely explained in the embodiment modes and hence omittedly explained herein.

When the alternating current voltage is applied to the pixel electrode, an alternating current voltage generates on a testing electrode 303 superposed with the pixel electrode. The alternating current voltage generated on the testing electrode 303 includes, as information, an operating state of the same pixel.

The alternating current voltage generated on the testing electrode 303 is provided to a signal processing circuit 312. The signal processing circuit 312

operates a value of the alternating current voltage generated on each testing electrode. Specifically, calculated is a difference between alternating current voltages on the respective testing electrodes. The alternating current voltage generated on the testing electrode 303 differs in waveform depending on an
5 operating state of the pixel. For this reason, the calculated difference of alternating current voltage includes, as information, an operating state of the pixel. Consequently, the signal having, as information, a calculated difference of alternating current voltage (operating information signal) includes, as information, an operating state of the pixel. The operation information signal is inputted to a
10 selector circuit 313.

The alternating current voltage generated on the testing electrode often includes various noises. The noise caused on the testing electrode, having comparatively near frequency and voltage, can be removed to a certain extent by calculating a difference in value between the alternating current voltages generated
15 on the testing electrodes. The frequency and voltage of the noise is nearer as the testing electrodes are closer in position to each other. Consequently, it is preferred to calculate a difference of alternating current voltage between the testing electrodes closer in position to each other.

The selector circuit 313 is supplied, through the measuring sequencer 308,
20 with the positional information of a pixel selected by the panel display sequencer 309. The selector circuit 313 inputs an operation information signal corresponding to the selected pixel of among a plurality of input operation information signals, to a signal analyzer 314.

The signal analyzer 314 amplifies the input operation information signal and
25 then A/D-converts it into a digital form, followed by operation processing. Note that the A/D conversion is not necessarily required and the operation process may

be by analog. The operation process is carried out in order to analyze an operating state of the pixel. Accordingly, it is possible for a designer to properly select a content of the operation process.

The operation information signal, after the operation process, is inputted to
5 the measuring controller 306. The measuring controller 306 specifies a pixel state from the operation-processed operation information signal and further determines a normality/abnormality of the pixel.

Incidentally, the light-emitting device of the invention is not limited to the configuration shown in Fig. 13. It is satisfactory for the light-emitting device to
10 have means to generate an alternating current voltage, means to supply voltage, without contact, to an interconnection and circuit element of the device substrate, means to read, without contact, a voltage applied to the pixel electrode of the device substrate, and means to control a position of the device substrate. Furthermore, it is satisfactory to specify a pixel state from an alternating current
15 voltage read, without contact, and to determine a normality/abnormality of the pixel.

⋮
⋮
⋮

[Embodiment 2]

This embodiment explains a configuration of a test apparatus for confirming an operating state of pixels and determining a normality/abnormality thereof by the
20 use of alternating current voltages generated on a plurality of testing electrodes in Embodiment 2.

Fig. 14 shows a block diagram of a configuration of a test apparatus of this embodiment.

A measurement start instruction is inputted as information from a man-
25 machine I/F 6305 to a measuring controller 6306. The measuring controller 6306

inputs a handler I/F 6307 with an instruction to control the position of a device substrate 6302 as subject-of-test, first testing substrate 6301 and second testing substrate 6315, as information, in order to start a measurement.

5 The handler I/F 6307 superposes together a secondary coil formed region (not shown) possessed by the device substrate 6302 and a primary coil formed region 6304 possessed by the first testing substrate 6301, through a constant spacing. Meanwhile, the handler I/F 6307 superposes together a pixel electrode (not shown) possessed by the device substrate 6302 and a testing electrode 6303 possessed by the second testing substrate 6315, through a constant spacing.

10 The measuring controller 6306 inputs a measurement start instruction, as information, to a measuring sequencer 6308. Thereupon, the measuring sequencer 6308 controls a panel display sequencer 6309 to select a position of a pixel of a subject-of-test, and inputs the position, as information, from the panel display sequencer 6309 to a coil driver 6310. An RF carrier 6311, having a signal source
15 and alternating current power source, can supply an alternating current voltage to a rear-staged circuit. The measuring sequencer 6308 controls the RF carrier 6311 to input an alternating current voltage to the coil driver 6310.

The coil driver 6310 uses the input alternating current voltage to supply an external input buffer 6311 with an alternating current voltage for operating the
20 pixel of a subject-of-test. The external input buffer 6311 buffer-amplifies the supplied alternating current voltage and provides it to the primary coil formed region 6304.

By providing the primary coil formed region 6304 with the alternating current voltage, the pixel of a subject-of-test possessed by the device substrate 6302
25 operates. The alternating current voltage is applied to the pixel electrode of the same pixel.

When the alternating current voltage is applied to the pixel electrode, an alternating current voltage generates on a testing electrode 6303 being superposed with the pixel electrode. The alternating current voltage generated on the testing electrode 6303 includes, as information, an operating state of the same pixel.

5 The alternating current voltage generated on the testing electrode 6303 is provided to a signal processing circuit 6312. The signal processing circuit 6312 operates a value of the alternating current voltage generated on each testing electrode. Specifically, calculated is a difference of occurred alternating current voltage of between the testing electrodes. The alternating current voltage generated
10 on the testing electrode often includes various noises. The noise caused on the testing electrode, having comparatively near frequency and voltage, can be removed to a certain extent by calculating a difference between the alternating current voltages generated on the testing electrodes. The frequency and voltage of the noise is nearer as the testing electrodes are closer in position to each other.
15 Consequently, it is preferred to calculate a difference of alternating current voltage between the testing electrodes closer in position to each other.

Incidentally, the alternating current voltage generated on the testing electrode 6303 differs in waveform depending on an operating state of the pixel. For this reason, the calculated difference of alternating current voltage includes, as
20 information, an operating state of the pixel. Consequently, the signal having, as information, a calculated difference of alternating current voltage (operating information signal) includes, as information, an operating state of the pixel. The— operation information signal is inputted to a selector circuit 6313.

The selector circuit 6313 is supplied, through the measuring sequencer 6308,
25 with the information of a position of a pixel selected by the panel display sequencer 6309, position of a pixel electrode being superposed with each testing electrode

6303 and ratio of an area of superposition. The selector circuit 6313 inputs an operation information signal corresponding to the selected pixel of among a plurality of input operation information signals, to a signal analyzer 6314.

The signal analyzer 6314 amplifies the input operation information signal and
5 then A/D-converts it into a digital form, followed by operation processing. Incidentally, the A/D conversion is not necessarily required, and the operation process may be by analog. The operation process is carried out in order to analyze an operating state of the pixel being superposed with the testing electrode during monitoring. Accordingly, it is possible for a designer to properly select a content of
10 the operation process.

The operation information signal, after the operation process, is inputted to the measuring controller 6306.

Then, the handler I/F 6307 changes the position of the second testing substrate 6315 relative to the device substrate 6302. The foregoing operation is
15 repeated plurality of times to input a plurality of operation information signals operation-processed to the measuring controller 6306. The measuring controller 6306 specifies a state of each pixel and determines a normality/abnormality of the pixel from the position and ratio in area of a pixel electrode superposed with each testing electrode during monitoring and the input operation information signal
20 operation-processed.

Note that the test apparatus of the invention is not limited to the configuration shown in Fig. 14. The test apparatus of the invention satisfactorily
has means to generate an alternating current voltage, means to supply voltage, without contact, to an interconnection and circuit element of the device substrate,
25 means to read, without contact, a voltage applied to the pixel electrode of the device substrate, and means to control a position of the device substrate.

Furthermore, it is satisfactory to specify a pixel state from an alternating current voltage read, without contact, and further to determine a normality/abnormality of the pixel.

[Embodiment 3]

5 This embodiment explains a detailed configuration of a signal processing circuit of the test apparatus shown in Fig. 13. Note that the signal processing circuit of the test apparatus shown in Fig. 14 may have a configuration shown in this embodiment. }

Fig. 15 shows a circuit diagram of a signal processing circuit of this
10 embodiment. The signal processing circuit 312 shown in Fig. 15 has a plurality of differential amplifiers 350_1 to 350_y-1 corresponding to testing electrodes 303 (E1 to Ey) in the number of y.

The alternating current voltages generated on the testing electrodes are respectively inputted to non-inverted inputs (+) of the differential amplifiers. To
15 an inverted input (-) of each differential amplifier is applied an alternating current generated on the testing electrode different from the testing electrode corresponding to the non-inverted input (+).

In this embodiment, the voltage of an alternating current generated on the testing electrode Ei (i = any one of 1 to y - 1) is provided to the non-inverted input
20 (+) of the differential amplifier 350_i. The voltage of an alternating current generated on the testing electrode Ei+1 (i = any one of 1 to y - 1) is provided to a second terminal of the differential amplifier 350_i+1.

Each differential amplifier inputs an operation information signal, as an output, to the rear-staged selector circuit 313. An operating state of a pixel superposed with
25 each testing electrode can be confirmed from the operation information signal

outputted from the differential amplifier. Specifically, an operating state of a pixel can be confirmed from a value or waveform of a voltage possessed by the operation information signal. However, the pixel superposed with the testing electrode E_v can be confirmed in its operating state from an operation information signal outputted
5 from the differential amplifier 350_{y-1}. Meanwhile, a dummy testing electrode may be prepared to provide an alternating current voltage generated on the testing electrode E_y to a non-inverted input (+) of a separately provided differential amplifier and a voltage of the dummy testing electrode to the second terminal. Furthermore, a dummy pixel, not for use in actual display but for the purpose of test,
10 may be provided in the pixel region so that the dummy pixel can be superposed with the dummy testing electrode.

The operating state of a pixel superposed with the testing electrode E_1 is included, as information, in an operation information signal outputted from the differential amplifier 350₁. The operating state of a pixel superposed with the
15 testing electrode E_j ($j = 2$ to $y - 1$) is included, as information, in an operation information signal outputted from the differential amplifiers 350_{j-1} and 350_j. The operating state of a pixel superposed with the testing electrode E_y is included, as information, in an operation information signal outputted from the differential amplifier 350_{y-1}.

20 Incidentally, it is possible for a designer to properly set a criterion as to whether a pixel is considered not normally operating depending upon what degree the operating state of the pixel differs from the normal operating state of the normal pixel.

Note that the signal processing circuit to be used in the invention is not
25 limited to the configuration shown in Fig. 15.

This embodiment can be implemented in free combination with Embodiment

1 or 2.

[Embodiment 4]

This embodiment explains a detailed configuration of a signal processing circuit of the test apparatus shown in Fig. 13. Note that the signal processing circuit of the test apparatus shown in Fig. 14 also may have a configuration shown in this
5 embodiment.

Fig. 16 shows a circuit diagram of a signal processing circuit of this embodiment. } The signal processing circuit 312 shown in Fig. 16 has, correspondingly to testing electrodes 303 (E1 to Ey) in the number of y, a plurality
10 of primary induction coils 360_1 to 360_y - 1, a plurality of secondary induction coils 361_1 to 361_y - 1 and a plurality of capacitances 362_1 to 362_y-1.

The primary and secondary induction coils of this embodiment (referred collectively to as induction coils) may each be or not be provided, at a center, with a magnetic member. Meanwhile, the interconnections possessed by the induction
15 coils may be or not be on the same plane.

The alternating current voltages generated on the testing electrodes are respectively inputted to first terminals of the primary induction coils. To a second terminal of each primary induction coil is applied an alternating current generated on the testing electrode different from the testing electrode corresponding to the
20 first terminal.

In this embodiment, the voltage of an alternating current generated on the testing electrode Ei (i = any one of 1 to y - 1) is provided to the first terminal of the primary induction coil 360_i. The voltage of an alternating current generated on the testing electrode Ei+1 (i = any one of 1 to y - 1) is provided to a second
25 terminal of the primary induction coil 360_i+1.

The primary induction coils 360₁ to 360_{y - 1} and the secondary induction coils 361₁ to 361_{y - 1} are respectively superposed together. The capacitances 362₁ to 362_{y - 1} are respectively formed between the first and second terminals of the secondary induction coils 361₁ to 361_{y - 1}.

5 The voltages generated on the first terminals of the secondary induction coils 361₁ to 361_{y - 1} are all applied, as operation information signal voltages, to the selector circuit 313. A constant voltage (ground voltage in Fig. 16) is provided to all the second terminals of the secondary induction coils 361₁ to 361_{y - 1}.

10 An operating state of a pixel superposed with each testing electrode can be confirmed from the operation information signal generated on the first terminal of the secondary induction coil. However, the pixel superposed with the testing electrode E_y can be confirmed in its operating state from an operation information signal generated on the first terminal of the secondary induction coil 361_{y - 1}.

15 Meanwhile, a dummy testing electrode may be prepared to provide an alternating current voltage generated on the testing electrode E_y to a first terminal of a separately provided primary induction coil and a voltage of the dummy testing electrode to the second terminal of the primary induction coil. An operating state of same can be confirmed from an operation information signal generated on the first terminal of a separately provided secondary induction coil. Furthermore, a
20 dummy pixel, not for use in actual display but for the purpose of test, may be provided in the pixel region so that the dummy pixel can be superposed with the dummy testing electrode.

25 The operating state of a pixel superposed with the testing electrode E₁ is included, as information, in an operation information signal generated on the first terminal of the secondary induction coil 361₁. The operating state of a pixel superposed with the testing electrode E_j ($j = 2$ to $y - 1$) is included, as information,

in an operation information signal generated on the first terminal of the secondary induction coil 361_j - 1 and first terminal of the secondary induction coil 361_j. The operating state of a pixel superposed with the testing electrode E_y is included, as information, in an operation information signal generated on the first terminal
5 of the secondary induction coil 361_y - 1.

It is possible for a designer to properly set a criterion as to whether a pixel is considered not normally operating depending upon what degree the operating state of the pixel differs from the normal operating state of the pixel.

Note that the signal processing circuit to be used in the invention is not
10 limited to the configuration shown in Fig. 16.

This embodiment can be implemented in free combination with Embodiment 1 or 2.

[Embodiment 5]

15 This embodiment explains a detailed configuration of the waveform shaper circuit in Embodiment Mode 1, with using Fig. 17. Note that the waveform shaper circuit of Embodiment Mode 2 also may have a configuration shown in this embodiment.

Fig. 17 shows a form of connection of between the signal source 201, the
20 primary coil formed region 101, the secondary coil formed region 117 and the waveform shaper circuit 116a that were shown in Fig. 3. The primary coil formed region 101 is provided with a plurality of primary coils 206. The secondary coil formed region 117 is provided with a plurality of secondary coils 207.

Each primary coil 206 is inputted with a testing alternating current signal from
25 the signal source 201. Specifically, a testing alternating current signal voltage is applied from the signal source 201 to between two terminals possessed by the

primary coil 206. When an alternating current signal is inputted to the primary coil 206, an alternating current voltage, or electromotive force, is generated on the corresponding secondary coil 207. The alternating current voltage is applied to the waveform shaper circuit 116a.

5 The waveform shaper circuit 116a is an electronic circuit used to form or shape a waveform of a quantity varying in time, i.e. voltage or current. Fig. 17 has resistances 501, 502 and capacitors 503, 504 to constitute an integration-type waveform shaper circuit 116a by the combination of the circuit elements. The waveform shaper circuit, of course, is not limited to the configuration shown in Fig.
10 17. Meanwhile, similarly to the power source circuit, a wave-detecting circuit using diodes may be used to shape waveforms.

The waveform shaper circuit 116a used in the invention generates and outputs, specifically, a clock signal (CLK), a start pulse signal (SP) or a video signal from an input alternating current electromotive force.

15 The waveform shaper circuit 116a can generate a signal in an arbitrary form without limited to the above signals. The signal to be generated by the waveform shaper circuit 116a is satisfactorily a signal for confirming an operating state of the pixel.

The signal output from the waveform shaper circuit 116a is inputted to the
20 rear-staged circuits, e.g. signal line drive circuit 111, scanning line drive circuit 112 and pixel region 113.

—This embodiment can be implemented in free combination with Embodiments 1 to 4.

[Embodiment 6]

25 This embodiment explains a detailed configuration of the rectifier circuit 116b

in Embodiment Mode 2, with using Fig. 18. Note that the rectifier circuit of Embodiment Mode 2 also may have a configuration shown in this embodiment.

Fig. 18 shows a form of connection of between the alternating current power source 202, the primary coil formed region 101, the secondary coil formed region 117 and the rectifier circuit 116b that were shown in Fig. 3. The primary coil formed region 101 is provided with a plurality of primary coils 206. The secondary coil formed region 117 is provided with a plurality of secondary coils 207.

Each primary coil 206 is inputted with a testing alternating current signal from the alternating current power source 202. When an alternating current signal is inputted to the primary coil 206, an alternating current voltage, or electromotive force, is generated on the corresponding secondary coil 207. The alternating current voltage is applied to the rectifier circuit 116b.

Note that the rectifier circuit in the invention means a circuit to generate a direct current power voltage from a supplied alternating current voltage. The direct current power voltage means a voltage kept at a constant height to be provided to a circuit, circuit element or pixel.

The rectifier circuit 116b shown in Fig. 18 has diodes 601, a capacitor 602 and a resistance 603. The diode 601 is to rectify an input alternating current voltage and converts it into a direct current voltage.

Fig. 19A shows a change in time of an alternating current voltage prior to rectification in the diode 601. Fig. 19B shows a change in time of the voltage after rectification. As can be seen from the comparison between the graphs of Figs 19A and 19B, the voltage after rectified takes zero or a value having one polarity at an interval of a half period, so-called a pulse voltage.

The pulse voltage shown in Fig. 19B is difficult in use as a power voltage. Consequently, usually the pulse is smoothened and converted into a direct current

voltage by being stored on a capacitor. However, in order to form a capacitor with a large capacity sufficient for smoothening the pulse by the use of a thin-film semiconductor, there is a need to impractically greatly increasing the area of a capacitor. Accordingly, the invention, after rectification, combines (adds) together
5 the pulse voltages different in phase thereby smoothening the voltage. The above configuration can sufficiently smoothen the pulse even where the capacitor is small in capacitance. Furthermore, the pulse can be sufficiently smoothened without positively providing a capacitor.

In Fig. 18, alternating current signals different in phase are respectively input
10 to four primary coils thereby outputting four pulse voltages different in phase from four diodes 601. The four pulse voltages are added together to form a direct current power voltage having a height maintained nearly constant that is to be outputted to the rear-staged circuit.

Although Fig. 18 formed a power voltage by adding together the four pulse
15 signals different in phase outputted from the four diodes 601, the invention is not limited to this configuration. The number of phase division is not limited to this. The number of phase division is not limitative provided that the output from the rectifier circuit is smoothened to such an extent that is usable as a power voltage.

Figs. 20A-20C show a change in time of a power voltage obtained by adding
20 together a plurality of rectified signals. Fig. 20A shows an example that one power voltage is generated by adding together four pulse voltages different in phase.

Because the rectifier circuit of the invention generates a voltage by adding a plurality of pulses together, the voltage has ripple as a component other than a direct current. Ripple corresponds to a difference between the highest voltage and
25 the lowest voltage. As the ripple is smaller, the voltage generated in the rectifier circuit nears a direct current and is easier to use as a power voltage.

Fig. 20B shows a change in time of a power voltage obtained by adding together eight pulse voltages different in phase. It can be seen that ripple is smaller as compared to the time change of power voltage shown in Fig. 20A.

Fig. 20C shows a change in time of a power voltage obtained by adding
5 together sixteen pulse voltages different in phase. It can be seen that ripple is further smaller as compared to the time change of power voltage shown in Fig. 20B.

In this manner, it can be seen that the power voltage is reduced in ripple into a direct current by adding together a multiplicity of pulses mutually different in
10 phase. Accordingly, as the number of phase division increases, the power voltage outputted from the rectifier circuit is easier to be smoothened. Also, as the capacitance of the capacitor 602 increases, the power voltage outputted from the rectifier circuit is easier to be smoothened.

The power voltage generated in the rectifier circuit 116b is outputted through
15 the terminals 610 and 611. Specifically, a voltage approximate to the ground is outputted through the terminal 610 while a power voltage having a positive polarity is outputted through the terminal 611. By connecting the diode reverse at the anode and cathode, the output power voltage can be inverted in polarity. The diode 602 connected to the terminals 610 and 611 is connected reverse at the anode and
20 cathode to the diode 601 connected to the terminals 612 and 613. Accordingly, a voltage approximate to the ground is outputted through the terminal 612 while a power voltage having a negative polarity is outputted through the terminal 613.

Incidentally, various circuits or circuit elements are formed on the device substrate. The power voltage to be supplied to the circuit or circuit element differs
25 in height depending upon the kind or application of the circuit or circuit element. In the rectifier circuit shown in Fig. 18, the voltage to be inputted to each terminal

can be adjusted in height by adjusting the amplitude of an input alternating current signal. Furthermore, the height of power voltage can be changed by changing the terminal connected.

The rectifier circuit used in the invention is not limited to the half-wave
5 rectifier circuit shown in Fig. 18. The rectifier circuit used in the invention may be a circuit capable of generating a direct current power supply from an input alternating current signal.

Figs. 21A-21B show circuit diagrams of rectifier circuits having configurations of other than that shown in Fig. 18. The rectifier circuit shown in Fig. 21A is a
10 voltage doubler full-wave rectifier circuit 901 having two diodes 902 and 903. Also, the voltage doubler full-wave rectifier circuit shown in Fig. 21A has capacitors 904 and 905. The position and number of capacitors is not limited to the showing in Fig. 21A.

The cathode of the diode 902 and the anode of the diode 903 are both
15 connected to one terminal of a secondary coil. By providing a plurality of voltage doubler full-wave rectifier circuits 901 to add together the outputs thereof, it is possible to obtain a direct current voltage twice as compared to that of a half-wave rectifier circuit shown in Fig. 18.

The rectifier circuit shown in Fig. 21B is a bridge rectifier circuit 911 having
20 four diodes 912, 913, 914 and 915. The four diodes 912, 913, 914 and 915 form a bridge. Meanwhile, the bridge rectifier circuit shown in Fig. 21B has a capacitor 916. The position and number of capacitors is not limited to that shown in Fig. 21B.

This embodiment can be implemented in free combination with Embodiments
25 1 to 5.

[Embodiment 7]

This embodiment explains the testing drive signals and power voltage with greater detail by exemplifying a case with the general light-emitting device.

Fig. 22 shows a configuration of an OLED panel for the general light-emitting device. Note that Fig. 22 explains an example of a drive circuit for a light-emitting device to display an image by use of digital video signals. The OLED panel shown in Fig. 22 has a signal line drive circuit 700, a scanning line drive circuit 701 and a pixel region 702.

The pixel region 702 is formed with a plurality of signal lines, a plurality of scanning lines and a plurality of power lines. The region surrounded by the signal line, the scanning line and the power line corresponds to a pixel. Note that Fig. 22 shows representatively only a pixel having one signal line 707, one scanning line 709 and one power line 708 of among the pixels in plurality. Each pixel has a switching TFT 703 as a switch element, a drive TFT 704, a storage capacitor 705 and an OLED pixel electrode 706.

The switching TFT 703 has a gate electrode connected to the scanning line 709. The switching TFT 703 has source and drain regions one of which is connected to the signal line 707 while the other is to the gate electrode of the drive TFT 704.

The driving TFT 704 has source and drain regions one of which is connected to the power line 708 while the other is to a pixel electrode 706. The gate electrode of the drive TFT 704 and the power line 708 form a storage capacitor 705. Note that the storage capacitor 705 may not necessarily be formed.

The signal line drive circuit 700 has a shift register 710, a first latch 711 and a second latch 712. The shift register 710, the first latch 711 and the second latch 712 are each given with power supply. Meanwhile, the shift register 710 is given

with a clock signal (S-CLK) and start pulse signal (S-SP) for the signal line drive circuit. The first latch 711 is given with a latch signal to determine the timing of latch and a video signal.

When a clock signal (S-CLK) and start pulse signal (S-SP) is inputted to the
5 shift register 710, a sampling signal is generated to determine the timing of sampling video signals and inputted to the first latch 711.

The sampling signal from the shift register 710, after buffer-amplified by a buffer or the like, may be inputted to the first latch 711. The interconnection onto which a sampling signal is inputted is connected with many circuits or circuit
10 elements and hence great in load capacitance (parasitic capacitance). The buffer is effective for preventing against the "blunt" of rise or fall in the timing signal caused due to great load capacitance.

The first latch 711 has a plurality of stages of latches. The first latch 711 samples an input video signal in synchronism with an input sampling signal, and
15 stores it in the sequence of latch to each stage.

Referred to as a line period is a time required to write a video signal to all the staged latches of the first latch 711. Actually, the line period, in some cases, includes the line period added with a horizontal return period.

After terminating one line period, a latch signal is inputted to the second latch
20 712. At this instance, the video signal written and held on the first latch 711 is sent at once to the second latch 712, and written to and held on all the staged latches of the second latch 712.

The first latch 711 having sent the video signal to the second latch 712 is sequentially written by a video signal depending upon a sampling signal from the
25 shift register 710.

In the second line period, the video signal written and held on the second

latch 712 is inputted onto the source signal line.

On the other hand, the scanning line drive circuit 701 has a shift register 721 and a buffer 722. The shift register 721 and the buffer 722 are given with a power supply. Meanwhile, the shift register 721 is given with a clock signal (G-CLK) and
5 start pulse signal (G-SP) for the scanning line drive circuit.

The power line 708 is applied with an alternating current voltage.

When a clock signal (G-CLK) and start pulse signal (G-SP) is inputted to the shift register 721, a select signal for determining the timing of scanning line selection is generated and inputted to the buffer 722. The select signal inputted to the buffer
10 722 is buffer-amplified and inputted to the scanning line 709.

The selection of the scanning line 709 turns on the switching TFT 703 connected at its gate electrode to the selected scanning line 709. The video signal inputted to the signal line is inputted to the gate electrode of the driving TFT 704 through the switching TFT 703 turned on.

15 The driving TFT 704 is controlled in its switching on the basis of the information 1 or 0 possessed by the video signal inputted to the gate electrode. When the driving TFT 704 is on, an alternating current voltage on the power line is provided to the pixel electrode. When the driving TFT 704 is off, the alternating current voltage on the power line is not provided to the pixel electrode.

20 In this manner, when the signal line drive circuit 700, scanning line drive circuit 701 and pixel region 702 operate, an alternating current voltage is applied to the pixel electrode whereby an alternating current voltage including the operation information of the pixel generates on the testing electrode 730. Pixel operation information is confirmed and pixel normality/abnormality is determined
25 on the basis of the alternating current voltage generated on the testing electrode 730.

Furthermore, even where a faulty generates on the drive circuit but there is no defect in the pixel, the voltage applied to the pixel electrode varies in value. Accordingly, it is possible to determine a normality/abnormality of the drive circuit.

5 In the case of the OLED panel shown in Fig. 22, S-CLK, S-SP, G-CLK, G-SP, latch signal and video signal are inputted as testing drive signals to the circuits. Note that the testing drive signals are not limited to the above signals. Any drive-related signal can be used as a testing drive signal. For example, besides the foregoing signals, inputted may be a signal to determine a timing of switching a
10 scanning direction on the scanning line or a signal to switch an input direction of a select signal to the scanning line. However, it is vital to input such a signal as can confirm an operating state of a pixel to be tested or can determine a normality/abnormality thereof.

In the case of testing part of the pixels possessed by the OLED panel instead
15 of testing the all thereof, it is satisfactory to input only such a drive signal as to drive only the part of the pixels. There is no need to always input all of the foregoing drive signals.

Note that, where a power voltage is generated by adding together pulse signals different in phase, the number of primary coils differs depending upon the number
20 of pulse signals to be added.

The test apparatus and method of the invention is not limited to the OLED panel having the configuration shown in Fig. 22.

This embodiment can be implemented in free combination with Embodiments 1 to 6.

25 [Embodiment 8]

This embodiment explains on cutting a substrate of after test to form a plurality of display substrate by the use of a large-sized substrate.

Fig. 23 shows a top view of a large-sized substrate before cut in this embodiment. 1001 is a pixel region, 1002 is a scanning line drive circuit, and 1003 is a signal line drive circuit. Also, the region shown at 1004 is formed with the circuits or circuit elements to be used only in a test process but not used after completing the test, i.e. a plurality of secondary coils, waveform shaper circuits, rectifier circuits, exclusive test circuit and so on.

In Fig. 23, by cutting the substrate along the line shown at the dotted line, nine display substrates are formed from one substrate. Incidentally, although this embodiment shows the example to form nine display substrates from one substrate, this embodiment is not limited to this number.

Note that cutting is made to physically, electrically disconnect the secondary coil and connector during cutting. In Fig. 23, the region 1004 is provided on the side of a substrate not to be used for display after cutting.

Explanation is made, as to how to cut the large-sized substrate, on an embodiment different from Fig. 23. In Fig. 24, 1101 is a pixel region, 1102 is a scanning line drive circuit, and 1103 is a signal line drive circuit. The region shown at 1104 is formed with the circuits or circuit elements to be used only in a test process but not used after completing the test, i.e. a plurality of secondary coils, waveform shaper circuits, rectifier circuits, exclusive test circuit and so on.

In Fig. 24, by cutting the substrate along the line shown at the dotted line, nine display substrates are formed from one substrate. Incidentally, although this embodiment shows the example to form nine display substrates from one substrate, this embodiment is not limited to this number.

Note that cutting and breaking is made to physically, electrically disconnect

the secondary coil and connector during cutting. In Fig. 24, the region 1104 is provided on a cut line of the substrate, and cut and broken after test. Because the circuit or circuit element formed in the region 1104 is not necessary after test, no trouble occurs in operating a completed semiconductor device.

- 5 The waveform shaper circuit or the rectifier circuit, after cut, may be left on the substrate to be used as a semiconductor device or on the substrate not to be used as a semiconductor device. Otherwise, the circuit, after cut, may be broken.

This embodiment can be implemented in free combination with the configurations of Embodiments 1 to 7.

10 [Embodiment 9]

This embodiment explains the operation sequence in the test process of the invention, by using a flowchart.

- Fig. 25 shows a flowchart of a test process of the invention. First, after completing the fabrication process prior to test, testing power voltage or drive signal voltage is applied, without contact, to a circuit element or interconnection of the device substrate.
- 15

- As a result, the pixel as a subject-of-test makes a certain operation to generate an alternating current voltage having the information of a pixel operating state on the testing electrode superposed with the pixel. The alternating current voltage is monitored plurality of times while changing the position of the testing electrode.
- 20

- On the basis of the alternating current voltage generated on the testing electrode, a pixel operating state is confirmed and a pixel normality/abnormality is determined. Incidentally pixel operating state is not necessarily screened into two of normality and abnormality but may be screened into a plurality of ranks based on the operating state.
- 25

Meanwhile, it is possible for a practitioner to properly set a determination criterion as to pixel normality/abnormality. In the case there are some pixels determined abnormal, the practitioner is allowed to properly set whether to determine the device substrate unacceptable or not. It is possible to determine abnormal where there is even one abnormal pixel, or otherwise, it is possible to determine abnormal where there are a constant number of abnormal pixels.

In the case of determining normal, the test is considered ended at that time to commence a fabrication process of after the test process.

Where determined abnormal, selection is made for removal from the process not to complete as a product (lot out) or to specify a cause of abnormality. Note that, where a plurality of products are to be fabricated from a large-sized substrate, lot-out will be entered after cutting the substrate.

Where a cause of abnormality is specified and repair is determined possible, the test process of the invention can be again made after repair to repeat the foregoing operation. Conversely, when repair is determined impossible, lot-out is entered at that time.

This embodiment can be implemented in free combination with the configurations of Embodiments 1 to 8.

[Embodiment 10]

This embodiment explains in detail the connection between a coil used in the invention, a terminal possessed by the coil and an interconnection (coil interconnection).

In Fig. 26A, a coil 1601 is formed on an insulation surface and an interlayer insulation film 1603 is formed covering the coil 1601 on the insulation surface. A contact hole is formed in the interlayer insulation film, to form on the interlayer

insulation film a coil interconnection 1602 connecting to the coil 1601 through the contact hole.

Fig. 26B is a sectional view taken on the broken line C-C' in Fig. 26A.

In Fig. 26C, a coil interconnection 1612 is formed on an insulation surface.

- 5 An interlayer insulation film 1613 is formed covering the coil interconnection 1612 on the insulation surface. A contact hole is formed in the interlayer insulation film, to form on the interlayer insulation film a coil 1611 connecting to the coil interconnection 1612 through the contact hole.

Fig. 26D is a sectional view taken on the broken line D-D' in Fig. 26C.

- 10 Note that the manufacturing method for a coil used in the invention is not limited to the above method. By patterning an insulation film, a vortex groove is formed. A conductive film is formed covering the groove on the insulation film. Thereafter, the conductive film is polished by etching or CMP process until the insulation film is exposed to thereby leave the conductive film only in the groove.
- 15 The conductive film left in the groove can be used as a coil.

This embodiment can be implemented in free combination with the configurations of Embodiments 1 to 8.

[Embodiment 11]

- This embodiment explains a method to conduct a test as to whether each pixel
- 20 normally operates or not, by the use of a Walsh function, in Embodiment Mode 1.

- This embodiment explains with an example in the case of a light-emitting device having 4 x 4 pixels. For the light-emitting device having 4 x 4 pixels, determined are sixteen function groups of $W_{00}(4, 4)$ to $W_{33}(4, 4)$ (hereinafter, abbreviated W_{00} to W_{33}) in the number of 16.
- 25

Fig. 27 concretely shows the position of pixels operated by the use of the function groups W_{00} to W_{33} . Note that the pixel shown white and the pixel shown with hatching are different in value of the voltage applied to the pixel electrode thereof.

5 In the case of operating the pixels in order by using the function group W_{00} to W_{33} in the order, the pixels in the number of 4×4 are different in operation one another. Consequently, even where the testing electrode is superposed with pixel electrodes based on the pixels having the same scanning line, test can be conducted as to whether each pixel is in normal operation or not.

10 Consideration is made to the pixels on the first line, for example. In the pixel (1, 1), provided that the case the pixel is shown white is denoted O while the case the pixel is shown by hatching is denoted X, the showing is with O in all the cases. The pixel (2, 1), for example, is shown as O O X X O O X X O O X X O O X X in the order. The pixel (3, 1) is shown as O X X O O X X O O X X O O X X O in the order. The pixel
15 (4, 1) is shown as O X O X O X O X O X O X O X in the order.

When all the pixels normally operate, the number of O in the pixels on the first line based on each function is expressed as 4, 2, 2, 2, 4, 2, 2, 2, 4, 2, 2, 2, 4, 2, 2, 2 in the order. When, for example, the pixel (2, 1) does not normally operate to make display as shown by hatching at all times, the number of O in the pixels on the
20 first line based on each function is expressed as 3, 1, 2, 2, 3, 1, 2, 2, 3, 1, 2, 2, 3, 1, 2, 2 in the order. Accordingly, by comparing the case all the pixels normally operate, the pixel (2, 1) can be presumed not in normal operation.

Although this embodiment used the Walsh function in the two dimensions, the pixels may be operated by using the Walsh function in one dimension. In this
25 case, in the foregoing light-emitting device having the 4×4 pixels, it is possible to test an operating state by the use of four function groups.

This embodiment can be implemented in free combination with the configurations of Embodiments 1 to 9.

The invention, by the above structure, can determine a normality/abnormality of a pixel as a subject-of-test without the use of a probe directly on an
5 interconnection or probe terminal. It is accordingly possible to prevent against the yield lowering in the later process due to the fine dust caused upon using a probe. Furthermore, because the normality/abnormality in every pattern forming process can be determined by one test process, the test process can be simplified.

WHAT IS CLAIMED IS:

1. A method of measuring a voltage comprising:

applying a voltage to an interconnection or circuit element in a pixel
without contact to thereby apply a voltage to a pixel electrode of the pixel; and
5 reading the voltage applied to the pixel electrode without contact.

2. A method of measuring a voltage comprising:

applying a voltage to interconnections or circuit elements respectively in
a plurality of pixels to thereby apply voltages to pixel electrodes respectively of the
pixels without contact; and

10 reading a sum of the voltages applied to the pixel electrodes respectively
of the pixels without contact.

3. A method of measuring a voltage comprising:

applying a first alternating current voltage to between two terminals of
a first coil;

15 superposing the first coil and a second coil together through a constant
spacing;

applying a third alternating current voltage to a pixel electrode of a pixel
by using a second alternating current voltage generated between two terminals of
the second coil;

20 superposing the pixel electrode and a testing electrode together through
a constant spacing; and

calculating the voltage applied to the pixel electrode from a fourth
alternating current voltage generated on the testing electrode.

4. A method according to claim 3,

wherein the third alternating current voltage is applied to the pixel electrode of the pixel by rectifying or waveform-shaping the second alternating current and applying to an interconnection or circuit element in the pixel.

5 5. A method of measuring a voltage comprising:

applying a first alternating current voltage to between two terminals of a first coil;

superposing the first coil and a second coil together through a constant spacing;

10 applying a third alternating current voltage to pixel electrodes respectively of a plurality of pixels by using a second alternating current voltage generated between two terminals of the second coil;

superposing the pixel electrodes of the pixels and a testing electrode together through a constant spacing; and

15 calculating a sum of voltages applied to the pixel electrodes respectively of the pixels from a fourth alternating current voltage generated on the testing electrode.

6. A method according to claim 5,

20 wherein the third alternating current voltage is applied to the pixel electrodes respectively of the plurality of pixel by rectifying or waveform-shaping the second alternating current and applying to interconnections or circuit elements respectively in the plurality of the pixels.

7. A method according to claim 3 or 5,

wherein the first coil and the second coil have interconnections formed on a same plane, and

wherein each of the interconnections is formed in a vortex form.

8. A method according claim 3 or 5,

5 wherein the first coil and the testing electrode are formed on a first insulation surface,

wherein the second coil and the pixel electrode are formed on a second insulation surface.

9. A method according to claim 8,

10 wherein a spacing between the first insulation surface and the second insulation surface is controlled by flowing a fluid between the first insulation surface and the second insulation surface.

10. A method according to claim 3 or 5,

15 wherein the pixel or each of the pixels is determined for a normality/abnormality by using a voltage applied to the pixel electrode or a sum thereof obtained using the voltage measuring method.

11. An apparatus for electrically testing pixels in a semiconductor device, the electrical test apparatus comprising:

a primary coil;

20 means for superposing the primary coil and a secondary coil in the semiconductor device together through a constant spacing;

means for superposing a pixel electrode of the pixel and a testing

electrode together through a constant spacing;

means for applying an alternating current voltage to between two terminals of the primary coil; and

means for confirming an operating state of the pixel from an alternating
5 current voltage generated on the testing electrode.

12. An apparatus according to claim 11,

whereby the alternating current voltage generated on the testing electrode includes an operating state of the pixel as information.

13. An apparatus according to claim 11,

10 wherein the spacing between the primary coil and the secondary coil is controlled by flowing a fluid between the primary coil and the secondary coil.

14. An apparatus according to claim 11,

wherein the first coil has an interconnection formed on a same plane,

and

15 wherein the interconnection is formed in a vortex form.

15. A method for manufacturing a semiconductor device comprising:

forming a pixel electrode and an interconnection or circuit element;

applying a voltage to the interconnection or circuit element without contact to thereby applying a voltage to the pixel electrode; and

20 reading the voltage applied to the pixel electrode without contact.

16. A method for manufacturing a semiconductor device comprising:

forming a pixel electrode, an interconnection or circuit element, a first coil and a second coil;

applying a first alternating current voltage to between two terminals of the first coil;

5 superposing the first coil and the second coil together through a constant spacing;

applying a third alternating current voltage to the pixel electrode by using a second alternating current voltage generated between two terminals of the second coil; }

10 superposing the pixel electrode and a testing electrode together through a constant spacing; and

calculating the voltage applied to the pixel electrode from a fourth alternating current voltage generated on the testing electrode.

17. A method according to claim 16,

15 wherein the third alternating current voltage is applied to the pixel electrode by rectifying or waveform-shaping the second alternating current voltage and applying to the interconnection or circuit element.

18. A method of measuring a voltage comprising:

20 applying a voltage to an interconnection or circuit element for controlling a voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with at least part of the pixel electrodes through a spacing; and

calculating a voltage applied to each of the pixel electrodes from a voltage on the testing electrode and a position of the testing electrode relative to

the pixel electrodes.

19. A method according to claim 18,
wherein the voltage is applied to the interconnection or circuit element
without contact.

5 20. A method of measuring a voltage comprising:
 applying a first alternating current voltage to between two terminals of
a first coil; }
 superposing the first coil and a second coil together through a spacing;
 applying a second alternating current voltage generated between two
10 terminals of the second coil to an interconnection or circuit element for controlling
a voltage to be applied to a plurality of pixel electrodes;
 moving a testing electrode while being superposed with at least a part of
the pixel electrodes through a spacing; and
 calculating a voltage applied to each of the pixel electrodes from a third
15 alternating current voltage generated on the testing electrode and a position of the
testing electrode relative to the pixel electrodes.

21. A method according to claim 20,
wherein the second alternating current is applied to the interconnection
or circuit element by rectifying or waveform-shaping the second alternating current
20 voltage and applying to the interconnection or circuit element.

22. A method according to claim 20,
wherein the first coil and the second coil have interconnections formed

on a same plane, and

wherein each of the interconnections is formed in a vortex form.

23. A method according to claim 20,

wherein the spacing between the first coil and the second coil is
5 controlled by flowing a fluid between the first coil and the second coil.

24. A method according to claim 18 or 20,

wherein the voltage on each of the pixel electrodes is calculated using a
Fourier transformation method using successive approximation and projection
section theorem or a superposition integration method.

10 25. An electrical test method comprising:

applying a voltage to an interconnection or circuit element for
controlling a voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with at least a part of
the pixel electrodes through a spacing; and

15 confirming an operating state of the interconnection or circuit element
from a voltage on the testing electrode and a position of the testing electrode
relative to the pixel electrodes.

26. A method according to claim 25,

wherein the voltage is applied to the interconnection or circuit element
20 without contact.

27. An electrical test method comprising:

applying a voltage to an interconnection or circuit element for
controlling a voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with at least a part of
the pixel electrodes through a spacing; and

5 determining a distribution of a voltage to be applied to the pixel
electrodes from a voltage on the testing electrode and a position of the testing
electrode relative to the pixel electrodes.

28. A method according to claim 27,

wherein the voltage is applied to the interconnection or circuit element
10 without contact.

29. A method according to claim 27, further comprising:

confirming an operating state of the interconnection or circuit element
from the voltage distribution.

30. An electrical test method comprising:

15 applying a first alternating current voltage to between two terminals of
a first coil;

superposing the first coil and a second coil together through a spacing;

applying a second alternating current voltage generated between two
terminals of the second coil to an interconnection or circuit element for controlling
20 a voltage to be applied to a plurality of pixel electrodes;

moving a testing electrode while being superposed with at least part of
the pixel electrodes through a spacing; and

confirming an operating state of the interconnection or circuit element

from a third alternating current voltage generated on the testing electrode and a position of the testing electrode relative to the pixel electrodes.

31. A method according to claim 30, further comprising:

determining a distribution of a voltage to be applied to the pixel
5 electrodes from the third alternating current voltage,

wherein the operating state of the interconnection or circuit element is confirmed from the voltage distribution.

}

32. A method according to claim 30,

wherein the second alternating current voltage is applied to the
10 interconnection or circuit element by rectifying or waveform-shaping and applying to the interconnection or circuit element.

33. A method according to claim 30,

wherein the first coil and the second coil have interconnections formed on a same plane, and

15 wherein each of the interconnections is in a vortex form.

}

34. A method according to claim 30,

wherein the spacing between the first coil and the second coil is controlled by flowing a fluid between the primary coil and the secondary coil.

35. An apparatus for electrically testing a plurality of pixels in a device

20 substrate, the electrical test apparatus comprising:

a primary coil;

means for superposing the primary coil and a secondary coil in the device substrate together through a spacing;

means for superposing at least a part of pixel electrodes respectively of the pixels with a testing electrode through a spacing;

5 means for changing a position of the testing electrode relative to the pixel electrodes of the pixels;

means for applying an alternating current voltage to between two terminals of the primary coil; and

means for confirming an operating state of each of the pixels from an
10 alternating current voltage generated on the testing electrode.

36. An apparatus according to claim 35,

wherein while superposing the part of the pixel electrodes respectively of the pixels with the testing electrode through the spacing, the position of the testing electrode relative to the pixel electrodes of the pixels is changed.

15 37. An apparatus according to claim 35,

wherein the spacing between the primary coil and the secondary coil is controlled by flowing a fluid between the primary coil and the secondary coil.

38. An apparatus according to claim 35,

20 wherein the first coil has an interconnection formed on a same plane, and

wherein the interconnection is formed in a vortex form.

39. A method for manufacturing a semiconductor device comprising:

forming an interconnection or circuit element, and pixel electrode to be supplied with a voltage through the interconnection or circuit element;

applying a voltage to the interconnection or circuit element;

moving a testing electrode while superposing at least a part of the pixel electrodes through a spacing; and

calculating voltages applied to the pixel electrodes respectively of the pixels due to a voltage applied to each of the pixel electrodes, from a voltage on the testing electrode and a position of the testing electrode relative to the pixel electrodes. }

10 40. A method according to claim 39,

wherein the voltage is applied to the interconnection or circuit element without contact.

41. A method according to claim 39,

wherein the semiconductor device includes a device substrate.