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(54) IMPROVEMENTS IN OR RELATING TO THIN FILM CIRCUITS

(71) We, HEWLETT-PACKARD COMPANY, a corporation organised and existing under the laws of the State of California, United States of America, of 1501 Page Mill Road, Palo Alto, California, United States of America, do hereby declare the invention, for which we pray that a Patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention is concerned with improvements in or relating to thin film circuits.

The fabrication of electronic circuitry wherein resistors and capacitors and their interconnections are formed by thin-film techniques is growing rapidly in importance. With thin-film technology, complex circuits having precision capacitors and resistors may be tailored to meet specific circuit design requirements, resulting in microcircuitry of reduced size, weight, and cost and increased reliability. One form of thin-film circuit, along with the method of manufacture, is disclosed in United States Patent No. 3,616,282 issued on October 26, 1971 to George E. Bodway, entitled METHOD OF PRODUCING THIN-FILM CIRCUIT ELEMENTS.

One typical process for the manufacture of thin-film resistor-capacitor circuits of the type shown in U.S. Patent No. 3,616,282 comprises the following steps, performed sequentially:

1. Forming the under-electrodes of the various capacitors on an insulating substrate by
 - (a) sputtering a layer of conductive metal such as tantalum (Ta) over the surface of the substrate,
 - (b) forming a mask on the metal layer by a known photo-resist technique, and
 - (c) etching through the mask to remove all the metal except for the desired capacitor under-electrodes and interconnections therebetween that serve to provide a single common electrical path for all the capacitor under-

electrodes during a subsequent anodizing step;

2. Forming a dielectric layer over a portion of the surface of each of the capacitor under-electrodes by
 - (a) depositing an oxide layer over the entire surface of the substrate, capacitor under-electrodes, and interconnections, such as for example, by a silicon dioxide (SiO₂) deposition,
 - (b) forming a mask on the oxide layer by the photo-resist technique,
 - (c) etching through the mask to remove the oxide layer from areas of the capacitor under-electrodes to be anodized,
 - (d) electrochemically anodizing the exposed portions of the capacitor under-electrodes in an appropriate electrolyte for an appropriate period of time to form the desired dielectric layer (for example, Ta₂O₅) of each capacitor under-electrode, and
 - (e) removing the anodizing mask by an oxide etch, leaving the partially anodized under-electrodes and the interconnections therebetween;
3. Removing the interconnections between the capacitor under-electrodes by
 - (a) forming a mask by the photoresist technique leaving the interconnections exposed, and
 - (b) etching away the interconnections;
4. Forming the various resistors on the substrate by
 - (a) sputtering a layer of resistive material such as tantalum nitride (Ta₂N) over the entire surface of the substrate and capacitor electrodes,
 - (b) depositing a first layer of conductive material such as chrome gold (CrAu), which adheres well to the resistive layer, over the resistive layer,
 - (c) forming a mask, which covers those areas of the structure where the resistors are to remain, by the photo-resist technique and

- (d) etching away the exposed first conductive layer and the underlying resistive layer, leaving the desired resistors;
- 5 5. In order to increase the yield of these circuits, depositing an additional oxide layer on the dielectric (Ta_2O_5) layer of each capacitor under-electrode to cure pinholes therein and other imperfections produced therein during the various fabrication steps performed after the anodizing step, such as during the oxide etching step of (2)e above and the resistive layer sputtering step of 4(a) above (this step is performed, for example, by depositing a layer of silicon dioxide (SiO_2) over the structure with a value of .055 pf/mil² $\pm$ 5% for the combined Ta_2O_5 and SiO_2 layers).
- 10 6. Forming the upper-electrodes of the various capacitors by
- 15 (a) depositing a second layer of conductive material such as chrome gold (CrAu) over the entire surface of the structure,
- 20 (b) forming a mask which covers those areas of the structure where the capacitor upper-electrodes and the underlying additional oxide layer are to remain by the photoresist technique, and
- 25 (c) etching away the exposed second conductive layer and then the underlying additional oxide layer, leaving the desired capacitor upper-electrodes;
- 30 7. Complete the upper-electrodes of the various capacitors and forming the interconnections between the various capacitors and resistors by
- 35 (a) depositing a third layer of conductive material such as chrome gold (CrAu) over the entire surface of the structure,
- 40 (b) forming a mask on the third conductive layer by the photo-resist technique to define the capacitor upper-electrodes and interconnections,
- 45 (c) plating a thick layer (.30—.40 mils) of gold to form the interconnections, and
- 50 (d) etching away the second and then the third conductive layers where not covered by the thick gold interconnections.
- 55 It is noted that, in the above process, certain difficult steps are performed. For example, the masking and anodizing steps of 2(b), (c), and (d) above are troublesome since, during anodizing, the mask has to withstand 200 volts in an electrolytic bath, and the mask oftentimes breaks down.
- 60 Other difficult steps in the process are the interconnection masking and etching steps of 3(a) and (b) above. Still other difficult steps in the process are the masking and etching steps of 6(b) and (c), particularly since the mask formed must be pinhole free to prevent pinholes from being etched in the capacitor dielectric layers. The etching step of 6(c) requires the use of a silicon dioxide in forming the additional oxide layer, since it is difficult or impossible to etch other forms of oxide layers, and only silicon dioxide has been found to be satisfactory.
- 70 Since a photoresist mask alone is not capable of withstanding the oxide etch needed to form the capacitors in the etching step of 6(c), the layer of CrAu deposited during the step of 6(a) is needed to serve as a mask, and thus the two layers of CrAu deposited during the steps of 6(a) and 7(a) and the two subsequent CrAu etching steps of 6(c) and 7(d) are needed.
- 75 Also, where silicon oxide layers are selectively etched and remaining portions thereof are subsequently gold plated through a masking, there is a tendency for an undesirable gold bead to form around the upper edges of the masked portions of the oxide layers, the mask being unable to adequately protect these edges.
- 80 Because of the high temperatures involved in the SiO_2 deposition step of 5 above, it is necessary that the first layer of CrAu deposited in the step of 4(b) above be fairly thick, so as not to be deleteriously affected by diffusion of chrome therefrom due to the heat. Consequently the etching step of 4(d) above is lengthened resulting in less than optimum resistor definition.
- 85 The above process requires seven masking steps, and the trips between the photoresist masking stages and the subsequent deposition and etching stages result in an overall fabrication period of approximately three weeks.
- 90 It is an object of the present invention to provide an improved structure, for example an integrated circuit structure, for use in forming thin film capacitors and resistors and interconnections thereto on a substrate.
- 95 It is another object of the present invention to provide a method of manufacturing a structure, for example an integrated circuit structure, as referred to in the last preceding paragraph.
- 100 The present invention provides a structure for use in forming thin film capacitors and resistors and interconnections thereto on a substrate, the structure comprising a substrate of insulating material; a plurality of metallic film elements provided on said substrate, the metallic film elements having oxidized upper surfaces; a dielectric layer extending over the substrate and the oxidized upper surfaces of said plurality of metallic film elements; a layer of resistive material extending over said dielectric layer; and a layer of
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conductive material extending over said layer of resistive material.

5 Preferably each of said metallic film elements is made of tantalum and has a tantalum pentoxide upper surface, and the resistive material is tantalum nitride; alternatively each of said metallic film elements is made of hafnium and has a hafnium oxide upper surface, and the resistive material is tantalum nitride.

10 The present invention further provides a method of manufacturing a structure for use in forming thin film capacitors and resistors and interconnections thereto, the method comprising the steps of forming a plurality of metallic film elements on a surface of a substrate, forming an oxidized upper surface on each of the metallic film elements, forming a dielectric layer over the substrate surface and the oxidized upper surfaces of the metallic film elements, forming a layer of resistive material over the dielectric layer, and forming a layer of conductive material over the layer of resistive material.

25 Preferably each of the metallic film elements is made of tantalum and has a tantalum pentoxide upper surface, and the resistance material is tantalum nitride, alternatively each of the metallic film elements is made of hafnium having a hafnium oxide upper surface, and the resistive material is tantalum nitride.

30 In carrying out a method as set forth in either one of the last two preceding paragraphs, preferably the steps of forming an oxidized upper surface on each of the metallic film elements comprises forming a common interconnecting circuit for electrically interconnecting the metallic film elements so that the upper surfaces of the metallic film elements may be simultaneously electrochemically anodized, anodizing electrochemically the upper surfaces of the metallic film elements to form the oxidized upper surfaces, and there-after disconnecting the interconnecting circuit from between the metallic film elements; more preferably each interconnecting circuit is formed between the metallic film elements and the edge of the substrate, and disconnection of the interconnecting circuit is accomplished by severing a peripheral portion of the substrate.

35 The present invention further provides a method of manufacturing an integrated circuit structure including interconnected thin film capacitors and resistors, the method comprising the steps of forming a plurality of metallic film elements on a surface of a substrate, forming an oxidized upper surface on each of the metallic film elements, forming a dielectric layer over the substrate surface and the oxidized upper surfaces of the metallic film elements, forming a layer of resistive material over the dielectric layer, forming a first layer of conductive material

over the layer of resistive material, forming connections of a second layer of conductive material on the first layer of conductive material to define desired electrical connections for the resistors and capacitors, removing areas of both the first conductive layer and the resistive layer to expose the surface of the dielectric layer to define the resistors and to form the capacitors and the electrical connections for the resistors and capacitors, and removing selected portions of the first conductive layer to expose the underlying layer of resistive material to thereby form the resistors.

70 Preferably the step of removing areas of both the first conductive layer and the resistive layer further comprises the step of removing portions of both the first conductive layer and the layer of resistive material to define a dimension of each resistor before forming connection of a second layer of conductive material.

75 In carrying out a method as set forth in either one of the last two preceding paragraphs, preferably the step of forming the oxidized upper surfaces on the metallic film elements comprises anodizing the metallic film elements.

80 In carrying out a method as set forth in any one of the last three preceding paragraphs, preferably each of the metallic film elements is made of tantalum and has a tantalum pentoxide upper surface.

85 Preferably the resistive material is made of tantalum nitride.

90 Preferably the dielectric layer is made of a material comprising an oxide of silicon; more preferably the oxide of silicon is silicon dioxide.

95 Preferably the step of forming an oxidized upper surface on each of the metallic film elements comprises forming a common interconnecting circuit for electrically interconnecting the metallic film elements so that the metallic film elements may be electrochemically anodized simultaneously, electrochemically anodizing the upper surfaces of the metallic film elements to form the oxidized upper surfaces, and thereafter disconnecting the interconnecting circuit from between the metallic film elements. Preferably the interconnecting circuit is formed between the metallic film elements and the edge of the substrate, and disconnection of the interconnecting circuit is accomplished by severing a peripheral portion of the substrate.

100 Preferably the sheet resistivity of the layer of resistive material is lower than the ultimate resistivity desired and the method comprises the further step of heating the substrate for a first period of time to stabilize the layer of resistive material and heating the substrate for a second period of time to increase the resistivity of the layer of resistive material and trim the resistors to the desired ultimate

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value. More preferably a plurality of resistors of different values is formed, the sheet resistivity of all of the resistors being lower than the ultimate resistivity desired, and the
5 step of heating the substrate for the second period of time further comprises determining the length of time of heating needed to bring the first of the resistors up to its maximum permissible final value, determining the
10 length of time of heating needed to bring the last of the resistors to its minimum permissible final value, and the heating of said substrate for a period of time falling between said two extremes to thereby trim
15 all resistors to a value lying within their permissible limits.

The present invention further provides an integrated circuit structure including at least one thin-film capacitor and resistor, the
20 integrated circuit structure comprising: a substrate of insulating material; at least one metallic film element on a surface of the substrate, the metallic film element having an oxidized upper surface; a dielectric layer over
25 the oxidized upper surface of the metallic film element and the surface of the substrate; a resistive layer over a portion of the dielectric layer; a pair of spaced apart capacitor plates, each capacitor plate comprising a conductive layer on a portion of the
30 dielectric layer, the pair of capacitor plates being situated above the metal film element and defining a capacitor therebetween; and a pair of resistor terminals, each resistor terminal comprising a conductive layer on a
35 portion of the dielectric layer, the pair of resistor terminals being in contact with and separated by a portion of the resistive layer and defining a resistor therebetween.

40 Preferably a structure as set forth in the last preceding paragraph includes a first conductive layer on a portion of the resistive layer; and a second conductive layer on the first conductive layer, the capacitor plates
45 and resistor terminals comprising a portion of the resistive layer, the first conductive layer and the second conductive layer.

50 Preferably in a structure as set forth in either one of the last two preceding paragraphs interconnections are provided between selected ones of the resistor terminals and capacitor plates, the interconnections comprising a portion of the resistive layer, the first conductive layer and the second conductive layer attached to the selected ones of
55 the resistor terminals and capacitor plates.

60 Preferably the dielectric layer extends entirely over the surface of the substrate and the oxidized upper surface of the metallic film element and is made of silicon dioxide.

65 Preferably the metallic film element is a tantalum film element and the oxidized upper surface of the metallic film element is a layer of tantalum pentoxide.

There now follows a detailed description

which is to be read with reference to the accompanying drawings of a number of structures and methods according to the present invention, it is to be clearly understood that these have been selected for description to illustrate the invention by way of example and not by way of limitation.

In the drawings:

Figure 1 is a schematic diagram of a thin film resistor and capacitor structure made in accordance with a preferred embodiment of the present invention.

Figure 2 is a top view of the thin film structure of Figure 1 in an early stage of its fabrication.

Figure 3 is a cross-sectional side view of the thin film structure of Figure 2 taken along section line 3—3 therein.

Figure 4 is a top view of the thin film structure of Figure 1 in an advanced stage of its fabrication.

Figure 5 is a cross-sectional side view of the thin film structure of Figure 4 taken along section line 5—5 therein.

Figure 6 is a similar cross-sectional side view of the thin film structure of Figure 4 in a still later stage of its fabrication.

Figure 7 is a curve illustrating the relationship between resistance value and heat treatment time for the resistors formed in the thin film structure of Figure 1.

In order to more clearly describe the present invention, the step-by-step construction of a simple amplifier circuit shown in Figure 1 will be described in detail. This simple circuit comprises a transistor T1 coupled to a thin film resistor-capacitor structure comprising three resistors R1, R2, and R3 and five capacitors C1 through C5.

Referring now to Figures 2 and 3, the main body or support for the structure comprises a substrate 11 of good insulating material, such as sapphire, glass or ceramic, and of a suitable size, such as 1/2 inch wide, 1 inch long, and 25 mils thick. After proper cleaning, the upper surface of the substrate is deposited with a layer of good electrical conducting material on which a dielectric oxide layer may be anodically formed. This layer is preferably beta tantalum or hafnium of suitable thickness, for example 7,000 to 9,000 Å. Other suitable materials include aluminum, niobium, titanium and zirconium. This layer may be deposited by a number of suitable processes including cathodic sputtering and vacuum deposition.

The metallic layer deposited on substrate 11 is masked by a known photoresist technique and then etched to produce a plurality of metallic electrodes 12—16 which are to serve as the under-electrodes of the capacitors C1 through C5, respectively. These electrodes may be formed by techniques other than the photoresist masking technique. For example, ion beam machining

may be employed. At the time these electrodes are formed, interconnecting strips 17 and a common metallic pad 18 are also formed, the pad 18 and the interconnecting strips 17 forming a common electrical connection for the electrodes during the subsequent anodizing process.

A layer of good dielectric material is then formed on the entire surface area of each electrode by anodizing the metallic electrodes in an appropriate electrolyte, such as about 0.01% solution of citric acid at about 200 volts for one hour, resulting in the formation of an oxide layer 19 on the upper surface of each electrode. In the case of a tantalum electrode, a layer of tantalum pentoxide (Ta_2O_5) is formed, and in the case of a hafnium electrode, a layer of hafnium oxide (HfO_2) is formed. This layer is of the order of several thousand Angstrom units thick. Once the anodizing has been completed, the pad 18 and the interconnecting strips 17 for the electrodes 12—16 may be eliminated from the structure by sawing the substrate 11 along the lines 21 shown in Figure 2. This sawing step may be postponed until after the structure has been completely fabricated, if desired.

An oxide layer 22 is then formed over the entire surface of the substrate 11 and the anodized electrodes 12—16. For example, silicon dioxide (SiO_2) may be sputtered onto the surface to a selected thickness (for example 2500 Å) to give the desired capacitance density. Silicon dioxide will give a capacitance density of .055 pf/mil². The thickness of the silicon dioxide layer may be accurately controlled within $\pm 2\%$, and, thus, the value of the capacitors formed may be very accurately controlled. Since, in this invention, it is not necessary to etch the oxide layer 22 during subsequent steps in the process, many oxides can be selected, for example, hafnium dioxide, aluminum oxide, yttrium oxide and tantalum pentoxide, to give different dielectric constants and different capacitance densities ranging from .05 to .55 pf/mil², silicon nitride is another example of a material suitable for providing the layer 22. The oxide layer 22 will generally have a thickness in the range of 2000 Å to 1000 Å. The oxide layer 22 is preferably formed by sputtering, but may be applied by other techniques, such as gaseous deposition and electron beam deposition.

A layer 23 of good resistive material is then applied over the oxide layer 22, for example, an 800 Å thick layer of tantalum nitride (Ta_2N) applied by reactive sputtering. Other resistive materials, such as Nichrome (Registered Trade Mark), hafnium nitride, and rhenium, may be selected for use, and may be applied by suitable techniques, including sputtering and evaporation. As is well known, the thickness of the resistive layer 23

will vary depending on the value of the ohms per square desired. Generally the thickness will range from 200 Å to several thousand Å. Typically, a 30 or 50 ohms/square resistive layer 23 is utilized. The sheet resistivity is established at a lower value than the desired ultimate value, the end value being produced by trimming the resistors as described below. The nominal resistivity range for a 30 ohm/square layer is, for example 24.0—26.5 ohms/square and that for the 50 ohms/square layer is 39.0—42.0 ohms/square.

An electrically conducting metal layer 24, preferably of chrome gold (CrAu) is then applied by any suitable technique, such as sputtering or evaporation. The metal layer 24 may also be formed of moly gold, nickel gold, or copper and may be formed to a suitable thickness (for example, several thousand Å) giving about .1 ohms/square.

At this stage in the fabrication, a foam of standard, general purpose predeposited substrate structure has been fabricated. In our example, only five capacitor under-electrodes have been provided, but a much larger number are fabricated on the general purpose substrate, the electrodes being of various area sizes and ranging around the periphery of the substrate. The large central portion of the substrate is available for creating the various resistors and the circuit interconnections, as well as providing room for bonding transistors to the structure. Any desired ones of the various capacitor under-electrodes may be used in the subsequent circuit fabrication.

These general purpose structures are given to circuit designers for their use in creating innumerable circuits. Since the process apparatus necessary to perform the remaining steps in the fabrication of such circuits is generally available to circuit designers, custom design is greatly facilitated.

The next operation in the fabrication of the illustrative structure of Figure 1 is to define the width of the resistor elements by a photoresist masking and an etch of both the CrAu layer 24 and the Ta_2N resistive layer 23 down to the surface of the SiO_2 layer 22 to form openings 25, 26, 27, and 28 (see Figures 4 and 5). Openings 25 and 26 define the width of resistor R1 therebetween; openings 27 and 28 define the width of resistor R3 therebetween; and openings 26 and 28 define the width of resistor R2 therebetween.

As is well known, the value of resistance R of the resistors, given a particular sheet resistivity, is determined by the length, L, and the width, W, thereof, where

$$R = \frac{L}{W}$$

For high resistance, the resistor is long and narrow, generally taking a sinuous shape. In our illustration, the resistors are of relatively small value and are therefore shorter in length than width.

As a next stage of fabrication, the upper-electrodes of the capacitors, the desired interconnections between the circuit and the external connection pads are then plated through a suitable mask onto the CrAu layer 24. A conductive material, such as gold or copper, is used and deposited to a desired thickness (for example, 1/4 mil). As seen in Figure 4, conductors 29, 30, 31, and 32 serve as external connectors for the capacitors C1, C3, C4, and C5, respectively; conductor 33 serves as the external connector for resistor R2; conductor 34 interconnects one side of capacitor C2 with capacitor C1 and resistor R1; conductor 35 interconnects the other side of capacitor C2 with capacitor C3 and resistor R3; conductor 36 interconnects capacitor C4 and resistor R1; conductor 37 interconnects capacitor C5 and resistor R3; and conductor 38 serves as the connector between resistor R2 and the transistor T1 to be thereafter bonded to the structure.

The value of each capacitor is established by the extent of the two regions sandwiched directly between the two upper-electrodes and the under-electrode, for example, in the case of capacitor C1, the region directly between the under-electrode 12 and the two upper-electrodes 29 and 34. The overlaid area of upper-electrode 13 of capacitor C2 is smaller than that for the other capacitors, and the capacitance of capacitor C2 is therefore substantially smaller than that of the other four capacitors. Each capacitor is formed, in effect by two capacitors connected in series. Such capacitors form the subject of our Copending Patent Application No. 48004/73 (Serial No. 1358388). For example, capacitor C1 is formed by the capacitance between upper-electrode 29 and under-electrode 12 plus the capacitance between upper-electrode 34 and under-electrode 12. The electrical connections of this capacitor are both made to the upper-electrodes 29 and 34, and no external connections are made with the under-electrode 12.

As mentioned above, the resistors of this circuit are low in value and, therefore, the length of the resistors is short. Resistor R2 is smaller in value than resistors R1 and R3 and is therefore wider.

As a next stage of fabrication the CrAu layer 24 and then the resistive Ta₂N layer 23 are removed from all areas 39 between and around the various circuit elements by employing photoresist and etching techniques. Thereafter, the layer 24 of CrAu is removed, by etching, from the areas 40, 41, and 42, leaving the layer of resistive material (Ta₂N) to form the resistors R1, R3, and

R2, respectively, in these areas (see Figure 6).

The resistors are now stabilized by placing the substrate in an oven at $425^{\circ} \pm 3^{\circ}\text{C}$ for a suitable period of time (for example, 10 min. ± 10 sec.).

As mentioned above, the sheet resistivity of the resistors was made lower than the desired ultimate value. The resistors are now brought up to final value by trimming. In one known method for raising the resistor value, an electrolyte is spread over the resistors, and they are then trim anodized to raise them to within the lower and upper permissible limits.

A resistor trimming technique, eliminating the need for anodizing, is utilized in this invention. The sheet resistivity may be raised by heat treating the resistors. For a given starting resistance, the resistors will increase in value proportionally to the length of time of the heat treatment. A typical curve illustrating the relationship between resistance R and heat treatment time T is shown in Figure 7. As shown by this curve, the resistance rises in a linear fashion during the earlier stage of the heat treatment and tends to level off later in the heat treatment. For any particular resistor, the starting resistance may be measured and, from the curve of Figure 7, the heating time necessary to raise the resistor value to within acceptable limits may be determined. The time range for each resistor on the substrate may be determined, and a common time length needed to bring all the resistors within range may be selected. For example, the length of the heat treatment time which will first bring one of the plurality of resistors to its maximum allowable resistance value is determined. This will be the maximum allowable time for trimming all the resistors. The length of heat treatment time needed to bring the last one of the resistors just over its minimum allowable resistance value is determined. This will be the minimum allowable time for the trimming. The proper heat treatment time will lie between these two limits. By using the formula of the trimming curve, and supplying the starting resistor values, all the computations necessary to determine a desired heat treatment time may be performed by a computer, significantly decreasing the fabrication time for these networks.

As an example, the oven is heated to $425^{\circ}\text{C} \pm 3^{\circ}\text{C}$ and the substrate, or substrates if more than one is being trimmed, is treated for from 10 minutes to 60 minutes, depending on the computed treatment time for the particular one or more substrates.

After final test of the circuit, the transistor T may be bonded to the interconnect 35 so that the collector electrode is coupled to the junction of C2, C3, and a R3. Electrical lead 43 is added to connect the base electrode to interconnect 34 between capacitors C1 and

C2 and resistor R1 while electrical lead 44 is added to connect the emitter electrode with interconnect 38 to the resistor R2.

WHAT WE CLAIM IS:—

1. A structure for use in forming thin film capacitors and resistors and interconnections thereto on a substrate, the structure comprising a substrate of insulating material; a plurality of metallic film elements provided on said substrate; a dielectric layer extending over the substrate and the oxidized upper surfaces of said plurality of metallic film elements; a layer of resistive material extending over said dielectric layer; and a layer of conductive material extending over said layer of resistive material.

2. A structure according to claim 1, wherein each of said metallic film elements is made of tantalum and has a tantalum pentoxide upper surface, and the resistive material is tantalum nitride.

3. A structure according to claim 1, wherein each of said metallic film elements is made of hafnium and has a hafnium oxide upper surface, and the resistive material is tantalum nitride.

4. A method of manufacturing a structure for use in forming thin film capacitors and resistors and interconnections thereto, the method comprising the steps of forming a plurality of metallic film elements on a surface of a substrate, forming an oxidized upper surface on each of the metallic film elements, forming a dielectric layer over the substrate surface and the oxidized upper surfaces of the metallic film elements, forming a layer of resistive material over the dielectric layer, and forming a layer of conductive material over the layer of resistive material.

5. A method according to claim 4, wherein each of the metallic film elements is made of tantalum and has a tantalum pentoxide upper surface, and the resistive material is tantalum nitride.

6. A method according to claim 4, wherein each of the metallic film elements is made of hafnium having a hafnium oxide upper surface and, the resistive material is tantalum nitride.

7. A method according to any of claims 4, 5 and 6, wherein the step of forming an oxidized upper surface on each of the metallic film elements comprises forming a common interconnecting circuit for electrically interconnecting the metallic film element so that the upper surfaces of the metallic film elements may be simultaneously electrochemically anodized, anodizing electrochemically the upper surfaces of the metallic film elements to form the oxidized upper surfaces, and thereafter disconnecting the interconnecting circuit from between the metallic film elements.

8. A method according to claim 7, wherein

the interconnecting circuit is formed between the metallic film elements and the edge of the substrate, and disconnection of the interconnecting circuit is accomplished by severing a peripheral portion of the substrate.

9. A method of manufacturing an integrated circuit structure including interconnected thin film capacitors and resistors, the method comprising the steps of forming a plurality of metallic film elements on a surface of a substrate, forming an oxidized upper surface on each of the metallic film elements, forming a dielectric layer over the substrate surface and the oxidized upper surfaces of the metallic film elements, forming a layer of resistive material over the dielectric layer, forming a first layer of conductive material over the layer of resistive material, forming connections of a second layer of conductive material on the first layer of conductive material to define desired electrical connections for the resistors and capacitors, removing areas of both the first conductive layer and the resistive layer to expose the surface of the dielectric layer to define the resistors and to form the capacitors and the electrical connections for the resistors and capacitors, and removing selected portions of the first conductive layer to expose the underlying layer of resistive material to thereby form the resistors.

10. A method according to claim 9, wherein the step of removing areas of both the first conductive layer and the resistive layer further comprises the step of removing portions of both the first conductive layer and the layer of resistive material to define a dimension of each resistor before forming connections of a second layer of conductive material.

11. A method according to either one of claims 9 and 10, wherein the step of forming the oxidized upper surfaces on the metallic film elements comprises anodizing the metallic film elements.

12. A method according to any one of claims 9, 10 and 11, wherein each of the metallic film elements is made of tantalum and has a tantalum pentoxide upper surface.

13. A method according to any one of claims 9 to 12, wherein the resistive material is made of tantalum nitride.

14. A method according to any one of claims 9 to 13, wherein the dielectric layer is made of a material comprising an oxide of silicon.

15. A method according to claim 14, wherein the oxide of silicon is silicon dioxide.

16. A method according to any of claims 9 to 15, wherein the step of forming an oxidized upper surface on each of the metallic film elements comprises forming a common interconnecting circuit for electrically interconnecting the metallic film elements so that the metallic film elements may be



C2 and resistor R1 while electrical lead 44 is added to connect the emitter electrode with interconnect 38 to the resistor R2.

WHAT WE CLAIM IS:—

1. A structure for use in forming thin film capacitors and resistors and interconnections thereto on a substrate, the structure comprising a substrate of insulating material; a plurality of metallic film elements provided on said substrate; a dielectric layer extending over the substrate and the oxidized upper surfaces of said plurality of metallic film elements; a layer of resistive material extending over said dielectric layer; and a layer of conductive material extending over said layer of resistive material.

2. A structure according to claim 1, wherein each of said metallic film elements is made of tantalum and has a tantalum pentoxide upper surface, and the resistive material is tantalum nitride.

3. A structure according to claim 1, wherein each of said metallic film elements is made of hafnium and has a hafnium oxide upper surface, and the resistive material is tantalum nitride.

4. A method of manufacturing a structure for use in forming thin film capacitors and resistors and interconnections thereto, the method comprising the steps of forming a plurality of metallic film elements on a surface of a substrate, forming an oxidized upper surface on each of the metallic film elements, forming a dielectric layer over the substrate surface and the oxidized upper surfaces of the metallic film elements, forming a layer of resistive material over the dielectric layer, and forming a layer of conductive material over the layer of resistive material.

5. A method according to claim 4, wherein each of the metallic film elements is made of tantalum and has a tantalum pentoxide upper surface, and the resistive material is tantalum nitride.

6. A method according to claim 4, wherein each of the metallic film elements is made of hafnium having a hafnium oxide upper surface and, the resistive material is tantalum nitride.

7. A method according to any of claims 4, 5 and 6, wherein the step of forming an oxidized upper surface on each of the metallic film elements comprises forming a common interconnecting circuit for electrically interconnecting the metallic film element so that the upper surfaces of the metallic film elements may be simultaneously electrochemically anodized, anodizing electrochemically the upper surfaces of the metallic film elements to form the oxidized upper surfaces, and thereafter disconnecting the interconnecting circuit from between the metallic film elements.

8. A method according to claim 7, wherein

the interconnecting circuit is formed between the metallic film elements and the edge of the substrate, and disconnection of the interconnecting circuit is accomplished by severing a peripheral portion of the substrate.

9. A method of manufacturing an integrated circuit structure including interconnected thin film capacitors and resistors, the method comprising the steps of forming a plurality of metallic film elements on a surface of a substrate, forming an oxidized upper surface on each of the metallic film elements, forming a dielectric layer over the substrate surface and the oxidized upper surfaces of the metallic film elements, forming a layer of resistive material over the dielectric layer, forming a first layer of conductive material over the layer of resistive material, forming connections of a second layer of conductive material on the first layer of conductive material to define desired electrical connections for the resistors and capacitors, removing areas of both the first conductive layer and the resistive layer to expose the surface of the dielectric layer to define the resistors and to form the capacitors and the electrical connections for the resistors and capacitors, and removing selected portions of the first conductive layer to expose the underlying layer of resistive material to thereby form the resistors.

10. A method according to claim 9, wherein the step of removing areas of both the first conductive layer and the resistive layer further comprises the step of removing portions of both the first conductive layer and the layer of resistive material to define a dimension of each resistor before forming connections of a second layer of conductive material.

11. A method according to either one of claims 9 and 10, wherein the step of forming the oxidized upper surfaces on the metallic film elements comprises anodizing the metallic film elements.

12. A method according to any one of claims 9, 10 and 11, wherein each of the metallic film elements is made of tantalum and has a tantalum pentoxide upper surface.

13. A method according to any one of claims 9 to 12, wherein the resistive material is made of tantalum nitride.

14. A method according to any one of claims 9 to 13, wherein the dielectric layer is made of a material comprising an oxide of silicon.

15. A method according to claim 14, wherein the oxide of silicon is silicon dioxide.

16. A method according to any of claims 9 to 15, wherein the step of forming an oxidized upper surface on each of the metallic film elements comprises forming a common interconnecting circuit for electrically interconnecting the metallic film elements so that the metallic film elements may be



electrochemically anodized simultaneously, electrochemically anodizing the upper surfaces of the metallic film elements to form the oxidized upper surfaces, and thereafter disconnecting the interconnecting circuit from between the metallic film elements.

17. A method according to claim 16, wherein the interconnecting circuit is formed between the metallic film elements and the edge of the substrate, and disconnection of the interconnecting circuit is accomplished by severing a peripheral portion of the substrate.

18. A method according to any one of claims 9 to 17 wherein the sheet resistivity of the layer of resistive material is lower than the ultimate resistivity desired and comprising the further step of heating the substrate for a first period of time to stabilize the layer of resistive material and heating the substrate for a second period of time to increase the resistivity of the layer of resistive material and trim the resistors to the desired ultimate value.

19. A method according to claim 18, wherein a plurality of resistors of different values is formed, the sheet resistivity of all of the resistors being lower than the ultimate resistivity desired, and the step of heating the substrate for the second period of time further comprises determining the length of time of heating needed to bring the first of the resistors up to its maximum permissible final value, determining the length of time of heating needed to bring the last of the resistors to its minimum permissible final value, and the heating of said substrate for a period of time falling between said two extremes to thereby trim all resistors to a value lying within their permissible limits.

20. An integrated circuit structure including at least one thin-film capacitor and resistor, the integrated circuit structure comprising:

- a substrate of insulating material;
- at least one metallic film element on a surface of the substrate, the metallic film element having an oxidized upper surface;
- a dielectric layer over the oxidized upper surface of the metallic film element and the surface of the substrate;
- a resistive layer over a portion of the dielectric layer;
- a pair of spaced apart capacitor plates,

each capacitor plate comprising a conductive layer on a portion of the dielectric layer, the pair of capacitor plates being situated above the metal film element and defining a capacitor therebetween; and

a pair of resistor terminals, each resistor terminal comprising a conductive layer on a portion of the dielectric layer, the pair of resistor terminals being in contact with and separated by a portion of the resistive layer and defining a resistor therebetween.

21. An integrated circuit structure according to claim 20 including:

a first conductive layer on a portion of the resistive layer; and

a second conductive layer on the first conductive layer, the capacitor plates and resistor terminals comprising a portion of the resistive layer, the first conductive layer and the second conductive layer.

22. An integrated circuit structure according to either one of claims 20 and 21 including interconnections between selected ones of the resistor terminals and capacitor plates, the interconnections comprising a portion of the resistive layer, the first conductive layer and the second conductive layer attached to the selected ones of the resistor terminals and capacitor plates.

23. An integrated circuit structure according to any one of claims 20 to 22 wherein the dielectric layer extends entirely over the surface of the substrate and the oxidized upper surface of the metallic film element and is made of silicon dioxide.

24. An integrated circuit structure according to any one of claims 20 to 23 wherein the metallic film element is a tantalum film element and the oxidized upper surface of the metallic film element is a layer of tantalum pentoxide.

25. A method of manufacturing a thin film structure substantially as hereinbefore described with reference to the accompanying drawings.

26. A thin film structure substantially as hereinbefore described with reference to the accompanying drawings.

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