PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : G06F 9/38	A1	(11) International Publication Number: WO 00/39670
		(43) International Publication Date: 6 July 2000 (06.07.00)

(21) International Application Number: PCT/US99/31321

(22) International Filing Date: 30 December 1999 (30.12.99)

(30) Priority Data:
09/224,621 31 December 1998 (31.12.98) US

(71) Applicant: INTEL CORPORATION [US/US]; 2625 Walsh Avenue, Santa Clara, CA 95051 (US).

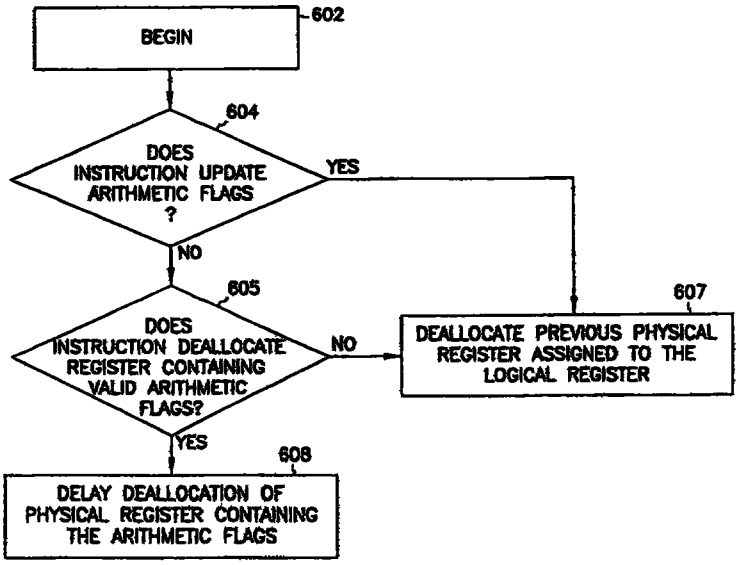
(72) Inventors: RAMIREZ, Ricardo; 20833 Elenda Drive, Cupertino, CA 95014 (US). MORRISON, Mike; 3131 Homestead Drive #10–J, Santa Clara, CA 95051 (US).

(74) Agent: VIKSNINS, Ann, S.; Schwegman, Lundberg, Woessner & Kluth, P.O. Box 2938, Minneapolis, MN 55402 (US).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: DELAYED DEALLOCATION OF AN ARITHMETIC FLAGS REGISTER



(57) Abstract

A microprocessor capable of delaying the deallocation of an arithmetic flags register is described. A system processes instructions of a first instruction set architecture which has an arithmetic flags register. The system also processes instructions of a second instruction set architecture which is not compatible with the first instruction set architecture. In order to process a first instruction of the first instruction set architecture that implicitly updates the arithmetic flags register, the arithmetic flags register shares a physical destination register with a general register containing a result for the first instruction. An instruction that does not update the arithmetic flags but would deallocate the register containing the arithmetic flags triggers the delayed deallocation mechanism of the present invention.