

Claims

What is claimed is:

1. An integration method for an electronic device comprising:
preparing a first electronic device having a first substrate, including:
 forming a first electrically conductive trace overlying at least a portion of the first substrate,
 forming a first barrier layer overlying at least a portion of the first electrically conductive trace,
 forming one or more first electrically conductive interconnects in contact with the first barrier layer, and
 forming a first bonding layer overlying at least a portion of the first electrically conductive trace and at least partially surrounding the one or more first interconnects;
preparing a second electronic device having a second substrate, one or more second electrically conductive interconnects, and a second bonding layer;
contacting the one or more first interconnects with the one or more second interconnects; and
contacting the first bonding layer with the second bonding layer.
2. The integration method according to claim 1, further comprising:
bonding the first bonding layer to the second bonding layer; and
bonding via temperature treatment the one or more first interconnects to the one or more second interconnects, whereby diffusion occurs between the one or more first interconnects and the one or more second interconnects.
3. The integration method according to claim 1 or claim 2, further comprising:
 forming a second electrically conductive trace on at least a portion of the second substrate;
 forming a second barrier layer on at least a portion of the second electrically conductive trace;
 forming the one or more second electrically conductive interconnects in contact with the second barrier layer; and

forming the second bonding layer on at least a portion of the second trace and at least partially surrounding the one or more second interconnects.

4. The integration method according to claim 3, or any other preceding claim, comprising:

preparing an opposite side of the second electronic device, including:

forming a third electrically conductive trace overlying at least a portion of the second substrate opposite the second electrically conductive trace;

forming a third barrier layer overlying at least a portion of the third electrically conductive trace;

forming one or more third electrically conductive interconnects in contact with the third barrier layer; and

forming a third bonding layer overlying at least a portion of the third electrically conductive trace and at least partially surrounding the one or more third interconnects; and

preparing a third electronic device having a third substrate, one or more fourth electrically conductive interconnects, and a fourth bonding layer;

bonding via direct contact the third bonding layer to the fourth bonding layer; and

bonding via temperature treatment the one or more third interconnects to the one or more fourth interconnects, whereby diffusion occurs between the one or more third interconnects and the one or more fourth interconnects.

5. The integration method according to claim 4, wherein the bonding via temperature treatment of the one or more first interconnects to the one or more second interconnects results in completion of a first integration stacking sequence;

wherein the bonding via temperature treatment of the one or more third interconnects to the one or more fourth interconnects results in completion of a second stacking sequence; and

wherein the method further comprises repeating **N** stacking sequences to define a vertically integrated stacked electronic device assembly.

6. The integration method according to claim 5, or any other preceding claim,
wherein the vertically integrated stacked electronic device assembly is tested after each bonding via temperature treatment.
7. The integration method according to claim 1, or any other preceding claim, further comprising:
removing a portion of the first and second bonding layers to expose respective outwardly addressable faces of the one or more first interconnects and the one or more second interconnects; and
contacting the faces of the one or more first interconnects with the respective faces of the one or more second interconnects.
8. The integration method according to claim 1, or any other preceding claim, further comprising:
forming a first photoresist layer overlying at least a portion of the first barrier layer; and
patterning the first photoresist layer to form one or more channels in the first photoresist layer;
wherein the one or more first interconnects are formed in the one or more channels in the first photoresist layer.
9. The integration method according to claim 8, further comprising:
after patterning the first photoresist layer, and after forming the one or more first interconnects, removing at least a portion of the first photoresist layer such that the one or more first interconnects remain.
10. The integration method according to claim 1, or any other preceding claim, further comprising:
forming a first seed layer overlying at least a portion of the first barrier layer, the first barrier layer being configured to accept formation of the first seed layer thereon;
wherein the first seed layer is configured to accept formation of the one or more first interconnects such that at least those portions of the first seed layer in contact

with the one or more first interconnects become an integral portion of the one or more first interconnects.

11. The integration method according to claim 1, or any other preceding claim, further comprising:

after forming the one or more first electrically conductive interconnects and before forming the first bonding layer, patterning the first electrically conductive trace; wherein the patterning removes at least a portion of the first electrically conductive trace and at least a portion of the first barrier layer.

12. The integration method according to claim 1, or any other preceding claim, further comprising:

forming a first adhesion layer overlying at least a portion of the first substrate; wherein the first adhesion layer is interposed between the first substrate and the first electrically conductive trace.

13. The integration method according to claim 4, comprising:

forming one or more electrically conductive vias through the second substrate to electrically connect the second electrically conductive trace with the third electrically conductive trace.

14. The integration method according to claim 1, or any other preceding claim,

wherein the first electrically conductive trace is made with a first metallic material;

wherein the one or more first electrically conductive interconnects are made with a second metallic material that is different from the first metallic material; and

wherein the first barrier layer is interposed between the first electrically conductive trace and the one or more first electrically conductive interconnects, the first barrier layer being configured to prevent interdiffusion of the one or more first interconnects with the first trace.

15. The integration method according to claim 14,
wherein the first electrically conductive interconnect is made from a transition metal; and

wherein the first bonding layer is made from a non-metallic oxide.

16. The integration method according to claim 1, or any other preceding claim,

wherein the first electrically conductive trace is formed by physical vapor deposition, chemical vapor deposition, vapor phase deposition, or sputtering;

wherein the barrier layer is formed by physical vapor deposition, chemical vapor deposition, vapor phase deposition, or sputtering;

wherein the one or more first interconnects are formed by physical vapor deposition, chemical vapor deposition, sputtering, or electroplating; and

wherein the first bonding layer is formed by chemical vapor deposition, sputtering, spin-on glass process, or plasma enhanced CVD.

17. An integrated 3D electronic device, comprising a first electronic device having:

a first substrate;

a first plurality of electrically conductive traces disposed on at least a portion of the first substrate;

a first plurality of electrically conductive interconnects disposed in contact with the first plurality of electrically conductive traces;

a first plurality of barrier layers interposed between the respective first plurality of electrically conductive traces and the first plurality of electrically conductive interconnects; and

a first bonding layer at least partially overlying the first substrate and at least partially surrounding the first plurality of interconnects,

wherein the first plurality of barrier layers are configured to prevent interdiffusion between the respective first plurality of electrically conductive traces and the first plurality of electrically conductive interconnects.

18. The integrated 3D electronic device according to claim 17, further comprising a second electronic device having:

- a second substrate;
- a second plurality of electrically conductive traces disposed on at least a portion of the second substrate;
- a second plurality of electrically conductive interconnects disposed in contact with the second plurality of electrically conductive traces;
- a second plurality of barrier layers interposed between the respective second plurality of electrically conductive traces and the second plurality of electrically conductive interconnects; and
- a second bonding layer at least partially overlying the second substrate, wherein the second plurality of barrier layers are configured to prevent interdiffusion between the respective second plurality of electrically conductive traces and the second plurality of electrically conductive interconnects, wherein the first bonding layer is bonded to the second bonding layer, and wherein at least one of the first plurality of interconnects is diffusion bonded to at least one of the second plurality of interconnects.

19. The integrated 3D electronic device according to claim 17 or claim 18, wherein the first plurality of barrier layers are configured to accept formation of respective first seed layers thereon, the first seed layers being compatible with the first plurality of electrically conductive interconnects such that the first seed layers form respective integral portions of the first plurality of electrically conductive interconnects..

20. The integrated 3D electronic device according to claim 18 or claim 19, wherein at least one of the first plurality of electrically conductive traces and the second plurality of electrically conductive traces are made from aluminum or aluminum alloy;

- wherein at least one of the first plurality of electrically conductive interconnects and the second plurality of electrically conductive interconnects are made from nickel or nickel alloy;

- wherein at least one of the first plurality of barrier layers and the second plurality of barrier layers are selected from the group consisting of: titanium nitride, titanium tungsten, tantalum, and tantalum nitride; and

wherein at least one of the first bonding layer and the second bonding layer are made from an oxide.