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Picture signal decoder and converter

The invention relates to a circuit arrangement comprising a digital color decoder for decoding a digital chrominance signal of a picture signal, the chrominance signal having a first sampling frequency which is optimized for the properties of the chrominance signal and/or the picture signal.

Known digital color decoders for decoding a chrominance signal of a digital picture signal applied thereto and for generating component signals from the chrominance signal and the picture signal operate at a digital picture signal sampling frequency which is specially adapted to the properties of this picture signal and/or its chrominance signal. For example, the sampling frequency may be coupled to the horizontal frequency of the picture signal or to the chrominance subcarrier frequency of the chrominance signal. The chrominance signal is thus decoded at a minimal level of interference, while the coupling to the horizontal frequency of the picture signal results in the overall picture signal being processed with minimal interference.

It is an object of the invention to improve a circuit arrangement of this type in such a way that the component signals generated by this arrangement can be processed optimally for subsequent circuit arrangements.

According to the invention, this object is achieved by a sampling frequency converter coupled to the color decoder for converting the digital chrominance component signals determined by the decoder into a second sampling frequency which is adaptable to the requirements of subsequent circuit elements for signal processing and/or picture display.

Digital picture signals are increasingly being processed, not only in digitally operating television receivers but also in other apparatuses for processing such picture signals. Such apparatuses may be, for example, digital video recorders or personal computers. They generally operate at predetermined sampling frequencies adapted to the signal processing operations in these apparatuses. For example, in computers, these frequencies are more or less predetermined for picture processing. By means of the circuit arrangement according to the invention, in which a sampling frequency converter is coupled to the color decoder, it is possible to process the component signals supplied by the color

This Sheet Has Been Replaced

decoder at the first sampling frequency in such a way that it can be optimally further processed in subsequent circuit elements, for example, in apparatuses of the type mentioned above. If these second apparatuses operate at a second sampling frequency, it is possible to convert the component signals from the first into the second sampling frequency by means of the sampling frequency converter in such a way that the second sampling frequency is adaptable to the requirements of the circuit arrangements in the subsequent apparatus. If necessary, this adaptation may be flexible, for example, when different sampling frequencies are chosen in a computer for different display formats.

Moreover, if desired, it is possible to change the aspect ratio of the picture signal by means of this circuit arrangement. Picture signals having different aspect ratios can also be adapted to the required data current or to the required sampling frequency of subsequent circuit elements in such a way that it is adaptable to a picture display by these subsequent circuit elements. For example, a picture signal having a 16:9 aspect ratio but being transmitted at the first sampling frequency in a horizontal sync signal frame having an aspect ratio of 4:3 can thus be adapted to a 16:9 aspect ratio picture display for the purpose of further processing.

Because of its flexible adaptation to various conditions, the circuit arrangement according to the invention is adaptable to different apparatus designs. The circuit arrangement thus provides the possibility of one construction with a simple adaptation to different apparatus designs.

The circuit arrangement according to the invention is also suitable for analog picture signals. As characterized by an embodiment of the invention, the digital color decoder is then preceded by an A/D converter for converting an analog chrominance signal applied thereto and an analog picture signal, which may comprise the chrominance signal, into digital signals having the first sampling frequency.

Another embodiment of the invention is characterized in that the sampling frequency converter is provided with a buffer memory for ensuring that the output of the color decoder supplies a continuous data current of chrominance component signals at the second sampling frequency, and in that the buffer memory is preferably also used for correcting possible timebase fluctuations in the chrominance signal.

In this way, it is ensured in every case that the data current supplied from the output of the circuit arrangement at the second sampling frequency appears without gaps, i.e. without interferences, and that there is no overflow of data in the circuit arrangement according to the invention.

This Sheet Has Been Replaced

In a further embodiment of the invention, the second sampling frequency is advantageously derived from the first sampling frequency. This ensures that there is no drift between these two sampling frequencies.

Further advantageous embodiments of the invention are described in the dependent Claims.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawing,

the sole Figure shows a block diagram of a circuit arrangement according to the invention, having an input which receives a picture signal VBS. A chrominance signal C is associated with this picture signal. An increasingly common aspect of practice in picture signal processing operations, also for a transmission standard such as PAL or NTSC, is to apply the chrominance signal as separately as possible from the rest of the picture signal to the decoder.

The picture signal VBS is applied to a first A/D converter 1; the chrominance signal C is applied to a second A/D converter 2.

A color decoder 3, for example, suitable for multistandard use, i.e. a decoder capable of decoding chrominance signals of different transmission standards, such as, for example, PAL, SECAM or NTSC, is coupled to the two A/D converters 1 and 2.

The output of the color decoder 3 supplies digital component signals, denoted by Y, U and V in the Figure.

In this embodiment, the picture signal VBS and the associated chrominance signal C is assumed to be a PAL signal. The component signal Y supplied from the output of the color decoder 3 then indicates the luminance component, and the signals U and V indicate the chrominance components.

The signals are subsequently received by a sampling frequency converter 4 which supplies corresponding signals from its output, but are clocked at a different sampling frequency. These signals are denoted by Y', U' and V' in the Figure.

These signals are subsequently further processed in an arrangement 5 which is shown only diagrammatically in the Figure and comprises circuit elements optimized for, or operating at, the sampling frequency at which the signals Y', U' and V' are present.

The circuit arrangement shown in the Figure also comprises a first clock-

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generating circuit 6. This circuit may generate, for example, a first sampling frequency derived from the picture signal VBS. The first and the second A/D converter 1, 2, the color decoder 3 and the sampling frequency converter 4 are controlled by this sampling frequency.

The analog picture signal VBS and the associated chrominance signal C are converted into digital signals in the converters 1 and 2 at this sampling frequency, and these digital signals are applied to the color decoder 3. The signals are processed in the color decoder 3 at this first sampling frequency. Also the component signals Y, U and V supplied from the output of the decoder 3 convey this first sampling frequency.

The sampling frequency converter converts these signals Y, U and V at the first sampling frequency into the signals Y', U' and V' which convey a second sampling frequency. This second sampling frequency is generated by a second clock-generating circuit 7. The second sampling frequency is optimized for the subsequent circuit elements symbolized by means of the circuit block 5.

The second clock-generating circuit 7 supplies the second sampling frequency generated by this circuit to the sampling frequency converter 4 and to the subsequent circuit elements 5.

The second sampling frequency may advantageously be derived from the first sampling frequency generated by the first clock-generating circuit 6.

The subsequent circuit elements symbolized by means of the circuit block 5 may be, for example, elements of a personal computer or of a digital video recorder. Such apparatuses generally operate at predetermined sampling frequencies which, in the embodiment shown in the Figure, correspond to the second sampling frequency generated by the second clock-generating circuit 7.

The first sampling frequency generated by the first clock-generating circuit 6 is adapted to the properties of the chrominance signal C and the picture signal VBS. For example, the advantage of deriving this first sampling frequency from the sync signal frame of the picture signal VBS is that the color decoder can better react to timebase fluctuations of the picture signal or its sync signal frame, or that these timebase fluctuations disturb the color decoding operation to a minimal extent.

Overall, it is achieved by means of this circuit arrangement that, on the one hand, an optimum color decoding operation can be performed and, on the other hand, this decoded digital picture signal is optimally adaptable to subsequent circuit arrangements. There may also be a continuous adaptation to the different sampling frequencies, as is advantageous in, for example, a personal computer for different format or pixel rate

This Sheet Has Been Replaced

displays. Moreover, it is possible to convert the aspect ratio of the picture signal.

The sampling frequency converter shown diagrammatically in the Figure may be provided with a buffer memory. This buffer memory can ensure that the data current of chrominance component signals supplied from the output of the color decoder 3 at the second sampling frequency is continuous, i.e. there are no gaps in this data current. On the other hand, such a buffer memory may prevent overflow of data within the color decoder. The buffer memory may further be used for correcting timebase fluctuations of the picture signal, hence also of the chrominance signals.

CLAIMS

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1. A circuit arrangement comprising a digital color decoder (3) for decoding a digital chrominance signal of a picture signal, the chrominance signal having a first sampling frequency which is optimized for the properties of the chrominance signal and/or the picture signal, characterized by a sampling frequency converter (4) coupled to the color decoder for converting the digital chrominance component signals determined by the decoder into a second sampling frequency which is adaptable to the requirements of subsequent circuit elements (5) for signal processing and/or picture display.

2. A circuit arrangement as claimed in Claim 1, characterized in that the digital color decoder is preceded by an A/D converter (1;2) for converting a chrominance signal applied thereto, or a picture signal into a digital signal having the first sampling frequency.

3. A circuit arrangement as claimed in Claim 1 or 2, characterized in that the sampling frequency converter (4) is provided with a buffer memory for ensuring that the output of the color decoder (3) supplies a continuous data current of chrominance component signals at the second sampling frequency, and in that the buffer memory is preferably also used for correcting possible timebase fluctuations in the chrominance signal.

4. A circuit arrangement as claimed in any one of Claims 1 to 3, characterized in that the second sampling frequency is derived from the first sampling frequency.

5. A circuit arrangement as claimed in any one of Claims 1 to 4, characterized in that the first sampling frequency is derived from the line frequency of the picture signal.

6. A circuit arrangement as claimed in any one of Claims 1 to 5, characterized in that the first sampling frequency is derived from the chrominance subcarrier frequency of the chrominance signal.

7. A circuit arrangement as claimed in any one of Claims 1 to 6, characterized in that the second sampling frequency is chosen in such a way that a conversion of the aspect ratio of the chrominance signal or the picture signal is achieved.

8. A circuit arrangement as claimed in any one of Claims 1 to 7,

This Sheet Has Been Replaced

characterized in that the second sampling frequency depends on a sampling frequency in a subsequent picture display/signal processing unit of a personal computer.

9. A circuit arrangement as claimed in any one of Claims 1 to 7, characterized in that the second sampling frequency depends on a sampling frequency in a subsequent signal processing unit of a video recorder.

10. A picture display device including a circuit arrangement as claimed in any one of Claims 1 to 8.

11. A video recorder including a circuit arrangement as claimed in Claim 9.