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PROVISIONAL PATENT
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**SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE
HAVING A LEAKAGE CURRENT REDUCTION MEANS**

Background of the Invention

5 The present invention relates generally to semiconductor design technology, and more particularly, to a system and method for reducing leakage current in a semiconductor circuit.

Due to many technological advances, integrated circuits, or "chips," incorporate many millions of transistors on a single monolithic device. This provides many advantages, including increased speed and reduced size, but
10 the current drawn by each transistor becomes more of a problem as the number of transistors on a single chip increases. The problem is somewhat alleviated by the fact that all of the transistors on a single chip are never simultaneously active, and theoretically, a transistor only draws current while it is active. However, a transistor does draw a small leakage current
15 while it is inactive. Although the magnitude of the leakage current for a single transistor is typically on the order of a few pico-amperes, due to the large number of transistors on a single chip, the few pico-amperes per inactive transistor becomes a significant amount.

For example, Figs. 1a and 1b illustrate a conventional p-channel
20 metal oxide semiconductor ("PMOS") transistor 10a and a corresponding voltage-current graph 10b. The transistor 10a has a gate G, a source S, a drain D, and a well W. The well W is typically biased to the same voltage applied to the source S. The transistor 10a is activated by forming a p-channel (not shown) of minority carriers in the well W between a source-
25 drain junction (not shown) when a voltage V_{GS} is applied to the transistor.

In operation, if the voltage V_{GS} is negative, the transistor 10a is active and draws a drain current I_D as shown in the graph 10b. If the voltage V_{GS} is equal to 0V, the transistor 10a is inactive and the drain



current I_D approaches 0 amps. However, the drain current I_D does not quite reach 0amps because the transistor 10a still draws a very small leakage current I_{LK} , which flows across the drain-source junction due to the minority carriers still located in the p-channel.

5 Therefore, what is needed is a circuit and method for enabling a transistor to operate in a mode in which the leakage current drawn by the transistor is significantly reduced. *A technology for reducing leakage current is described in U.S. patent NOS. 5,274,601 (1993/12/28), 5,408,144 (1995/4/18), and 5,521,529 (1996/5/28).*

Summary of the Invention

10 The present invention, accordingly, provides a circuit and method for reducing the leakage current drawn by a transistor while it is inactive. In a first implementation, a circuit selectively drives the gate of the transistor to a voltage level above a source voltage. As a result, the gate-source voltage is reversed and leakage current flowing through the transistor is substantially reduced. In a second implementation, a circuit selectively
15 biases the well of the transistor to a voltage level above a normal bias voltage. As a result, the voltage-current characteristics of the transistor are modified so that leakage current is substantially eliminated.

20 A technical advantage achieved with the present invention is that it enables a transistor to operate in a normal mode, with typical voltage-current characteristics, or in a standby mode, with a significantly reduced leakage current.

Brief Description of the Drawings

Fig. 1a is a schematic diagram of a conventional transistor.

Fig. 1b is a voltage-current graph of the transistor of Fig. 1a.

25 Fig. 2 is a schematic diagram of a circuit embodying a first implementation of the present invention.



Fig. 3 is a schematic diagram of a circuit embodying a second implementation of the present invention.

Fig. 4 is a graph of a voltage-current characteristic of a transistor of the circuit of Fig. 3.

Fig. 5 is a DRAM block diagram to which this invention is applied.

Fig. 6 is another embodiment of this invention.

5 **Detailed Description of the Preferred Embodiment**

As described above, Figs. 1a and 1b respectively illustrate a conventional transistor and its voltage and current characteristics. The description below utilizes conventional transistors, such as the transistor 10a, and therefore the individual components and characteristics of the transistor 10a are used and referenced by the description of the preferred embodiment.

Referring to Fig. 2, the reference numeral 12 designates, in general, to a first implementation of an integrated circuit embodying features of the present invention. The circuit 12 utilizes a first positive power supply (VPERI), a second positive power supply (VPP) and a ^{ground-level} negative power supply (VSS) such that $VSS < VPERI < VPP$. For the sake of example, VSS, VPERI, and VPP will be deemed to be 0V, 2.5V and 3.6V, respectively. The circuit 12 comprises an input signal IN, a standby signal STB, an output signal OUT, two inverters 14, 16, one pass transistor 18, and one standby transistor 20. The inverter 14 comprises a p-channel metal oxide semiconductor ("PMOS") transistor 22 and an n-channel metal oxide semiconductor ("NMOS") transistor 24 and the inverter 16 comprises a PMOS transistor 26 and an NMOS transistor 28. Furthermore, all of the NMOS transistors 18, 24, 28 have a VSS-biased well, one PMOS transistor 20 has a VPP-biased well, and two PMOS transistors 22, 26 have a VPERI-biased well.

In operation, when the standby signal STB is "high," ^(VPP) the circuit 12 is in a normal mode and operates as a conventional driver. The signal



received at the input signal IN is inverted by the inverter 14, passed through the pass transistor 18, inverted again by the inverter 16, and driven at the output signal OUT. However, when the standby signal STB is "low", ^(VSS) the circuit 12 enters a standby mode. Because the standby signal STB is low, the ^(first switch transistor) pass transistor 18 ^(second switch transistor) becomes inactive and the standby transistor 20 becomes active. When this happens, an input N1 of the inverter 16 is pulled high to the VPP voltage level (3.6V). As a result, the voltage VGS of the transistor 26 becomes positive, due to the voltage at the gate of the transistor 26 being greater than the voltage at the source, reducing the number of minority carriers in the channel in the source-drain junction of the transistor and thereby reducing the leakage current ("ILK") through the transistor as shown in Fig. 1b.

Referring to Fig. 3, the reference numeral 30 designates, in general, to a second implementation of an integrated circuit embodying features of the present invention. The circuit 30 utilizes the same three power supplies VSS, VPERI, VPP of the circuit 12 (Fig. 2) and comprises the same signals IN, OUT and STB. The circuit 30 further comprises two inverters 32, 34, and two well-biased transistors 36, 38. The inverter 32 comprises a PMOS transistor 40 and an NMOS transistor 42 and the inverter 34 comprises a PMOS transistor 44 and an NMOS transistor 46. Furthermore, all of the NMOS transistors 38, 42, 46 have a VSS-biased well, the PMOS transistors 36 has a VPP-biased well, and the PMOS transistors 40 has a VPERI-biased well. The well of the PMOS transistor 44 is connected to the drains of the two well-biased transistors 36, 38, which have their sources connected to VPERI and VPP, respectively.

In operation, when the standby signal STB is ^(VPP) high, the circuit 30 is in a normal mode and operates as a conventional driver. The signal received at the input signal IN is inverted by the inverter 32, is inverted again by the inverter 34, and is driven at the output signal OUT. Because the



standby signal STB is high, the well-biased transistor 36 is inactive and the well-biased transistor 38 is active. As a result, the well of the PMOS transistor 44 is biased to VPERI (2.5V) and performs in a normal, conventional manner. However, when the standby signal STB is low, ^(V_{SS}) the circuit 30 enters a standby mode. In the standby mode, the well-biased transistor 38 is inactive and the well-biased transistor 36 is active. As a result, the well of the PMOS transistor 44 is biased to VPP (3.6V) and performs in a different manner, as described below.

Referring to Fig. 4, the graph 50 includes a dotted line 52, which represents the voltage-current characteristics of the VPERI-well-biased transistor 44, just like the conventional transistor 10a of Fig. 1, and a solid line 54, which represents the voltage-current characteristics of the VPP-well-biased transistor 44 of Fig. 3. By applying the bias voltage VPP (3.6V) to the well of the transistor 44, the well is biased above the source voltage of the transistor, which is at the VPERI voltage level. As a result, the voltage-current characteristics of the transistor 44 are offset from the conventional characteristics shown by the dotted line 52. Due to this offset, when the voltage VGS equals 0V, the corresponding leakage current ILK is significantly reduced.

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Figure 5 shows a DRAM block diagram to which this invention is applied. The DRAM shown in this figure is configured on a single semiconductor substrate made of monolithic silicon using a fabrication technique for semiconductor circuits.

This DRAM receives external power-supply voltage VDD such as 3.3 V and ground voltage Vss, such as 0 V, from the external power-supply terminal. Memory array (MARY) 1 comprises word lines, data-line pairs, and dynamic memory cells. In the DRAM of this embodiment, the MOS transistors of memory array 1 are made compact to increase the storage capacity. Accompanied by the reduction in the gate length of the MOS transistor, the gate oxidized film is made thin. Due to this, the operation voltage of memory array 1 is reduced; step-down voltage VARY, e.g., 2.0 V, is used. Substrate bias voltage VBB (-1 V) is applied to the substrate (well area) on which MOS transistors are formed.

Decoder and word driver (DEC/WDRIV) 2 selects a predetermined word line by receiving external address signal A0 to Ai. Using step-down voltage VPERI, such as 2.5 V, for the peripheral circuit, low power consumption is achieved. A boost voltage, such as 3.6 V, is used for the word-line drive. The circuit of this invention shown in Figs. 2 and 3 can be used for the decoder section in the above decoder and word driver 2.

Step-down circuits 4, 6, and 7 generate the above step-down voltages VPERI, VBB, and VARY. Step-down circuit 4 can be omitted. In such a case, external power-supply voltage VDD is used instead of step-down voltage VPERI. Step-up circuit 5 generates the above step-up voltage VPP. Timing generator (TG) 8 generates an internal control signal by receiving external control signals CONT1-CONTn. The above standby signal STB is output from the above timing generator (TG) 8, and is supplied to the above peripheral circuit. I/O circuit (DIO) 3, which includes a main amplifier, a write amplifier, and a data I/O buffer, is connected to external I/O terminals DQ0 - DQi.

The circuit shown in Fig. 6 shows another embodiment of this invention. Transistors 61, 62, 65, and 66 correspond to transistors 26, 28, 22, and 24 shown in Fig. 2. In the embodiment of Fig. 6, first and second switch transistors 64 and 63 are

provided to reduce the leak current which flows in the NMOS transistor 62 when the NMOS transistor 62 is off.

In the circuit shown in Fig. 2, the output signal is fixed to low (VSS). By contrast, the output signal is fixed to the high level (VPERI) during a standby state. In Fig. 6, when the standby signal STB' is low (VBB), the PMOS transistor 64 is on, the NMOS transistor 63 is off, and an output signal OUT corresponding to an input signal IN can be obtained. In addition, while the standby signal STB' is high (VPERI), the circuit is in the standby state. In this case, the PMOS transistor 64 is off and the NMOS transistor 63 is on. During the standby state, the gate voltage (VBB) of the NMOS transistor 62 becomes lower than the source voltage (VSS). As a result, the NMOS transistor 62 is turned off sufficiently, and a leak current is reduced.

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Although illustrative embodiments of the present invention have been shown and described, a latitude of modification, change and substitution is intended in the foregoing disclosure, and in certain instances, some features of the invention will be employed without a corresponding use of other features. For example, the leakage current reduction scheme can be implemented in a register or a buffer, and is described with a driver only for ease of description. Furthermore, NMOS transistors also draw a leakage current and would benefit from application of the present invention. Finally, additional or alternative components and other circuits may be added without altering the scope of the invention. Accordingly, it is

appropriate that the appended claims be construed broadly and in a manner consistent with the scope of the invention.

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Claims

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What is claimed is:

- 1 1. An output circuit comprising:
2 a first terminal for receiving a positive power supply voltage;
3 a second terminal for receiving a ^(ground-level) ~~negative~~ power supply
4 voltage; and
5 a first inverter comprising a PMOS transistor and an NMOS
6 transistor connected in series between said first and second terminals;
7 wherein, in a normal mode, an input signal to said first
8 inverter, supplied to gates of said PMOS and NMOS transistors, has a first
9 voltage level corresponding to said ^(ground-level) ~~negative~~ power supply voltage and a
10 second voltage level corresponding to said positive power supply voltage,
11 and
12 wherein, in a standby mode, said input signal to said first
13 inverter has a third voltage level being higher than the level of said positive
14 power supply voltage.

- 1 2. An output circuit according to claim 1, further comprising:
2 a second inverter;
3 a third terminal for receiving a voltage having said third
4 voltage level;
5 a ^{first} ~~pass~~ transistor having a source-drain path provided between
6 an output terminal of said second inverter and an input terminal of said
7 first inverter; and
8 a ^{second} ~~standby~~ transistor having a source-drain path provided
9 between an input terminal of said first inverter and said third terminal;





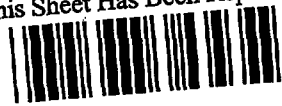
10 wherein, in said normal mode, said ~~pass~~^{first} transistor is active
11 and said ~~standby~~^{second} transistor is inactive, and
12 wherein, in said standby mode, said ~~pass~~^{first} transistor is inactive
13 and said ~~standby~~^{second} transistor is active.

1 3. An output circuit comprising:
2 a first terminal for receiving a positive power supply voltage;
3 a second terminal for receiving a ~~negative~~^{ground-level} power supply
4 voltage; and
5 an inverter comprising a PMOS transistor and an NMOS
6 transistor connected in series between said first and second terminals,
7 wherein, in a normal mode, a first voltage level corresponding
8 to said power supply voltage is applied to a well of said PMOS transistor,
9 and
10 wherein, in a stand-by mode, a second voltage level is applied
11 to said well of said PMOS transistor, said second voltage level being higher
12 than a level of said positive power supply voltage.

1 4. A circuit for reducing leakage current in a transistor, the
2 circuit comprising an output transistor having a gate connected to an input
3 of the circuit, a drain connected to an output of the circuit and a source
4 connected to a first power supply, and means for selectively disconnecting
5 the gate from the input and connecting the gate to a second power supply,
6 wherein a voltage level of the second power supply is greater than a voltage
7 level of the first power supply.

1 5. The circuit of claim 4 wherein the means for selectively
2 connecting and disconnecting comprises a PMOS transistor connected





3 between the gate and the second power supply and an NMOS transistor
4 connected between the gate and the input.

1 6. A method for selectively switching a PMOS transistor between
2 a normal mode in which the PMOS transistor operates in a conventional
3 manner and a standby mode in which a leakage current of the PMOS
4 transistor is significantly reduced, the method comprising selectively
5 connecting a gate of the PMOS transistor to a power supply having a
6 voltage level that is greater than a source voltage of the PMOS transistor.

1 7. The method of claim 6 wherein in the normal mode, the gate of
2 the PMOS transistor is connected to an input signal operating at a voltage
3 level less than or equal to the source voltage of the PMOS transistor.

1 8. A method for selectively switching an NMOS transistor
2 between a normal mode wherein the NMOS transistor operates in a
3 conventional manner and a standby mode wherein a leakage current of the
4 NMOS transistor is significantly reduced, the method comprising
5 selectively connecting a gate of the transistor to a power supply having a
6 voltage level that is less than a source voltage of the NMOS transistor.

1 9. The method of claim 8 wherein in the normal mode, the gate of
2 the NMOS transistor is connected to an input signal operating at a voltage
3 level greater than or equal to the source voltage of the NMOS transistor.

1 10. A circuit for reducing leakage current in a transistor, the
2 circuit comprising an output transistor having a gate connected to an input
3 of the circuit, a drain connected to an output and a source connected to a
4 first power supply, and means for selectively connecting a well of the output



5 transistor to either the first power supply or a second power supply,
6 wherein a voltage level of the second power supply is greater than a voltage
7 level of the first power supply.

1 11. The circuit of claim 10 wherein the means for selectively
2 connecting comprises a first well-biased transistor and a second well-biased
3 transistor wherein the first well-biased transistor connects the well of the
4 output transistor to the first power supply and the second well-biased
5 transistor connects the well of the output transistor to the second power
6 supply.

1 12. A method for selectively switching an output transistor
2 between a normal mode wherein the output transistor operates in a
3 conventional manner and a standby mode wherein a leakage current
4 through the output transistor is reduced comprising selectively connecting a
5 well of the output transistor between two separate power supplies.

1 13. The method of claim 12 wherein the step for selectively
2 connecting comprises activating either a first well-biased transistor
3 connected in series between the well of the output transistor and the first
4 power supply or activating a second well-biased transistor connected in
5 series between the well of the output transistor and the second power
6 supply.

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14. A semiconductor memory comprising:
a memory array;
a peripheral circuit coupled to said memory array; and
a step-up circuit generating a second power-supply voltage
higher than a first power-supply voltage,

wherein said peripheral circuit includes (a) an output transistor having a gate coupled to an input terminal, a drain coupled to an output terminal and a source receiving said first power-supply voltage and (b) a switch circuit which supplies said second power-supply voltage to said gate with said gate disconnected from said input terminal.

15. A semiconductor memory according to claim 14, wherein a high level of an input signal supplied to said input terminal corresponds to a level of said first power-supply voltage.

16. A semiconductor memory according to claim 15, wherein said peripheral circuit is a decoder which generates a select signal for the above memory array by receiving address signals.

17. A semiconductor memory comprising:
a memory array;
a decoder coupled to said memory array;
a control circuit which outputs a control signal to indicate whether said decoder is in either normal operation state or stand-by state; and

a step-up circuit which generates a second power-supply voltage higher than a first power-supply voltage,

wherein said decoder comprises (a) an output circuit having a PMOS transistor with a gate coupled to an input terminal, a drain coupled to an output terminal and a source receiving said first power-supply voltage and (b) a switch circuit which supplies said second power-supply voltage to said gate with said gate disconnected from said input terminal.

18. A semiconductor memory according to claim 17, further comprising a NMOS transistor having a gate coupled to said input



terminal, a drain coupled to said output terminal and a source receiving a ground-level voltage.

19. A semiconductor memory according to claim 18, wherein said switch circuit comprises (a) a first switch MOS transistor having a source-drain path provided between the common gate of said NMOS transistor and PMOS transistor and said input terminal and (b) a second switch MOS transistor having a source-drain path provided between said common gate and a terminal receiving said second power-supply terminal.

20. A semiconductor memory according to claim 19, wherein said first switch MOS transistor is an NMOS transistor, said second switch MOS transistor is a PMOS transistor, and said control signal is applied to the common gate of said first and second switch MOS transistors.

21. A semiconductor memory according to claim 19, wherein a high level of an input signal applied to said input terminal corresponds to a level of said first power-supply voltage, and a low level of an input signal corresponds to said ground-level voltage.

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