

The invention relates to an asynchronous digital correlator and to demodulators including such a correlator.

This correlator makes it possible to process a
5 complex signal consisting of a first and a second
carrier, I and Q, which are modulated by a pseudo-random
function in order to spread the spectrum, and are modu-
lated by an orthogonal M-ary code. Such a complex signal
results, for example, from a modulation of PSK or MSK or
10 QPSK type, with spread spectrum and modulation by Walsh
codes. Demodulation of such a signal requires its
spectrum to be compressed by means of a pseudo-random
function identical to that which was used to spread this
spectrum, and then consists in recognising a transmitted
15 datum, by identifying the modulating code from among the
M possible codes. These two operators can be produced by
means of a correlator. A correlator for BPSK signals is
known from the document Proceedings of Melecon '87
Mediterranean Electrotechnical Conference, 34th Congress
20 on Electronics, Joint Conference, 1987 pages 157-161 -
IEEE New York, US, M.K. Sust et al entitled : "All
digital signal processing in a spread spectrum communica-
tion system".

However, to correlate more complex modulations,
25 there is currently no correlator enabling a complex
signal to be correlated with a reference signal, over a
great length, such as 256 moments, whilst having a
sufficiently simple structure to make it possible to
produce a demodulator which can be integrated into a
30 single integrated circuit. The correlators of known types
are designed for the recognition of frames rather than
for demodulation. A first type of known correlator
device, which is available commercially in the form of an
integrated circuit, functions over 64 moments only. A
35 second known type of correlator, available commercially
in integrated-circuit form, functions over 256 moments
and includes no intermediate outputs providing partial
correlation values relating to a smaller number of
moments.

The known demodulators include a large number of 64-moment or 256-moment correlators. Indeed, they include an array of four 64-moment correlators, or one 256-moment correlator, for the carrier I; and an array of four 64-moment correlators, or one 256-moment correlator, for the carrier Q, for each of the M-ary codes. The number M possibly being equal to 16, the number of correlator integrated circuits can thus reach 128.

The aim of the claimed invention is therefore to propose an asynchronous digital correlator making it possible to produce in particular simpler demodulators which might possibly be integrated into a small number of integrated circuits, or even into a single integrated circuit. The subject of the invention is a correlator having a systolic structure in which the calculations for the carrier I and for the carrier Q are time-division multiplexed, and which is divided in such a way that it provides values of the modulus of a partial correlation function calculated over much smaller lengths than the total correlation length, so as to allow code recognition by means of a relatively simple arithmetic circuit which calculates linear combinations of these moduli.

According to the invention, an asynchronous digital correlator for correlating a binary reference signal, with a complex signal consisting of a first and a second carrier which are modulated by a pseudo-random function and by an M-ary orthogonal Walsh coding, these two carriers being sampled and digitized, characterized in that it includes:

- a multiplexer for transmitting alternately a value of the first carrier and a value of the second carrier, with a period equal to half their sampling period;

- a first digital filter matched to the pseudo-random function, including an array of registers for storing L consecutive bits of the reference signal and an array of M correlation macro-cells receiving the sequence of the multiplexed values of the first and of the second carrier (I, Q), each macro-cell calculating the value of

a first function, termed partial correlation, between N bits of the reference signal and N values of the first carrier, then calculating the value of a second function, termed partial correlation, between N bits of the reference signal and N values of the second carrier, N being equal to L/M ;

- a second digital filter including calculating means for determining the value of linear combinations of the values of the first partial correlation functions, then of linear combinations of the values of the second partial correlation functions, which means are matched to the Walsh codes, the coefficients of the linear combinations being unchanged and being equal to ± 1 ; and including means for demultiplexing the values of the linear combinations, and determining the modulus of a vector having the values of these two linear combinations as components.

The invention will be better understood and other details will emerge with the aid of the description below and the accompanying figures:

- Figure 1 represents the schematic diagram of an illustrative embodiment of a demodulator according to the prior art;

- Figure 2 represents the schematic diagram of an illustrative embodiment of a first type of demodulator including a correlator according to the invention;

- Figure 3 represents the more detailed schematic diagram of a correlation macro-cell making up this illustrative embodiment;

- Figure 4 and 5 represent partial diagrams of this macro-cell;

- Figure 6 represents the schematic diagram of a calculating device belonging to this illustrative embodiment;

- Figure 7 represents the schematic diagram of an illustrative embodiment of a second type of demodulator including a correlator according to the invention;

- Figure 8 represents the schematic diagram of a calculating device belonging to this illustrative

embodiment.

The demodulator represented in Figure 1, and which belongs to the prior art, includes:

- two input terminals, 1 and 2, respectively
5 receiving the digital values of two carriers, I and Q, modulated by a pseudo-random function and by an orthogonal M-ary code and which are sampled and digitized;
- a Walsh code generator, 13, having 16 outputs respectively providing 16 binary signals corresponding to
10 16 Walsh codes, and denoted W0, ..., W15;
- a generator 14 providing a pseudo-random binary signal, PN, identical to that which was used to spread the spectrum of the two carrier waves I and Q;
- 16 correlator arrays, 100 to 115, for
15 correlating the carrier I with the 16 reference signals, each array such as the array 100, including four correlators, 5 to 8, each functioning over 64 moments and consisting of an integrated circuit;
- 16 correlator arrays, 200 to 215, for
20 correlating the carrier Q with the 16 reference signals, each array being identical to the array 100;
- a set 9 of sixteen devices for calculating the modulus of a two-component vector;
- a device 10 for detecting the maximum out of 16
25 values.

Each of the arrays 100 to 115 and 200 to 215 can also be made up by means of a single correlator integrated circuit functioning over 256 moments.

The correlator arrays, 100 to 115, respectively
30 provide digital values FI0 to FI15 which are the values of the correlation functions of the carrier I with the sixteen reference signals respectively, over 256 moments. The outputs of the correlator arrays, 200 to 215, respectively provide values FQ0 to FQ15 which are the values of
35 the correlation functions of the carrier Q with the sixteen reference signals respectively, over 256 moments. Each of the calculating devices of the set 9 calculates the modulus of a vector whose components are a value of the correlation function of the carrier I with a

reference signal corresponding to a code, and a value of the correlation function of the carrier Q with the same reference signal. For example, a calculating device from the set 9 calculates the square root of $F_{I0}^2 + F_{Q0}^2$.

5 The set 9 provides the sixteen values, F0 to F15, of the moduli of the correlation functions of the complex signal consisting of the carrier I and of the carrier Q, correlated with the sixteen reference signals. The sixteen values F0 to F15 are compared with one another by
10 the device 10. The latter provides, to an output terminal 19, the index j of the correlation function having the largest modulus. This index j designates the code which modulates the carriers I and Q. The device 10 furthermore provides, to an output terminal 20, the value Fj of the
15 modulus.

This demodulator according to the prior art is complex and bulky since there are 32 correlation arrays in parallel.

Figure 2 represents the schematic diagram of an
20 illustrative embodiment of a demodulator of a first type, including a correlator according to the invention. This demodulator includes 5 sub-sets:

- a multiplexer 23 for alternately transmitting a value of the carrier I and a value of the value [sic]
25 Q, at a tempo twice their sampling frequency;
- a first digital filter 31 matched to the pseudo-random function which spreads the spectrum of the carriers I and Q;
- a second digital filter 35 matched to the
30 sixteen Walsh codes, which may modulate the carriers I and Q in order to transmit a datum; this second filter calculating sixteen values of moduli of correlation functions, F0 to F15, corresponding to the sixteen Walsh codes;
- 35 - a device 34 for selecting the maximum out of these sixteen values, and providing the maximum value Fj to an output terminal 28 and providing the index j, which identifies the modulating code, to an output terminal 29.

The first digital filter, 31, comprises:

- a generator 24 providing a pseudo-random signal, PN, identical to that which was used to spread the spectrum of the complex signal to be demodulated;

- an array of shift registers, 40, including 256
5 stages in total;

- a set 41 of 16 independent registers, each providing in parallel 16 bits and their complements;

- an array 42 of sixteen correlation macro-cells each calculating a partial correlation function value on
10 16 bits;

- a multiplexer 23 having two data inputs, an output, and a control input.

The pseudo-random signal PN constitutes a reference signal REF, for the demodulation. The bits of the
15 signal REF are stored and shifted one by one in the register array 40 under the control of a clock signal CKR, in tempo with their creation by the generator 24. The signal CKR is provided to an input terminal 25 by a conventional clock signal generator which is not represented in the figure. The register array 40 stores 256
20 bits of the reference signal. The contents of these registers are transferred as a block into the register array 41, under the control of a clock signal, load, in synchronism with the clock signal CKS. The period of the
25 signal load is, for example, 10mS [sic], whilst that of CKR is, for example, 30nS [sic]. The clock signal load is provided to an input terminal 26 by a conventional clock signal generator which is not represented in the figure.

The multiplexer 23 is a multiplexer with two
30 inputs and one output, the inputs of which are connected respectively to input terminals 21 and 22 which receive the carriers I and Q to be demodulated, in the form of digital values coded on four bits, the negative values being coded by two's complement. The output of the
35 multiplexer 23 provides a value consisting of four bits: X0, ..., X3, to an input of the array, 42, with sixteen correlation macro-cells. The multiplexer 23 and the correlation macro-cells are controlled by a clock signal CKS, at a tempo twice the sampling tempo of the carriers

I and Q. The clock signal CKS is provided to an input terminal 27 by a conventional clock signal generator which is not represented in Figure 2.

The first correlation cell in the array 42 is a cell 43 which receives the four bits $X_0, \dots, X_3$, alternately representing a value of the carrier I and a value of the carrier Q; and which receives 32 bits $R_0, \dots, R_{15}, \bar{R}_0, \dots, \bar{R}_{15}$, representing 16 bits of the reference signal which are stored in a register of the array 41.

10 The macro-cell 43 retransmits the four bits $X_0, \dots, X_3$ to a following macro-cell, with a delay equal to 16, 17, 18, 19 periods respectively of the clock signal CKS; and provides in succession a value CPI_0 of the partial correlation function corresponding to the signal I, and

15 then a value CPQ_0 of the partial correlation function corresponding to the signal Q.

Each macro-cell is identical to the macro-cell 43 and includes: an input of sixteen bits receiving 16 successive bits of the reference signal and 16 complementary bits; an input of four bits receiving a value of the sequence of multiplexed values of the carriers I and Q;

20 an output retransmitting the four bits of this value to the following macro-cell, with a delay equal to 16, 17, 18, 19 periods respectively of the clock signal CKS; and

25 an output of eight bits providing in succession the value of a first partial correlation function, corresponding to the carrier I, and then the value of a second partial correlation function corresponding to the carrier Q, this output being connected to an input of the device 32 for

30 calculating linear combinations.

The correlator array 42 possesses 16 outputs of 8 bits providing respectively 16 values of partial correlation functions: $CPI_0, \dots, CPI_{15}$, corresponding to the carrier I; then providing respectively 16 values of

35 partial correlation functions: $CPQ_0, \dots, CPQ_{15}$, corresponding to the carrier Q.

The filter 35 includes: a device 32 for calculating linear combinations and a device 33 for demultiplexing and for calculating moduli. The device 32 calculates,

over 256 moments, the value of the correlation function F_{Ii} of the carrier I with the pseudo-random signal PN and with each Walsh code W_i , for $i=0$ to 15; and then calculates, over 256 moments, the value F_{Qi} of the correlation function of the carrier Q with the pseudo-random signal PN and with each Walsh code W_i for $i=0$ to 15; by combining the values $CPI_0, \dots, CPI_{15}$, respectively, $CPQ_0, \dots, CPQ_{15}$ of the partial correlation functions over 16 moments, of the carrier I, respectively of the carrier Q, with the reference signal REF. It should be noted that in this demodulator the reference signal REF consists solely of the pseudo-random signal PN, contrary to the reference signals used in the known device represented in Figure 1.

The device 32 is a device with "pipe-line" structure, controlled by the clock signal CKS. It possesses sixteen outputs of eight bits respectively providing values $FI_0, \dots, FI_{15}$ which are values of the correlation function of the signal I with the reference signal and with the 16 Walsh codes respectively; then providing respectively values $FQ_0, \dots, FQ_{15}$ which are values of the correlation function of the signal Q with the reference signal and with the sixteen Walsh codes respectively.

The device 33 calculates the modulus F_i of the correlation function, over 256 moments, of the complex signal to be demodulated, with the pseudo-random signal and with each Walsh code W_i for $i=0$ to 15.

The device 33 receives and then demultiplexes the values F_{Ii} and F_{Qi} , for $i = 0$ to 15, and calculates the modulus F_i of a vector with components F_{Ii} and F_{Qi} , by determining the square root of $F_{Ii}^2 + F_{Qi}^2$. The device 33 possesses sixteen outputs respectively providing the values $F_0, \dots, F_{15}$, to 16 inputs of the device 34. The device 34 selects the largest value, denoted F_j , out of the values F_i for $i = 0$ to 15, and selects the corresponding index j . This index j designates the Walsh code which is detected by the demodulator, in other words it designates the datum which is transmitted by the signals I and Q. The devices 32, 33 and 34 are also controlled by

the clock signal CKS.

Figure 3 represents the schematic diagram of macro-cell 43, the other macro-cells of the array 42 being identical to the macro-cell 43. Each macro-cell has a systolic structure, consisting of a matrix of 128 identical cells functioning on a single bit. This matrix includes 8 lines of 16 cells. The first cell, 49, of the first line of cells receives a bit X0 of a value of the carrier I or Q. This bit X0 is transferred from one cell to another of the first line, each with a delay equal to one period of the clock CKS. The first cell of the second line of the matrix receives the bit X1 with a delay equal to one period of the clock CKS, relative to the bit X0. This delay is effected by a D flip-flop 57. The cells of the second line retransmit the bit X1, each with a delay equal to one period [lacuna] the clock CKS.

The first cell of the third line receives the bit X2 with a delay equal to two periods of the clock CKS, a delay effected by a set 58 consisting of two D flip-flops. The cells of the third line retransmit the bit X2, each with a delay equal to one period of the clock CKS. The first cell of the third line receives the bit X3 with a delay equal to three periods of the clock CKS, a delay effected by a set 59 of three D flip-flops. The cells of the third line retransmit the bit X3, each with a delay equal to one period of the clock CKS.

The first cell of the fourth line receives the bit X3 with a delay equal to three periods of the clock CKS, a delay effected by a set 59 of three D flip-flops. Each cell of the fourth line pretransmits the bit X3 with a delay equal to one clock period CKS.

The first cell of the fifth line receives the bit X3 with a delay equal to four periods of the clock CKS, a delay effected by a set 60 of four D flip-flops. Each cell of the fifth line retransmits the bit X3 with a delay equal to one period of the clock CKS. The first cell of the eighth line receives the bit X3 with a delay equal to seven periods of the clock signal CKS, a delay effected by a set 63 of seven D flip-flops. Each cell of

the eighth line retransmits the bit X3 with a delay equal to one period of the clock CKS. The first cell of the sixth line receives the bit X3 with a delay equal to five periods of the clock CKS, a delay effected by a set 61 of
5 five D flip-flops. Each cell of the sixth line retransmits the bit X3 with a delay equal to a period of the clock CKS. The first cell of the seventh line receives the bit X3 with a delay equal to six periods of the clock signal CKS, a delay effected by a set 62 of six
10 D flip-flops. Each cell of the seventh line retransmits the bit X3 with a delay equal to one period of the clock CKS. The last cell of each line therefore provides one of the bits X0, X1, X2, X3, with a delay dependent on the rank of the line, to an input of the following macro-cell
15 in the array 42.

Each cell possesses an input receiving a partial correlation result bit provided by an output, termed the partial correlation result, belonging to the next cell. In this example, there is never an overflow of the
20 capacity of a macro-cell, and consequently there is no provision for transmitting result bits from one macro-cell to another. The partial correlation result bit inputs of the last cells respectively receive bits C0, ..., C7 having a zero value.

25 All the cells of the first column, all the cells of the second column etc., respectively receive the bits R15 and $\bar{R}15$, ..., R0 and $\bar{R}0$, of the reference signal. A carry input, of the first cell of the first column, receives the bit $\bar{R}15$ and provides a carry bit to the
30 following cell in the same column. The following cell in turn provides a carry bit to another following cell, each time with a delay equal to one period of the clocks CKS. Similarly, in the succeeding columns, a carry input of the first cell receives respectively $\bar{R}14$, ..., $\bar{R}0$, and
35 the cells of the following lines provide carry bits to the cells of the next line.

The partial correlation result output of each cell of the first column provides a result bit from correlation over 16 moments. The first cell of the first

line provides a bit S0, by way of a set 50 of seven D flip-flops effecting a delay equal to seven periods of the clock CKS. The first cell of the second line provides a bit S1, by way of a set 51 of six D flip-flops effecting a delay equal to six periods of the clock signal CKS. The first cell of the third line provides a bit S2, by way of a set 52 of five D flip-flops effecting a delay equal to five periods of the clock CKS. The first cell of the fourth line provides a bit S3 by way of a set 53 of four D flip-flops effecting a delay equal to four periods of the clock signal CKS. The first cell of the fifth line provides a bit S4 by way of a set 54 of three D flip-flops effecting a delay equal to three periods of the clock CKS. The first cell of the sixth line provides a bit S5 by way of a set 55 of two D flip-flops effecting a delay equal to two periods of the clock CKS. The first cell of the seventh line provides a bit S6 by way of one D flip-flop, 56, effecting a delay equal to one period of the clock CKS. The first cell of the eighth line provides a bit S7 directly.

Figure 4 represents the more detailed schematic diagram of one of the cells, 50, of the correlation macro-cell 43. Cell 50 includes:

- an exclusive NOR gate, 70, having a first input receiving a bit R of the reference signal, this bit being furthermore transmitted, without modification, to the next cell in the same column, and having a second input receiving a bit Xin of a value of the carrier I or of the carrier Q;
- an adder 71, having a first input which receives a bit Sin, which is a partial correlation result provided by the next cell in the same line, and having a second input connected to the output of the gate 70;
- a first D flip-flop, 72, having an input receiving the bit Xin; having a control input receiving the clock signal CKS; and having an output providing a bit Xout which is the previous value of the bit Xin, to the next flip-flop in the same line;
- a second D flip-flop, 73, having an input

connected to the output of the adder 71; having a control input receiving the clock signal CKS; and having an output providing a bit Sout which is a partial correlation result constituting one bit of the value of one of the partial correlation functions of the carriers I and Q;

- a third D flip-flop, 74, having an input connected to a carry output of the adder 71; having a control input receiving the clock signal CKS; and having an output providing one bit, Cout, which constitutes a carry for the next cell in the same column.

Figure 5 illustrates the operation of one line of the matrix of cells of the macro-cell 43, for calculating the value of bit S5 of the partial correlation function of the carrier I or Q. This line consists of sixteen cells 79, 78, 77, ..., 76. The first cell 79, receives, at the instant considered, the bit X(20) provided by the output of the set 60 of four D flip-flops. At the same instant, this set 60 receives, on its input, a bit X(24). The bits X are retransmitted in succession by each of the cells of the line, each time adding a delay equal to one period of the clock CKS. Consequently, the cells of the line respectively receive the bits X(20), X(19), X(18), X(17), ..., X(5) at the instant considered.

The values are applied respectively to the exclusive NOR gates of each of the cells so as to form the product of these bits with the bits R15, ..., R0 of the reference signal. In each cell, the result of the product is applied to the first input of the adder which adds to it the value of a carry bit provided by the homologous cell in the preceding line, and which also adds to it the partial correlation result bit provided by the next cell in the same line. For example, in cell 79, the carry bit C15 is added to the result of the product X(20).R15 and to the bit Sout 14.

The second input of each adder receives a partial correlation result bit provided by the output of the adder of the next cell, by way of a D flip-flop. Each adder moreover provides a carry bit, C15', ..., C0',

respectively, to the cells of the next line. The output of the adder of the first cell, 79, provides the value of the bit S5, by way of the D flip-flop which includes its cell, and of the set 54 of three D flip-flops effecting a delay equal to two periods of the clock CKS. The value of the bit S5 is thus equal to the sum of $R_i.X(i+5)+C_i$, for $i = 0$ to 15.

Figure 6 represents a schematic diagram of the device 32 for calculating linear combinations, determining in succession a value of a first partial correlation function for the signal I, then a value of a second partial correlation function for the signal Q, for the sixteen Walsh codes. The device 32 possesses sixteen inputs respectively receiving CPI0, ..., CPI15, in that order; then CPQ0, ..., CPQ15, in that order. This device 32 has a "pipe-line" structure including four lines of operators, each operator calculating a linear combination of two intermediate values determined by two operators of the preceding line. Each operator is: either an adder followed by a register, or a subtractor followed by a register. The registers are controlled by the clock signal CKS.

The first line consists of pairs of operators: one adder and one subtractor, taken in that order, and respectively calculating the sum and the difference of two values applied respectively to two neighbouring inputs of the device 32.

The operators of the second line, constitute four identical groups each including two adders and then two subtractors. Each of the adders adds the value provided by the operator situated above it and the intermediate value provided by the operator situated two ranks further on in the line above. Each subtractor calculates the difference between the intermediate value provided by the operator situated above it and the intermediate value provided by the operator situated two ranks earlier, in the preceding line.

The operators of the third line constitute two identical groups each including four adders and then four

subtractors. Each adder calculates the sum of the intermediate value provided by the operator situated above it and of the intermediate value provided by the operator situated four ranks further on in the preceding line. Each subtractor calculates the difference between the intermediate value provided by the operator situated above it and the intermediate value provided by the operator situated four ranks earlier in the preceding line.

10 The fourth line of operators consists of eight adders and then eight subtractors. Each adder calculates the sum of the intermediate value provided by the operator situated above it and of the intermediate value provided by the operator situated eight ranks further on in the preceding line. Each subtractor calculates the difference between the intermediate value provided by the operator situated above it and the intermediate value provided by the operator situated eight ranks earlier in the preceding line. The outputs of the eight adders and of the eight subtractors of the fourth line provide respectively the values FI0, FI15, FI7, FI8, FI3, FI12, FI4, FI11, FI1, FI14, FI6, FI9, FI2, FI13, FI5, FI10, of the correlation function of the carrier I, and then provide the values FQ0, FQ15, FQ7, FQ8, FQ3, FQ12, FQ4, FQ11, FQ1, FQ14, FQ6, FQ9, FQ2, FQ13, FQ5, FQ10 of the correlation function of the carrier Q.

Figure 7 represents the schematic diagram of an illustrative embodiment of a demodulator of a second type, also including a correlator according to the invention. The elements which are identical to the elements of the first illustrative embodiment bear the same reference but with the index '. This illustrative embodiment includes a first digital filter 88 including in particular: two register arrays 40 and 41' a multiplexer 23' and an array 42' of correlation macro-cells, which are identical to the elements described earlier.

The reference signal REF' differs from the signal REF. It is provided by the output of an exclusive OR gate, 82, which forms the product of a pseudo-random

signal PN and of a Walsh code signal W_i . A generator 80 provides the pseudo-random signal PN, which is identical to that which was used to modulate the signals I and Q to be demodulated. A generator 81 provides the Walsh code
5 signal W_i . In this second type of demodulator, the reference signal REF' is therefore matched to a Walsh code chosen from among the M possible codes. This particular feature makes it possible to simplify the second filter, matched to the Walsh coding.

10 The filter matched to the Walsh coding is constructed from a matched filter 89 comprising: a device 83 for calculating linear combinations; a device 85 for demultiplexing and for calculating the correlation function for the Walsh code W_i ; and a device 84 for
15 demultiplexing and for calculating the correlation function for another Walsh code W_h which is related to the code W_i . The index h is related to the index i through the following relation: $h = M-i$.

For example, if the generator 81 provides the
20 Walsh code W_0 , the devices 85 and 84 respectively provide the values F_0 and F_{15} of the correlation function, for the Walsh code W_0 and for the Walsh code W_{15} respectively. If the generator 81 provides the Walsh code W_1 , the outputs of the devices 85 and 84 respectively provide the
25 correlation functions F_1 and F_{14} corresponding respectively to the Walsh code W_1 and to the Walsh code W_{14} . The demodulator can therefore, at a given instant, detect only two codes out of the 16 Walsh codes, but this is sufficient in certain applications and, on the other
30 hand, allows a major simplification of the calculating device 83, as will emerge later.

The calculating device 83 possesses sixteen inputs of eight bits, connected respectively to sixteen outputs of the array 42' of correlation macro-cells.
35 These inputs respectively receive the values CPI_0' , ..., CPI_{15}' of the partial correlation functions of the carrier I with the reference signal, and then the values CPQ_0' , ..., CPQ_{15}' , of the partial correlation functions of the carrier Q with the reference signal. The device 83

possesses two outputs of eight bits, connected respectively to an input of the device 85 so as to provide it with a value F_{Ii} and then a value F_{Qi} of the correlation function of the carrier I, respectively, of the carrier Q, for the Walsh code W_i ; and a second output connected to an input of the device 84 so as to provide it with a value F_{Ih} and then a value F_{Qh} of the correlation function of the carrier I, respectively of the carrier Q, for the Walsh code W_h .

10 The device 85 demultiplexes the values F_{Ii} and F_{Qi} and then calculates the modulus of a vector having these values as components. This modulus constitutes the value F_i of the correlation function of the complex signal to be demodulated. The value F_i is provided to an
15 input of a device 90 for detecting a maximum.

 The device 84 demultiplexes the values F_{Ih} and F_{Qh} and then calculates the modulus of a vector having these values as components. The value F_h of this modulus constitutes the value of the correlation function of the
20 complex signal to be demodulated, for the Walsh code W_h . The value F_h is applied to a second input of the device 90. The device 90 possesses two outputs connected respectively to two output terminals, 86 and 87, of the demodulator so as to provide respectively two values j and F_j
25 which are respectively the index and the value of the larger of the two values F_i and F_h . The value j , which can be equal only to i or h , represents a transmitted datum. The devices 83, 84, 85 are controlled by a clock signal CKS' , at a tempo twice the tempo of sampling of
30 each of the carriers I and Q. The clock signal CKS' is provided by a conventional clock signal generator, which is not represented in Figure 7.

 Figure 8 represents the schematic diagram of the device 83 for calculating linear combinations. It has a
35 "pipe-line" structure including four lines of operators which are all adders except one which is a subtractor. Each operator is followed by a register controlled by the clock signal CKS' , and which is not represented in the figure. The first line of operators includes four adders,

91 to 94, each forming the sum of two even-rank partial correlation function values; and includes four adders 98 to 101, each forming the sum of two odd-rank partial correlation function values.

5 The second line of operators includes an adder 95 which adds up the intermediate values provided by the operators 91 and 92, an operator 96 which adds up the intermediate values provided by the adders 93 and 94, an adder 102 which adds up the intermediate values provided
10 by the adders 98 and 99, and an adder 103 which calculates the sum of the intermediate values provided by the adders 100 and 101.

 The third line includes an adder 97 which calculates the sum of the intermediate values provided by the
15 adders 95 and 96; and includes an adder 104 which calculates the sum of the intermediate values provided by the adders 102 and 103.

 The fourth line includes an adder 105 which calculates the sum of the intermediate values provided by
20 the adder 97 and by the adder 104; and includes a subtractor 106 which calculates the difference between the intermediate value provided by the adder 97 and the intermediate value provided by the adder 104.

 It can be easily verified that the adder 105 thus
25 provides a value equal to the sum of all the partial correlation function values applied to the inputs of the device 83, while the subtractor 106 provides the value of the difference between the sum of the values of the partial correlation functions having an even rank and the
30 sum of the partial correlation functions having an odd rank. The output of the adder 105 constitutes the output of the device 83 which provides the value F_{Ii} , and then the value F_{Qi} , of the correlation function of the carrier I, respectively of the carrier Q, for the Walsh code W_i .
35 The output of the subtractor 106 constitutes the output of the device 83 which provides the value F_{Ih} , and then the value F_{Qh} , of the correlation function of the carrier I, respectively, of the carrier Q, for the Walsh code W_h .

As emerges from the diagram of Figure 8, the

calculating device 83 is simpler to produce than the calculating device 32 represented in Figure 6. The second type of demodulator has a sufficiently simple diagram for it to be possible to integrate it fully into a single
5 integrated circuit, by using known technology allowing a 1.25 micron row width. It therefore allows a much simpler construction than the conventional correlator devices described earlier.

The invention is applicable in particular to the
10 construction of MSK, PSK or QPSK demodulators, with spread spectrum and orthogonal M-ary coding, for on-board aeronautical hardware for which bulk must be as small as possible.



CLAIMS

1. Asynchronous digital correlator for correlating a binary reference signal (REF), with a complex signal consisting of a first and a second carrier (I, Q) which are modulated by a pseudo-random function (PN) and by an M-ary orthogonal Walsh coding, these two carriers being sampled and digitized, characterized in that it includes:
 - a multiplexer (23) for transmitting alternately a value (I) of the first carrier and a value (Q) of the second carrier, with a period equal to half their sampling period;
 - a first digital filter (31) matched to the pseudo-random function (PN), including an array of registers (41) for storing L consecutive bits of the reference signal (REF) and an array (42) of M correlation macro-cells (43) receiving the sequence of the multiplexed values of the first and of the second carrier (I, Q), each macro-cell (43) calculating the value (CPI0, ..., CPI15) of a first function, termed partial correlation, between N bits of the reference signal and N values of the first carrier (I), then calculating the value (CPQ0, ..., CPQ15) of a second function, termed partial correlation, between N bits of the reference signal and N values of the second carrier (Q), N being equal to L/M;
 - a second digital filter (35) including calculating means (32) for determining the value of linear combinations of the values of the first partial correlation functions (CPI0, ..., CPI15), then of linear combinations of the values of the second partial correlation functions (CPQ0, ..., CPQ15), which means are matched to the Walsh codes, the coefficients of the linear combinations being unchanged and being equal to ± 1 ; and including means (33) for demultiplexing the values of the linear combinations (FII, FQI), and determining the modulus (Fi) of a vector having the values of these two linear combinations (FII, FQI) as components.
2. Correlator according to Claim 1, characterized in that each correlation macro-cell (43) has a systolic structure, including: a plurality of lines of N



correlation cells (49) each cell receiving a bit (X_0 , ..., X_3) of the multiplexed values (I , Q) and retransmitting this bit to a neighbouring cell in the same line, with a delay equal to one sampling half-period; receiving a bit ($\bar{R}_{15}$, R_{15} , ..., $\bar{R}_0$, R_0) of the reference signal and retransmitting this bit to a homologous cell in the following line; receiving a carry bit (C_{in}) provided by a homologous cell in the preceding line; providing, with a delay equal to a sampling half-period, a carry bit (C_{out}) to a homologous cell in the following line; receiving a partial correlation result bit (S_{in}) provided by the cell following it in the same line; providing with a delay equal to a sampling half-period, a partial correlation result bit (S_{out}) to the cell preceding it in the same line;

in that each line of N correlation cells furthermore includes:

- an array of registers (50, ..., 56) for delaying the partial correlation result bit (S_0 , ..., S_7) which it provides, by a delay dependent on the rank of the line in the macro-cell (43);

- an array of registers (57, ..., 63) for delaying the bit (X_0 , ..., X_3) of the multiplexed values (I , Q) which it receives, by a delay dependent on the rank of the line in the macro-cell (43).

3. Correlator according to Claim 2, characterized in that each correlation cell (49) includes:

- an exclusive OR gate (70), one input of which receives a bit (X_{in}) of a value (I , Q) of the multiplexed signals, and one input of which receives a bit (R) of the reference signal;

- a flip-flop (72), retransmitting said bit (X_{in}) of a value of the multiplexed signals, under the control of a clock signal (CKS) at a frequency twice the sampling frequency;

- an adder (71) one input of which is connected to the output of the exclusive OR gate (70); one input of which receives a partial correlation result bit (S_{in}) provided by the following cell in the same line; and one



input of which receives a carry bit (Cin) provided by the homologous cell in the preceding line;

- a flip-flop (73) retransmitting a partial correlation result bit (Sout) provided by a first output of the adder (71), under the control of the clock signal (CKS);

- a flip-flop (74) retransmitting a carry bit (Cout) provided by a second output of the adder (72), under the control of the clock signal (CKS).

10 4. Digital demodulator for demodulating a complex signal consisting of a first and a second carrier (I, Q), in quadrature, whose spectrum is spread by a pseudo-random function and which are modulated by an M-ary orthogonal coding, according to a PSK, or MSK, or QPSK modulation;

15 characterized in that it includes an asynchronous digital correlator for correlating a binary reference signal (REF), with a complex signal consisting of a first and a second carrier (I, Q) which are modulated by a pseudo-random function and by an M-ary orthogonal Walsh coding, these two carriers being sampled and digitized, the said correlator including:

20 - a multiplexer (23) for transmitting alternately a value (I) of the first carrier and a value (Q) of the second carrier, with a period equal to half their sampling period;

25 - a first digital filter (31) matched to the pseudo-random function (PN), including an array of registers (41) for storing L consecutive bits of the reference signal (REF) and an array (42) of M correlation macro-cells (43) receiving the sequence of the multiplexed values of the first and of the second carrier (I, Q), each macro-cell (43) calculating the value (CPI0, ..., CPI15) of a first function, termed partial correlation, between N bits of the reference signal and N values of the first carrier (I), then calculating the value (CPQ0, ..., CPQ15) of a second function, termed partial correlation, between N bits of the reference signal and N values of the second carrier (Q), N being equal to L/M;



- a second filter (35) including means (32) for calculating the values of a first and of a second linear combination (F_{In} , F_{Qn}) of partial correlation functions, demultiplexing these two values and calculating the
5 modulus (F_n) of a vector having these two values as components, for each of the M Walsh M -ary codes,

- and in that it furthermore includes means (34) for determining the largest modulus (F_j) among these M moduli and deducing therefrom which is the code (j) which
10 modulates the two carriers (I , Q).

5. Digital demodulator for demodulating a complex signal consisting of a first and a second carrier, in quadrature, whose spectrum is spread by a pseudo-random function and which are modulated by an M -ary orthogonal
15 coding, according to a PSK, or MSK, or QPSK modulation;

characterized in that it includes an asynchronous digital correlator for correlating a binary reference signal (REF), with a complex signal consisting of a first and a second carrier (I , Q) which are modulated by a
20 pseudo-random function and by an M -ary orthogonal Walsh coding, these two carriers being sampled and digitized,

- a generator (80) providing a pseudo-random binary signal identical to that having been used to spread the spectrum;

25 - a generator (81) of M -ary orthogonal codes providing a binary signal (W_i) according to one of these codes;

- an exclusive OR gate (83) for providing the correlator with a reference signal (REF') consisting of
30 the product of the binary signals (PN , W_i) provided by the two generators (80, 81) respectively;

the correlator including:

- a multiplexer (23) for transmitting alternately a value (I) of the first carrier and a value (Q) of the
35 second carrier, with a period equal to half their sampling period;

- a first digital filter (31) matched to the pseudo-random function (PN), including an array of registers (41) for storing L consecutive bits of the



reference signal (REF) and an array (42) of M correlation macro-cells (43) receiving the sequence of the multiplexed values of the first and of the second carrier (I, Q), each macro-cell (43) calculating the value (CPI0, ..., CPI15) of a first function, termed partial correlation, between N bits of the reference signal and N values of the first carrier (I), then calculating the value (CPQ0, ..., CPQ15) of a second function, termed partial correlation, between N bits of the reference signal and N values of the second carrier (Q), N being equal to L/M;
- a second filter (89) including means (83, 84) for calculating the values (FII, FQI) of a first and of a second linear combination of partial correlation functions, demultiplexing these two values and calculating the modulus (F_1) of a vector having these two values as components, for at least one of the M-ary codes (W_i , W_h).

6. Demodulator according to Claim 5, for demodulating a complex signal consisting of a first and a second carrier (I, Q), in quadrature, whose spectrum is spread by a pseudo-random function, and which are modulated by an M-ary Walsh coding, characterized in that the means (83) for calculating successively the value (FII, FQI) of a first and of a second linear combination of the partial correlation functions (CPI0', ..., CPI15', CPQ0', ..., CPQ15') include:

- a plurality of adders (91 to 97) for adding all the values (CPI0', CPI2', ..., CPI14'; CPQ0', CPQ2', ..., CPQ14') of the partial correlation functions having an even rank;

- a plurality of adders (98 to 103) for adding all the values (CPI1', CPI3', ..., CPI15'; CPQ1', CPQ3', ..., CPQ15') of the partial correlation functions having an odd rank;

- an adder (105) for adding the values provided by these two pluralities of adders and thus providing successively the value (FII, FQI) of a first and of a second component of the correlation function for a first Walsh code (W_i) which is that provided by the code



generator (81);

- a subtractor (106) for subtracting amongst them
the values provided by the two pluralities of adders and
thus providing successively the value (FIh, FQh) of a
5 first and of a second component of the correlation
function for a second Walsh code (Wh).