

FIG. 1

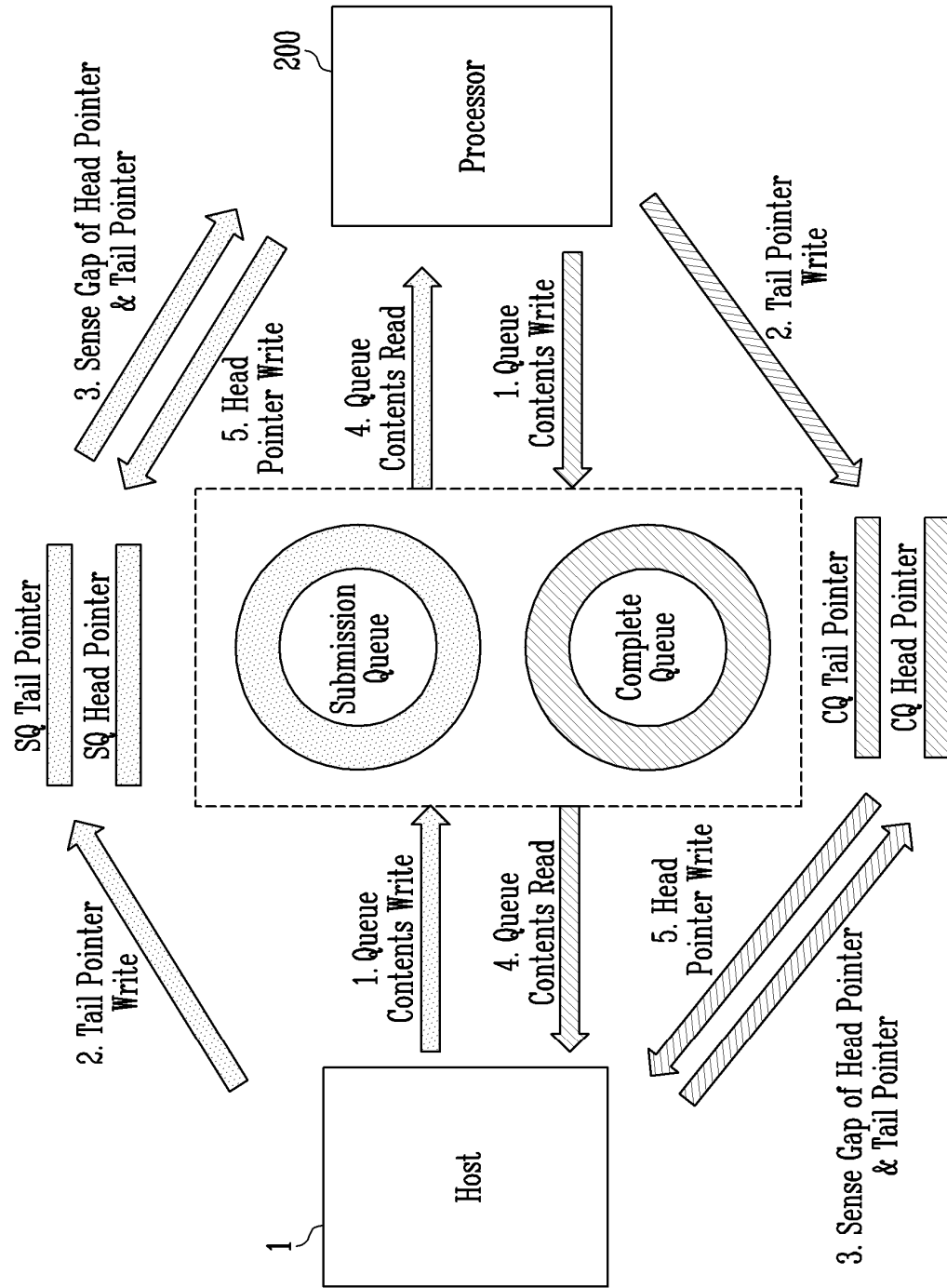


FIG. 2

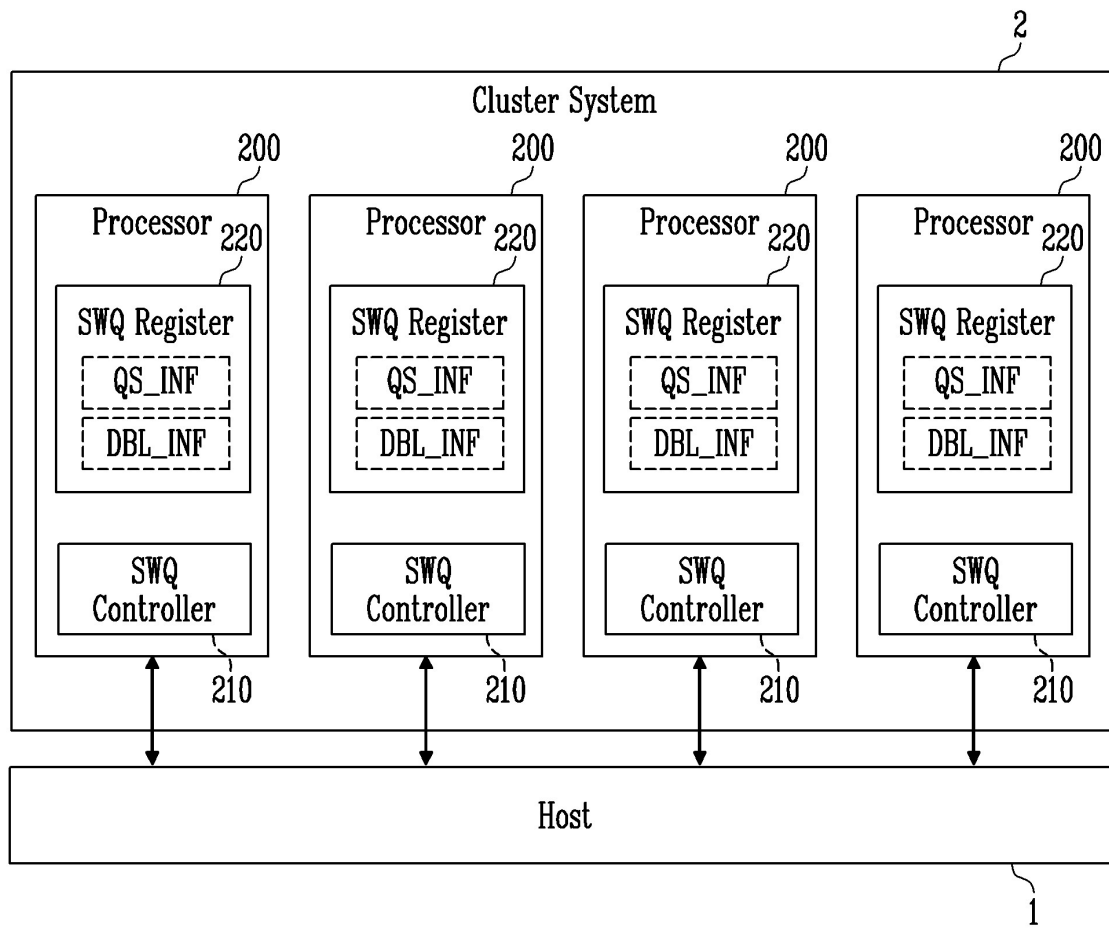


FIG. 3

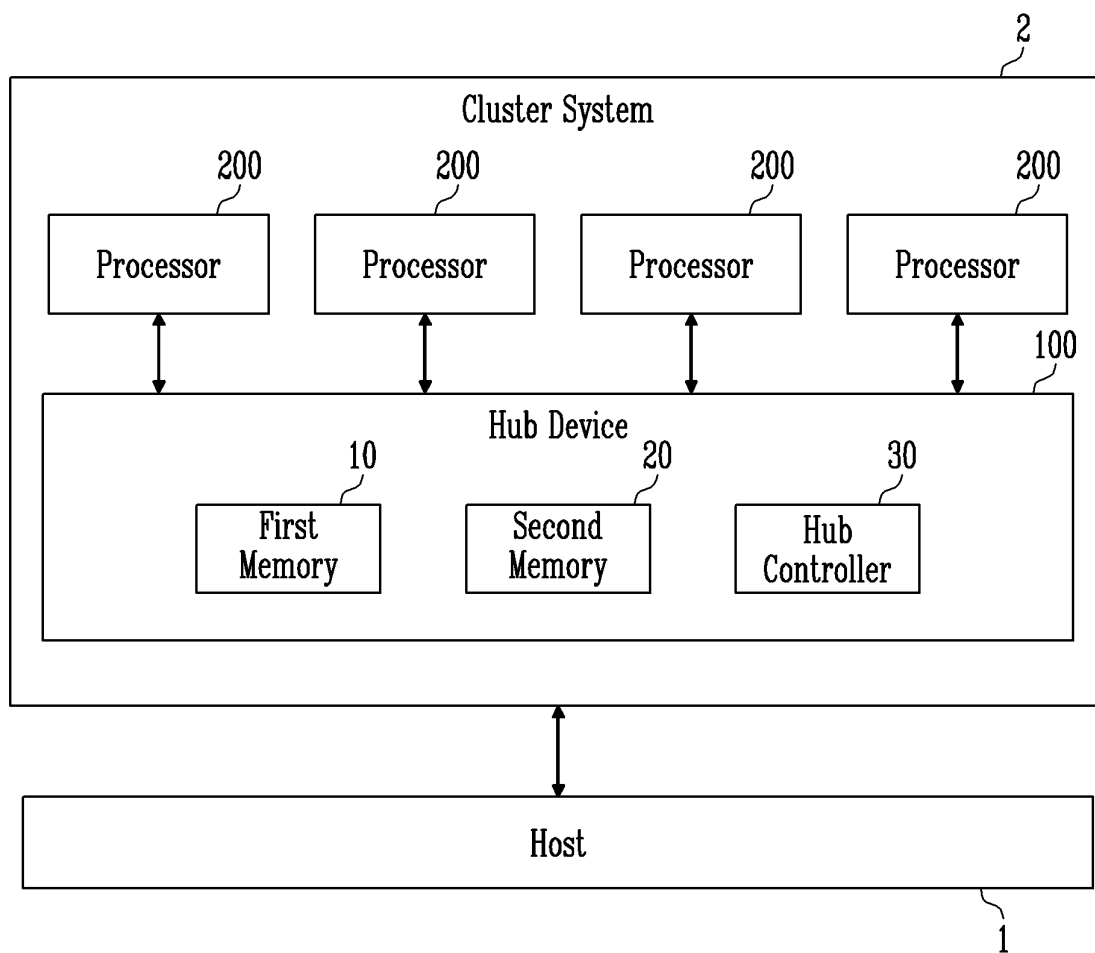


FIG. 4

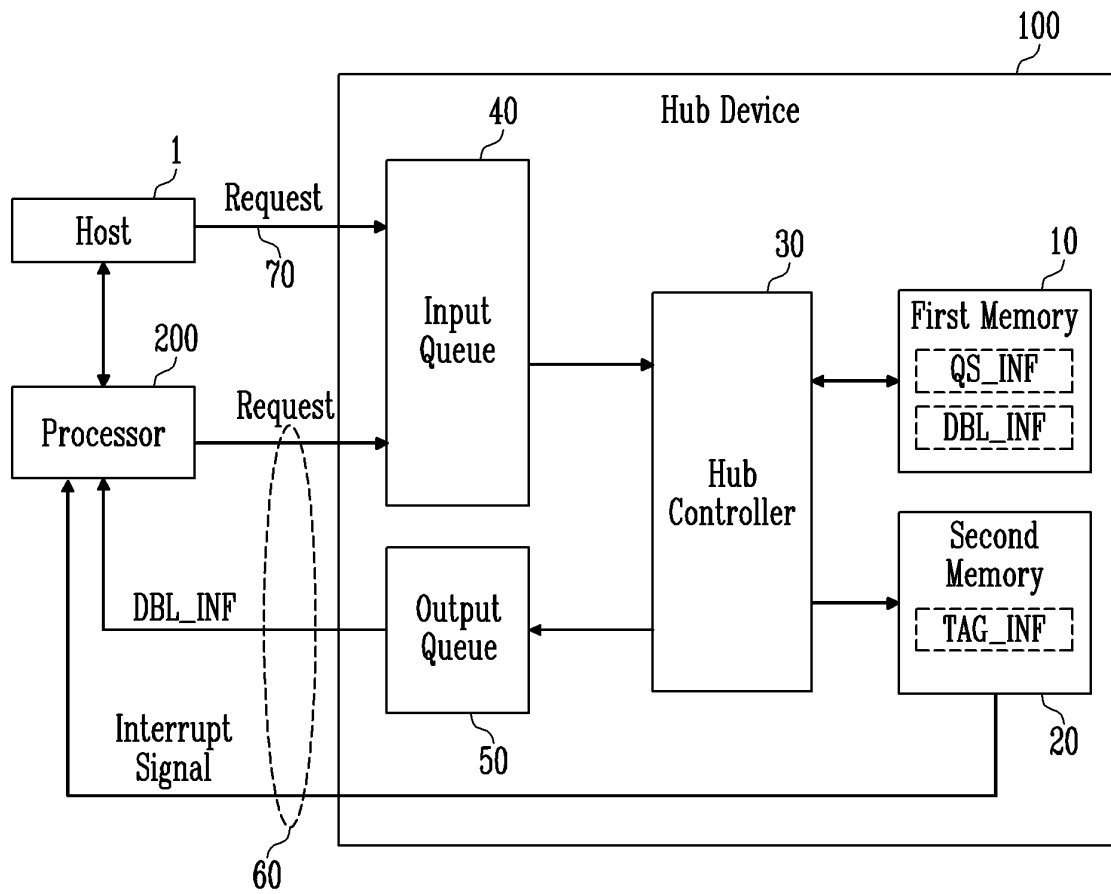


FIG. 5A

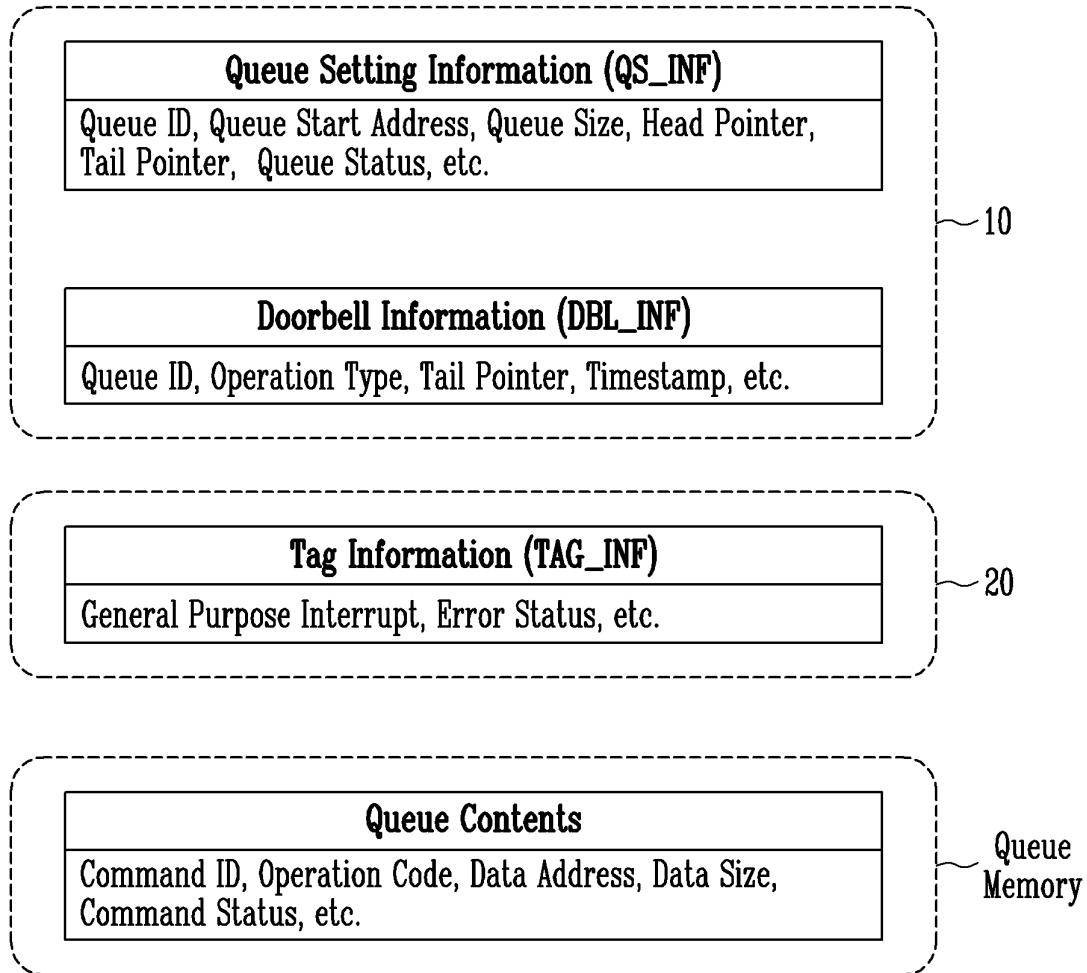


FIG. 5B

Processor #	SWQ #	QS_INF	DBL_INF
Processor 1	SWQ 1	QS_INF 1	DBL_INF 1
	SWQ 2	QS_INF 2	DBL_INF 2
	SWQ 3	QS_INF 3	DBL_INF 3
	SWQ 4	QS_INF 4	DBL_INF 4
Processor 2	SWQ 1	QS_INF 5	DBL_INF 5
	SWQ 2	QS_INF 6	DBL_INF 6
	SWQ 3	QS_INF 7	DBL_INF 7
	SWQ 4	QS_INF 8	DBL_INF 8

FIG. 6

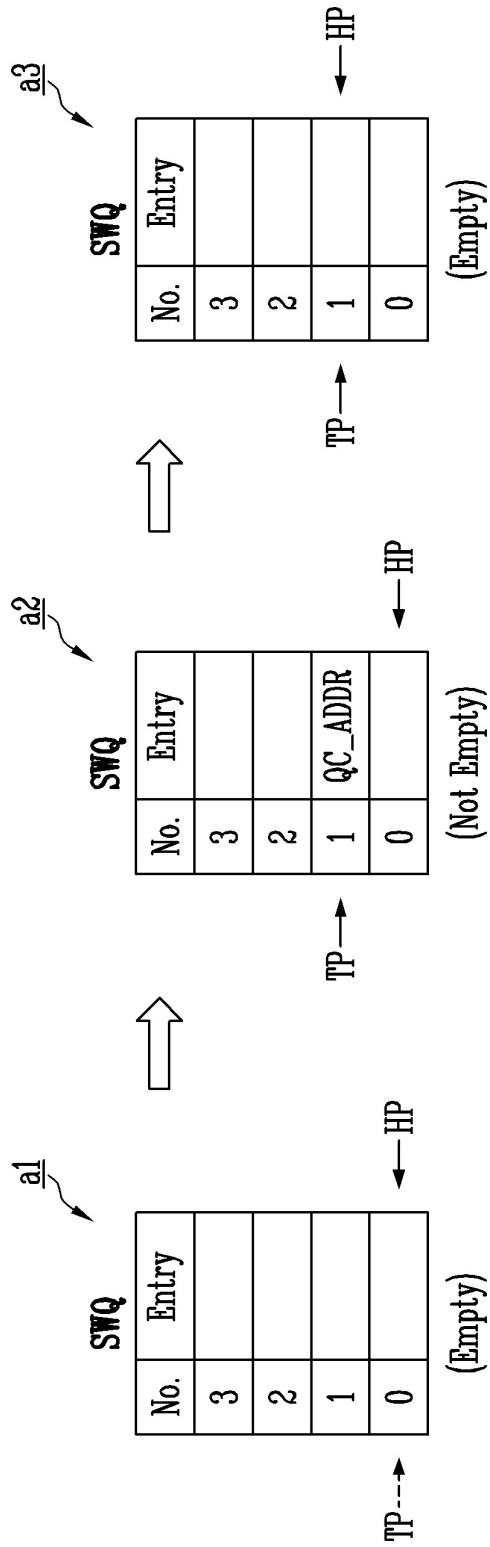


FIG. 7

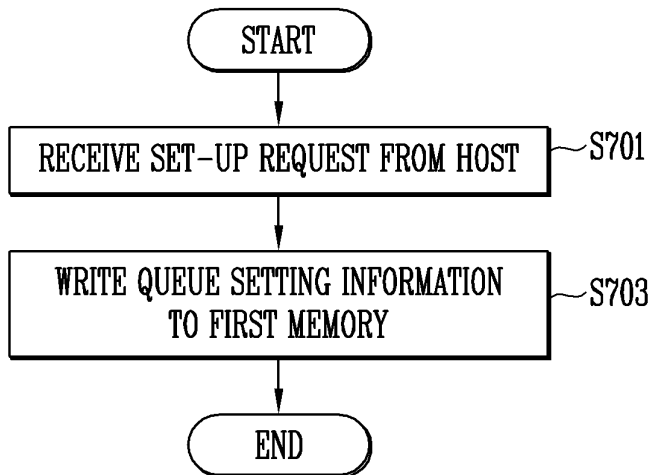


FIG. 8

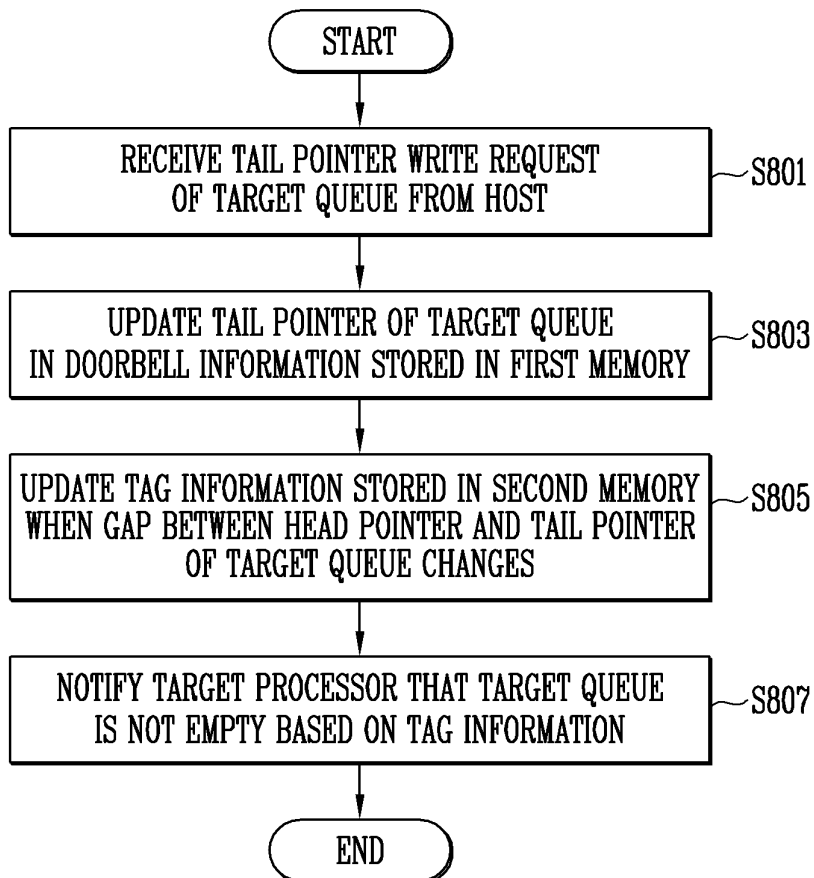


FIG. 9

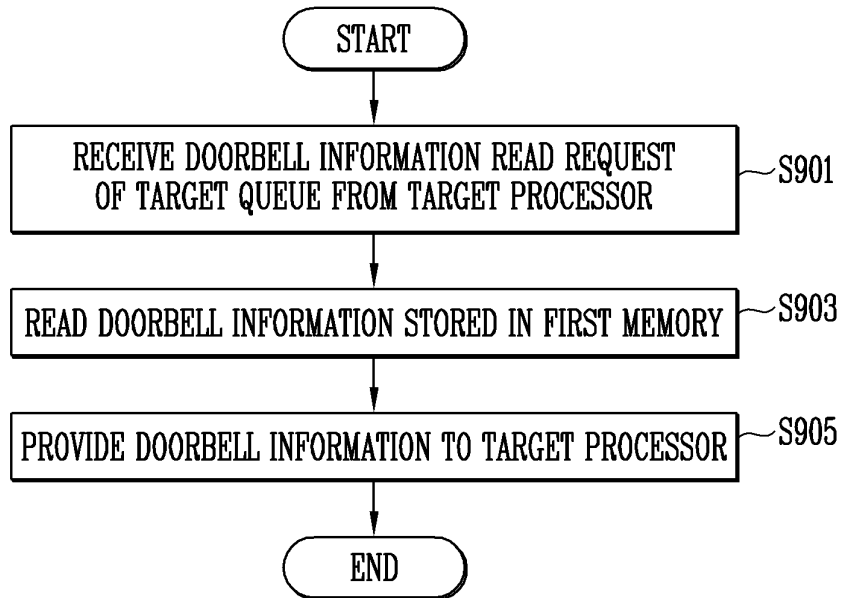


FIG. 10

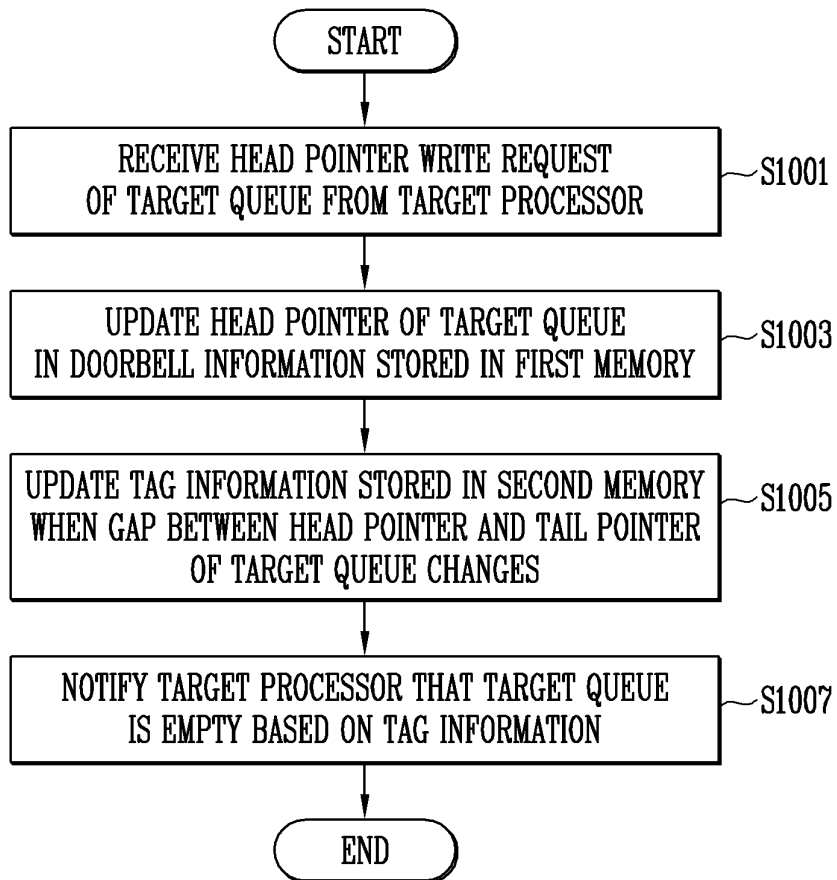


FIG. 11

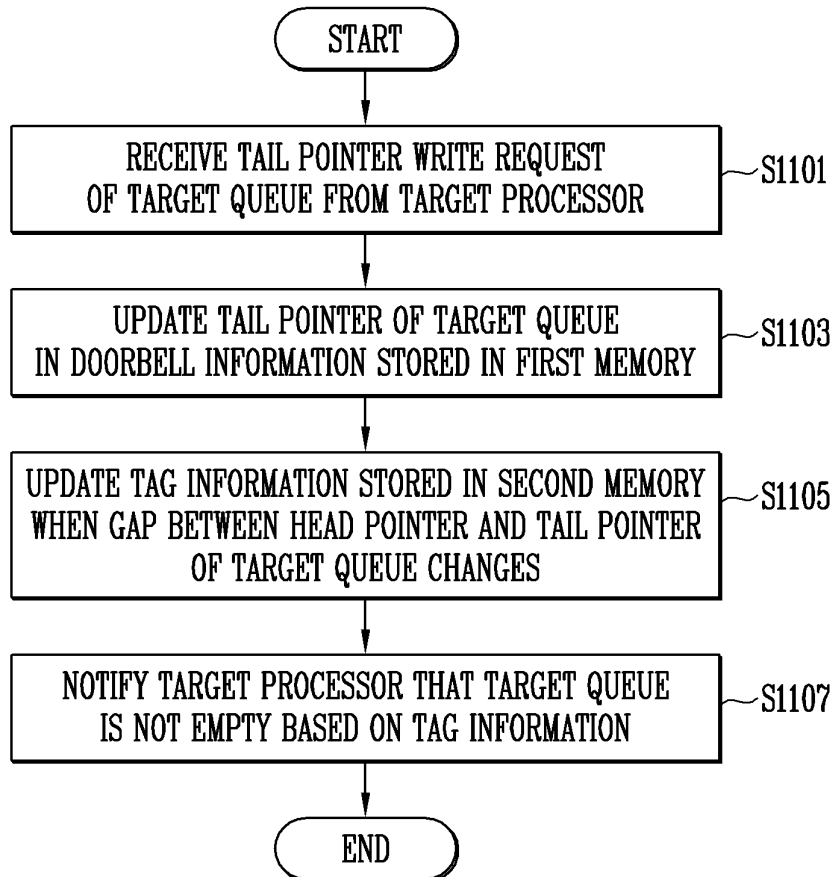


FIG. 12

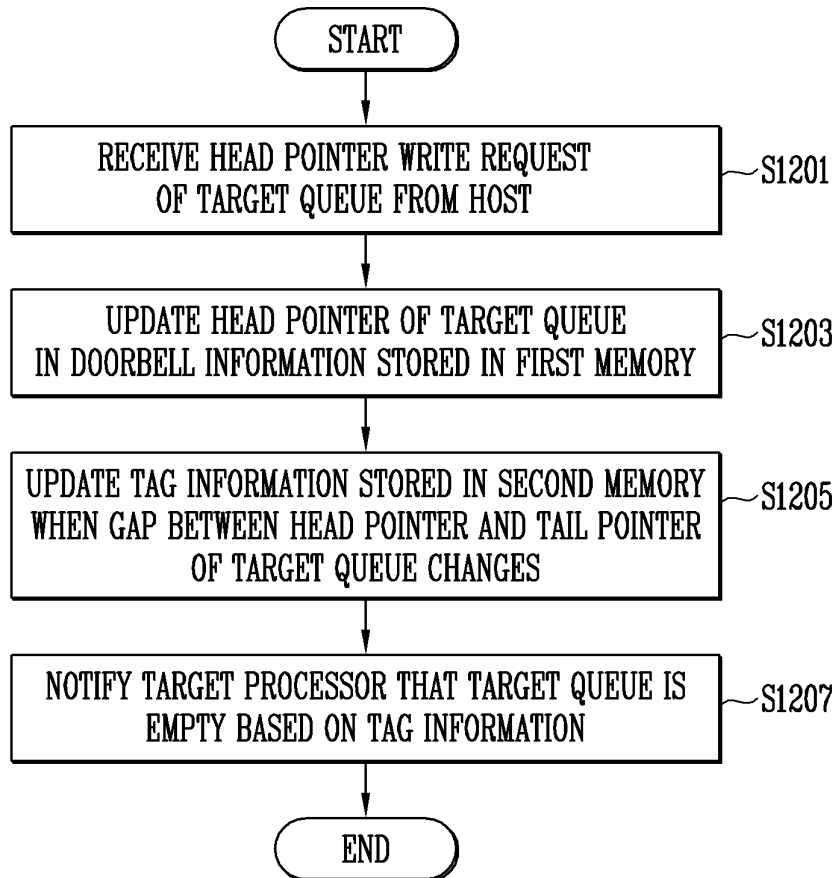


FIG. 13

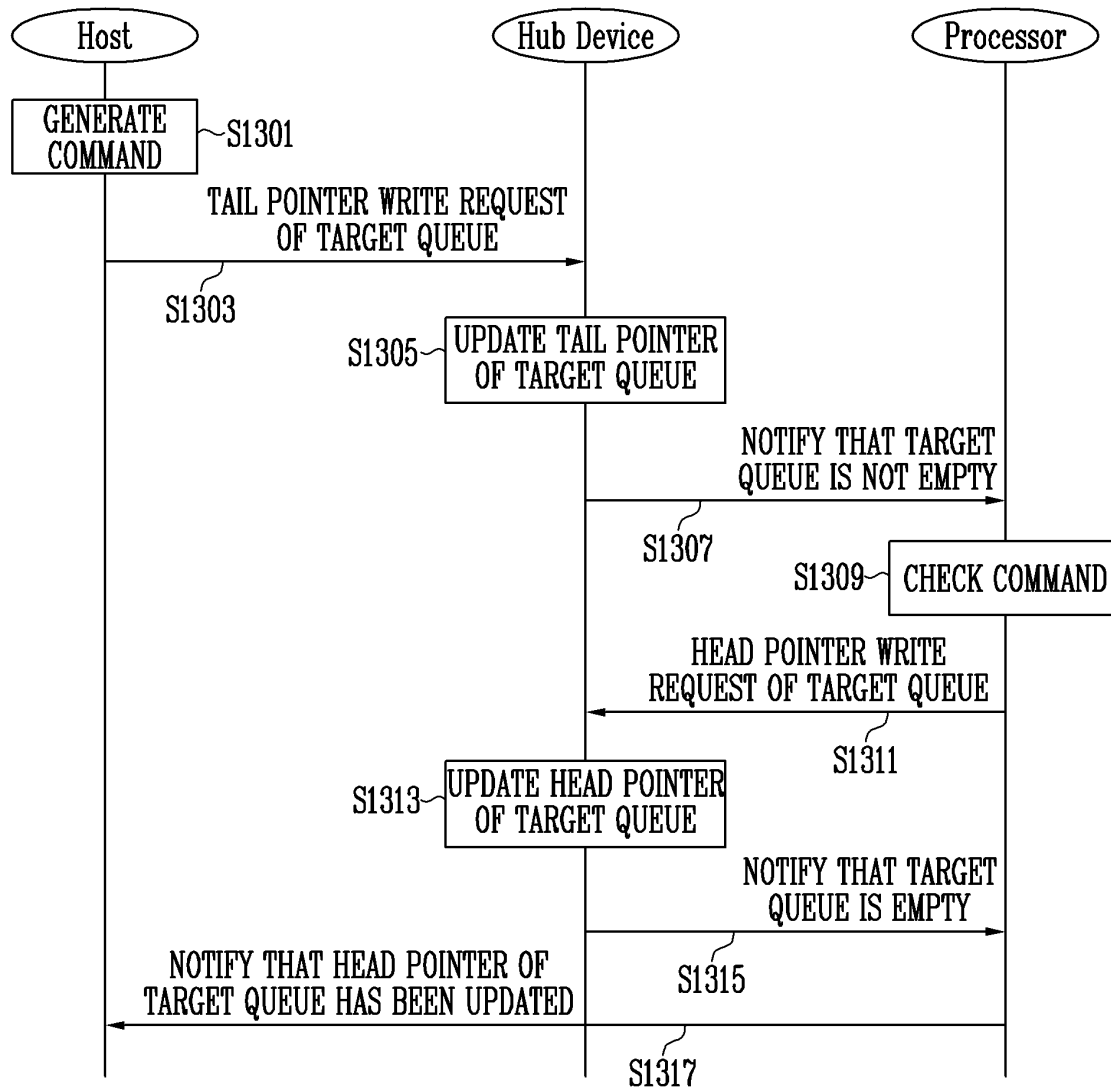


FIG. 14

