PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : G06F 17/30

A2

(11) International Publication Number: WO 00/29981

(43) International Publication Date: 25 May 2000 (25.05.00)

(21) International Application Number: PCT/NO99/00344

(22) International Filing Date: 12 November 1999 (12.11.99)

(30) Priority Data:
19985315 13 November 1998 (13.11.98) NO

(71) Applicant *(for all designated States except US)*: FAST SEARCH & TRANSFER ASA [NO/NO]; P.O. Box 1677 Vika, N–0120 Oslo (NO).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: SVINGEN, Børge [NO/NO]; Borkdalen 6, N–7550 Hommelvik (NO). HALAAS, Arne [NO/NO]; Overlege Bratts vei 60, N–7026 Trondheim (NO). BIRKELAND, Olaf, René [NO/NO]; Prof. Dahls gate 21B, N–0353 Oslo (NO).

(74) Agent: LEISTAD, Geirr, I.; Opticom ASA, P.O. Box 1872 Vika, N–0124 Oslo (NO).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
In English translation (filed in Norwegian).
Without international search report and to be republished upon receipt of that report.

(54) Title: A PROCESSING CIRCUIT AND A SEARCH PROCESSOR CIRCUIT

(57) Abstract

A processing circuit P_I for recognition and comparison of complex patterns in high-speed data streams can form a node in a network of circuits of this kind and comprises an interface for inputting of parameters for the circuit, at least one kernel processor P_0 in the form of a comparator unit (COM) for comparing two data words, a logic unit (E) connected with the comparator unit and comprising a multiplexer (MUX1), a first D flip–flop (2), a latency unit (LAT) for delaying a positive binary value with a given number of time units, a second D flip–flop (4), a sequence control unit (SC) which monitors and controls a comparison operation in the comparator unit (COM), and a result selector (RS) which combines two result values from other processing circuits or other result selectors. A search processor circuit (PMC) for performing search and comparison operations on complex patterns comprises a multiprocessor unit P_n with processing circuits P_I in a tree structure and forms a binary or superbinary tree with n+1 levels S and degree $k = 2^m$, m being a positive integer ≥ 1. An underlying level S_{n-q} generally comprises 2^{mq} circuits P_{n-q} provided nested in the $2^{m(q-1)}$ circuits P_{n-q+1} on the level S_{n-q+1}. A 0^{th} level S_0 defined for $q = n$ in the unit P_n comprises $2^{m(n-1)}$ to 2^{mn} kernel processors P_0 which form comparator units (COM) in the circuits P_I. All circuits $P_1, P_2..P_n$ have identical interfaces (I) and a logic unit (E) with a result selector (RS) for collecting the results of a search operation or a comparison operation. Use in search engines for search and retrieval of data stored in data bases.

