

Clock Recovery Circuit

An edge detector (10) detects edges of clock pulses in a digital signal and provides edge detect pulses to a state corrector (20). A
5 state sequencer (15) receives a clock signal and steps through a sequence of states in accordance with the clock signal to generate a recovered clock signal which is substantially synchronised with the clock pulses in the digital signal. The state corrector (20)
10 selectively providing reset states to reset the state sequencer in accordance with various parameters to maintain synchronisation between the clock pulses in the digital signal and the recovered clock signal. The state corrector (20) also inhibits resetting the state sequencer (15) when edge detect pulse produced from instability in the edge detector (10) are received.

15

FIG. 1 accompanies this abstract.