HIGH LIFETIME CONSUMABLE SILICON NITRIDE-SILICON DIOXIDE PLASMA PROCESSING COMPONENTS

BACKGROUND

[0001] Plasma processing apparatuses are used to process substrates by techniques including etching, physical vapor deposition (PVD), chemical vapor deposition (CVD), ion implantation and resist removal. One type of plasma processing apparatus used in plasma processing includes a reaction chamber containing upper and bottom electrodes. An RF generated plasma between the electrodes produces energetic ions and neutral species that etch the wafer substrate and chamber parts within the reaction chamber.

SUMMARY

[0002] A method of increasing mean time between cleans of a plasma etch chamber and chamber parts lifetimes is provided. Semiconductor substrates are plasma etched one at a time in the chamber while using at least one sintered silicon nitride component exposed to ion bombardment and/or ionized halogen gas. The silicon nitride component consists of between about 80 weight % and about 95 weight % high purity silicon nitride and between about 5 weight % and about 20 weight % sintering aid. The sintering aid consists of high purity silicon dioxide.

[0003] A plasma processing chamber is provided. A substrate holder supports a substrate within an interior of the processing chamber. A sintered silicon nitride component has an exposed surface adjacent the substrate. The component consists of between about 80 weight % and about 95 weight % high purity silicon nitride and between about 5 weight % and about 20 weight % sintering aid. The sintering aid consists of high purity silicon dioxide. A gas supply supplies process gas to the interior of the processing chamber. An energy source supplying energy into the interior of the processing chamber and energizes the process gas into a plasma state for processing the substrate. The component minimizes metallic contamination

on a surface of the substrate to below 100 x 10^{10} atoms/cm^2 during processing by the plasma.

[0004] A method of reducing metallic contamination on a surface of a silicon substrate during plasma processing is provided. A silicon substrate is placed on a substrate support in a reaction chamber of a plasma processing apparatus. The plasma processing apparatus including one or more sintered silicon nitride components. The silicon nitride components consist of between about 80 weight % and about 95 weight % high purity silicon nitride and between about 5 weight % and about 20 weight % sintering aid. The sintering aid consisting of high purity silicon dioxide. A process gas is introduced into the reaction chamber. A plasma is generated from the process gas. The silicon substrate is processed with the plasma.

[0005] A method of manufacturing a plasma etch chamber processing component exposed to ion bombardment and/or plasma erosion in a plasma etch chamber is provided. A powder composition is mixed, consisting of between about 80 weight % and about 95 weight % high purity silicon nitride and between about 5 weight % and about 20 weight % silicon dioxide. A shaped component is formed from the powder composition. The shaped component is densified with a simultaneous application of heat and pressure.

[0006] A plasma processing component is provided. The component comprises a sintered silicon nitride component, wherein the component consists of between about 80 weight % and about 95 weight % high purity silicon nitride and between about 5 weight % and about 20 weight % sintering aid. The sintering aid consists of high purity silicon dioxide.

BRIEF DESCRIPTION OF FIGURES

[0007] FIG. 1 illustrates a portion of an embodiment of a showerhead electrode assembly and a substrate support for a plasma processing apparatus.

[0008] FIGS. 2A-2B illustrate a portion of the substrate support for a plasma processing apparatus surrounding the hot edge ring.

[0009] FIG. 3 illustrates metallic contamination on the surface of silicon wafers after plasma processing in a processing chamber containing silicon nitride components and a magnesium oxide sintering aid.

[0010] FIG. 4 illustrates metallic contamination on the surface of silicon wafers after plasma processing in a processing chamber containing silicon nitride components and a silicon dioxide sintering aid.

[0011] FIGS. 5A and 5B illustrate wear rate of quartz and silicon nitride components containing various amounts of silicon dioxide as a sintering aid.

DETAILED DESCRIPTION

[0012] As integrated circuit devices continue to shrink in both their physical size and their operating voltages, their associated manufacturing yields become more susceptible to particle and metallic impurity contamination. Consequently, fabricating integrated circuit devices having smaller physical sizes requires that the level of particulate and metal contamination be less than previously considered to be acceptable.

[0013] The manufacturing of the integrated circuit devices includes the use of plasma etching chambers, which are capable of etching selected layers defined by a photoresist mask. The processing chambers are configured to receive processing gases (i.e., etch chemistries) while a radio frequency (RF) power is applied to one or more electrodes of the processing chamber. The pressure inside the processing chamber is also controlled for the particular process. Upon applying the desired RF power to the electrode(s), the process gases in the chamber are activated such that a plasma is created. The plasma is thus generated to perform the desired etching of the selected layers of the semiconductor wafer.

[0014] The plasma etch conditions create significant ion bombardment of the surfaces of the processing chamber that are exposed to the plasma. This ion bombardment, combined with plasma chemistries and/or etch byproducts, can produce significant erosion, corrosion and corrosion-erosion of the plasma-exposed surfaces of the processing chamber. As a result, surface materials are removed by physical and/or chemical attack, including

erosion, corrosion and/or corrosion-erosion. This attack causes problems including short part lifetimes, increased parts costs, particulate contamination, on-wafer transition metal contamination and process drift. Parts with relatively short lifetimes are commonly referred to as consumables. If the consumable part's lifetime is short, then the cost of ownership is high. Erosion of consumables and other parts generates particulate contamination in plasma processing chambers.

[0015] In addition, control of particulate contamination on the surfaces of semiconductor wafers during the fabrication of integrated circuits is essential in achieving reliable devices and obtaining a high yield. Processing equipment, such as plasma processing apparatuses, can be a source of particulate contamination. The desired metal contamination levels on wafer surfaces during etching operations in the plasma chamber are being reduced aggressively for new generations of semiconductor technology. On-wafer metal contamination specifications of 5×10^{10} atoms/cm^2 for metals are currently required for state-of the art semiconductor device manufacture in a plasma etch reactor. Examples of metallic contamination include aluminum, barium, calcium, cerium, chromium, copper, gallium, indium, iron, lithium, magnesium, nickel, potassium, sodium, strontium, tin, titanium, vanadium, yttrium, zinc or zirconium.

[0016] FIG. 1 illustrates an exemplary embodiment of a showerhead electrode assembly 10 for a plasma processing apparatus in which semiconductor substrates, e.g., silicon wafers, are processed. The showerhead electrode assembly 10 includes a showerhead electrode including a top electrode 12, a backing member 14 secured to the top electrode 12, and a thermal control plate 16. A substrate support 18 (only a portion of which is shown in FIG. 1) including a bottom electrode and an electrostatic clamping electrode (e.g., electrostatic chuck) is positioned beneath the top electrode 12 in the vacuum processing chamber of the plasma processing apparatus. A substrate 20 subjected to plasma processing is electrostatically clamped on a top support surface 22 of the substrate support 18.

[0017] In the illustrated embodiment, the top electrode 12 of the showerhead electrode includes an inner electrode member 24, and an optional outer electrode member 26. The inner electrode member 24 is preferably a cylindrical plate (e.g., a plate composed of silicon). The inner electrode member 24 can have a diameter smaller than, equal to, or larger than a wafer to be processed, e.g., up to 12 inches (300 mm) if the plate is made of silicon. In a preferred embodiment, the showerhead electrode assembly 10 is large enough for processing large substrates, such as semiconductor wafers having a diameter of 300 mm or larger. For 300 mm wafers, the top electrode 12 is at least 300 mm in diameter. However, the showerhead electrode assembly can be sized to process other wafer sizes or substrates having a non-circular configuration.

[0018] In the illustrated embodiment, the inner electrode member 24 is wider than the substrate 20. For processing 300 mm wafers, the outer electrode member 26 is provided to expand the diameter of the top electrode 12 from about 15 inches to about 17 inches. The outer electrode member 26 can be a continuous member (e.g., a continuous poly-silicon ring), or a segmented member (e.g., including 2-6 separate segments arranged in a ring configuration, such as segments composed of silicon). In embodiments of the top electrode 12 that include a multiple-segment, outer electrode member 26, the segments preferably have edges, which overlap each other to protect an underlying bonding material from exposure to plasma.

[0019] The inner electrode member 24 preferably includes multiple gas passages 28 extending through and in correspondence with multiple gas passages 30 formed in the backing member 14 for injecting process gas into a space in a plasma processing chamber located between the top electrode 12 and the substrate support 18. Backing member 14 includes multiple plenums 32 to distribute process gases to the gas passages 28 and 30 in the inner electrode member 24 and backing member 14, respectively.

[0020] Silicon is a preferred material for plasma exposed surfaces of the inner electrode member 24 and the outer electrode member 26. High-purity, single crystal silicon minimizes contamination of substrates during plasma

processing and also wears smoothly during plasma processing, thereby minimizing particles. Alternative materials that can be used for plasma-exposed surfaces of the top electrode 12 include SiC or AlN, for example.

[0021] In the illustrated embodiment, the backing member 14 includes a backing plate 34 and a backing ring 36, extending around the periphery of backing plate 34. In the embodiment, the inner electrode member 24 is co-extensive with the backing plate 34, and the outer electrode member 26 is co-extensive with the surrounding backing ring 36. However, the backing plate 34 can extend beyond the inner electrode member 24 such that a single backing plate can be used to support the inner electrode member 24 and the segmented outer electrode member 26. The inner electrode member 24 and the outer electrode member 26 are preferably attached to the backing member 14 by a bonding material.

[0022] The backing plate 30 and backing ring 36 are preferably made of a material that is chemically compatible with process gases used for processing semiconductor substrates in the plasma processing chamber, and is electrically and thermally conductive. Exemplary suitable materials that can be used to make the backing member 14 include aluminum, aluminum alloys, graphite and SiC.

[0023] The top electrode 12 can be attached to the backing plate 34 and backing ring 36 with a suitable thermally and electrically conductive elastomeric bonding material that accommodates thermal stresses, and transfers heat and electrical energy between the top electrode 12 and the backing plate 34 and backing ring 36. The use of elastomers for bonding together surfaces of an electrode assembly is described, for example, in commonly-owned U.S. Patent No. 6,073,577, which is incorporated herein by reference in its entirety.

[0024] In a capacitively coupled RF plasma reactor for processing large substrates such as 300 mm wafers, a secondary ground may also be used in addition to the ground electrode. For example, substrate support 18 can include a bottom electrode which is supplied RF energy at one or more frequencies, process gas can be supplied to the interior of the chamber

through showerhead electrode 12 which is a grounded upper electrode. A secondary ground, located outwardly of the bottom electrode in substrate support 18 can include an electrically grounded portion which extends generally in a plane containing the substrate 20 to be processed but separated by a hot edge ring 38. Hot edge ring 38 can be of electrically conductive or semiconductive material which becomes heated during plasma generation.

[0025] Additionally, a plasma confinement ring assembly 40 can be provided outwardly of backing plate 34 and backing ring 36. The plasma confinement ring assembly 40 and secondary ground can aid in confining the plasma in the space located between the top electrode 12 and the substrate support 18. A detailed discussion of plasma confinement rings and secondary grounds used in RF capacitively coupled plasma reactors can be found in commonly assigned U.S. Patent Nos. 5,534,751 and 6,744,212, both of which are hereby incorporated by reference. With confined plasma, there is little or no contamination caused by the chamber walls. Thus, confined plasmas provide a level of cleanliness that is not provided by unconfined plasmas. For example, confinement ring assembly 40 can be composed of quartz.

[0026] FIGS. 2A and 2B are an enlarged views of the region A in FIG. 1 surrounding hot edge ring 38. For control of etch rate uniformity on substrate 20 and matching the etch rate at the center of the substrate to the rate at the substrate edge, substrate boundary conditions are preferably designed for assuring continuity across the substrate in regard to the chemical exposure of the substrate edge, process pressure, and RF field strength. In the current designs, a hot edge ring 38 has been implemented to fit around the substrate 20. In order to minimize substrate contamination, the hot edge ring 38 is manufactured from a material compatible to the wafer itself. As an example, hot edge ring materials can include silicon, graphite, silicon carbide or the like.

[0027] Hot edge ring 38 overlies coupling ring 42 which is placed on the outer periphery of substrate support 18. The material for coupling ring 42 is

chosen for tapering the RF field strength at the edge of the substrate 20 to enhance etch rate uniformity. For example, coupling ring 42 can be made of a ceramic (e.g. quartz) or a conductive material.

[0028] Surrounding hot edge ring 38 is hot edge ring cover 44, which is composed of a dielectric material. Hot edge ring cover 44 overlies focus ring 46, which confines plasma in an area above the substrate 20 and can be composed of quartz. Further surrounding hot edge ring cover 44 is ground ring cover 48. Hot edge ring cover 44 protects the ground extension from attack by the plasma. For example, hot edge ring cover 44 and ground ring cover 48 can be composed of quartz. Ground extension 50 can be composed of aluminum.

[0029] As illustrated in FIG. 2B, conductive pin 52 and pin sleeve 54 can be contained within hot edge ring 38 and coupling ring 42. Conductive pin 52 monitors the RF bias voltage in the electrostatic chuck of substrate support 18 during plasma processing, which is used to determine overall characteristics of the plasma. For example, conductive pin 52 can be composed of silicon carbide or any conductive material. Pin sleeve 54 surrounds conductive pin 52 and electrically isolates conductive pin 52. For example, pin sleeve 54 can be composed of quartz.

[0030] Quartz can be used as the material of the interior surfaces of consumable parts. However, quartz has the shortest RF lifetime of the consumable materials present in a plasma chamber. The replacement of consumable materials and associated mean time between cleanings (MTBC) for plasma chambers is application specific. Currently, the MTBC for high aspect ratio contact (HARC) applications using the 2300 EXELAN FLEX® dielectric etch system, manufactured by Lam Research Corporation (Fremont, California) is dictated by the replacement of a quartz components at about 250 RF hours. In view of the foregoing, there is a need for high density plasma processing chambers having consumable parts that are more resistant to erosion and assist in minimizing contamination (e.g., particles and metallic impurities) of the wafer surfaces being processed.

[0031] Silicon nitride has been demonstrated to be material suitable for plasma processing components, such as gas distribution plates, liners, and focus rings for use in plasma processing chambers, as described in commonly-owned U.S. Patent No. 5,993,594.

[0032] Such silicon nitride components can be made in various ways. For instance, the silicon nitride can be hot pressed at temperatures above 1500°C using a powder that contains a high percentage of alpha silicon nitride. During hot pressing at such temperatures, the alpha phase transforms to the beta-modification and transformation and densification is dependent on the pressure, temperature and alpha/beta phase ratio of the starting powders. Sintering aids for silicon nitride can include MgO, Y_2O_3, CeO_2, ZrO_2, Al_2O_3, $Y_3Al_5O_{12}$ (yttrium aluminum garnet or YAG) and possibly other rare-earth oxides. The densification can be carried by sintering processes such as pressureless sintering, hot pressing, hot isostatic pressing (HIP-ing) or gas pressure sintering. Compared to hot isostatically pressed silicon nitride, the gas pressure sintered material may exhibit a coarser structure with high aspect ratio grains whereas the pressed material may have a finer, more equiaxed structure. The gas pressure sintering may be conducted using nitrogen gas pressures up to 2 MPa wherein the nitrogen gas suppresses the thermal decomposition of silicon nitride and allows higher sintering temperatures to be used for densification. Hot pressed silicon nitride can be formed by the application of heat and uniaxial pressure in graphite induction heated dies to temperatures in the range of 1650°C to 1850°C for 1 to 4 hours under an applied pressure of 15 to 30 MPa. Another technique involves firing a shaped component of silicon nitride at 1700°C to 1800°C under a nitrogen atmosphere at 0.1 MPa. Another technique involves adding additives such as MgO or Y_2O_3 to silicon, prior to its shaping and followed by nitridation in a temperature range of between about 1100°C and about 1450°C under a nitrogen atmosphere. Although metallic oxide sintering aids (e.g. MgO) facilitate the formation of dense silicon nitride components, they can potentially introduce

unacceptable levels of metallic contamination on the surface of silicon wafers during plasma processing.

[0033] Silicon nitride components formed by hot pressing, containing about 1 weight % MgO sintering aid, were installed in a 2300 EXELAN FLEX® dielectric etching system to determine surface concentration of various metallic contaminants after plasma processing. This material was fully dense and was produced by blending the high purity Si_3N_4 powders with Mg-containing compounds, followed by hot pressing in graphite dies at temperatures above 1600°C. After hot pressing, components were ground from the hot pressed blanks and cleaned for the etching chamber use.

[0034] Testing in a 2300 EXELAN FLEX® dielectric etching system included subjecting the silicon nitride components with about 1 weight % MgO to a plasma environment for about 50 hours before determining the levels of metallic elements on the surface of a silicon wafer. A blank photoresist coated silicon wafer was exposed to a high aspect ratio contact (HARC) etching recipe for about 5 minutes. For a HARC etching recipe, a gas mixture of about 100 SCCM C_4F_8/about 50 SCCM C_4F_6/about 100 SCCM CH_2F_2/about 50 SCCM O_2/about 1,000 SCCM Ar was delivered to the process chamber with a chamber pressure of about 35 mTorr and about 40 mTorr. Between about 5,000 Watts and about 6,000 Watts of RF power was applied to generate a plasma with the $C_4F_8/C_4F_6/CH_2F_2/O_2$/Ar process gas. After completion, the test wafer was removed and a waferless autoclean (WAC) chamber cleaning recipe was performed for about 30 seconds. For a WAC cleaning recipe, about 300 SCCM N_2 and about 3,000 SCCM O_2 were delivered to the process chamber with a chamber pressure of about 600 mTorr. About 700 Watts of RF power was applied to generate a plasma with the N_2/O_2 process gases to remove polymer deposits from the interior of the processing chamber. This sequence of the HARC etching recipe followed by a WAC recipe was repeated until the silicon nitride components were exposed to plasma environment for about 50 hours. The HARC etching recipe and the WAC chamber cleaning recipe were selected

because quartz is susceptible to erosion under these plasma processing conditions.

[0035] After the silicon nitride component was exposed to about 50 RF hours in a plasma environment, a blank uncoated 300 mm silicon test wafer was subjected to plasma processing using the HARC etching recipe for about 5 minutes. After plasma processing, the surface of the silicon wafer was rinsed with dilute nitric acid (HNO_3) and analyzed by inductively coupled plasma mass spectroscopy (ICP-MS) for surface concentration of various metallic contaminants (atoms/cm^2). FIG. 3 illustrates the surface concentration of various metallic contaminants for a blank 300 mm silicon wafer plasma processed in an etching system containing a plasma exposed silicon nitride-based component with a MgO sintering aid.

[0036] As described above, the contamination levels for metallic elements on the surface of a silicon wafer, with the exception of aluminum, is ideally 5 x 10^{10} atoms/cm^2 or lower. As can be seen in FIG. 3, the surface contamination of magnesium exceeded 100 x 10^{10} atoms/cm^2. Thus, for certain applications, the use of silicon nitride components with 1 weight % MgO sintering aid can produce less than completely satisfactory results, due to higher levels of magnesium and other contamination of the surface of a silicon wafer.

[0037] One approach to reducing the metallic contamination on the surface of a silicon wafer is use a sintering aids free of intentional additions of aluminum, barium, calcium, cerium, chromium, copper, gallium, indium, iron, lithium, magnesium, nickel, potassium, sodium, strontium, tin, titanium, vanadium, yttrium, zinc or zirconium. It has been determined that a high purity silicon nitride based plasma processing components containing high purity silicon dioxide as a sintering aid results in a reduction in contamination levels for metallic elements on the surface of a silicon wafer.

[0038] Silicon nitride components formed by hot isostatic pressing, containing 10 weight % silicon dioxide sintering aid, were installed in an 2300 EXELAN FLEX® dielectric etching system to determine surface concentration of various metallic contaminants after plasma processing. The

process steps for fabricating the silicon nitride component are: (1) blending 90 parts (weight %) of high purity silicon nitride powder with 10 parts (weight %) of high purity silicon dioxide powder in an alcohol solvent; (2) evaporating the alcohol solvent to form a dry powder mixture; (3) loading the powder mixture in a die set and subjecting the mixed power to uniaxial dry pressing or cold isostatic pressing (CIP) between about 100 MPa and about 120 MPa, to form a green body pre-form (i.e., unfired ceramic body); and (4) hot isostatic pressing (HIP-ing) the pre-form at a temperature of between about 1750°C and about 1900°C at an applied pressure between about 175 MPa and about 225 MPa, for between about 60 minutes to about 120 minutes using a glass encapsulation technique.

[0039] In uniaxial dry pressing or cold isostatic pressing, the density of the green body pre-form is no less than 45% of the theoretical density. After hot isostatic pressing, the silicon nitride components were determined to have a density of about 95% or more of the theoretical density, based on optical microstructure, in which the silicon nitride component was free of pores. The silicon nitride components containing the silicon dioxide sintering aid have a total metallic contamination of below 5000 ppm, preferably below 1000 ppm, and most preferably below 100 ppm. The metallic contamination includes barium, calcium, cerium, chromium, copper, gallium, indium, iron, lithium, magnesium, nickel, potassium, sodium, strontium, tin, titanium, vanadium, yttrium, zinc and zirconium.

[0040] As described previously, testing in a 2300 EXELAN FLEX® dielectric etching system included subjecting the silicon nitride components with 10 weight % silicon dioxide sintering aid to a plasma environment for about 50 hours before determining the levels of metallic elements on the surface of a silicon wafer. A blank photoresist coated silicon wafer was exposed to a high aspect ratio contact (HARC) etching recipe for about 5 minutes. After completion, the test wafer was removed and a waferless autoclean (WAC) chamber cleaning recipe was performed for about 30 seconds. This sequence was repeated until the silicon nitride components were exposed to plasma environment for about 50 hours.

[0041] After plasma processing, the surface of the silicon wafer was rinsed with dilute nitric acid (HNO_3) and analyzed by inductively coupled plasma mass spectroscopy (ICP-MS) for surface concentration of various metallic contaminants (atoms/cm^2). As seen in FIG. 4, the surface contamination of magnesium was below 5 x 10^{10} atoms/cm^2. Additionally, although calcium, lithium and sodium exceeded the 5 x 10^{10} atoms/cm^2 contamination level, the level of these metals was below about 22 x 10^{10} atoms/cm^2. In comparing the results of FIG. 3 and FIG. 4, the silicon nitride components containing 10% SiO_2 sintering aid provide for a significant improvement over silicon nitride components containing 1% MgO.

[0042] Silicon nitride components formed by hot isostatic pressing containing a SiO_2 sintering aid also exhibited superior wear resistance properties during exposure to a fluorocarbon/hydrofluorocarbon and oxygen/nitrogen plasma in comparison to their quartz counterparts. Furthermore, it was determined that silicon nitride containing about 10 weight % SiO_2 sintering aid exhibited the lowest wear rate. Silicon nitride-based components (e.g., pin sleeves) containing about 5 weight %, about 10 weight %, about 20 weight % and about 35 weight % SiO_2 sintering aid were formed by glass encapsulated hot isostatic pressing. After diamond grinding, the material to close tolerances and after cleaning, each component was individually placed in a 2300 EXELAN FLEX® dielectric etching system and exposed to alternating HARC etching recipe for about 5 minutes followed by a WAC recipe for about 30 seconds, until the total plasma exposure was about 18 RF hours. During testing, the pin sleeve component was subjected to ion bombardment and/or ionized halogen gas. Wear rate of the pin sleeve was determined by measuring the change in the dimension in the y-direction, as indicated in FIG. 5A. The pin sleeve is replaced when its height has been worn to 50% of the height of a new pin sleeve, as indicated in FIG. 5A. In one embodiment, the height of the pin sleeve can range between about 5 mm to about 15 mm.

[0043] As illustrated in FIG. 5B, silicon nitride pin sleeve components containing between about 5 weight % to about 20 weight % SiO_2 provided

improved wear rate during plasma processing, below about 8 μm/RF hour. Quartz components (i.e., 100% SiO_2) exhibited the highest wear rate at about 13 μm/RF hour. However, silicon nitride components containing about 10 weight % SiO_2 exhibited at least a two-fold decrease in wear rate, at about 6 μm/RF hour. Thus, replacing quartz consumable components with silicon nitride components containing between about 5 weight % and about 20 weight % SiO_2 (e.g., between about 8 weight % and about 12 weight %, between about 9 weight % and about 11 weight %, about 10 weight %) can more than double the lifetime from about 250 RF hours to between about 800 RF hours and about 1,000 RF hours.

[0044] While the foregoing has been described in detail with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications may be made, and equivalents thereof employed, without departing from the scope of the claims.

WHAT IS CLAIMED IS:

1. A method of increasing mean time between cleans of a plasma etch chamber and chamber parts lifetimes, comprising:

plasma etching semiconductor substrates one at a time in the chamber while using at least one sintered silicon nitride component exposed to ion bombardment and/or ionized halogen gas, the silicon nitride component consisting of between about 80 weight % and about 95 weight % high purity silicon nitride and between about 5 weight % and about 20 weight % sintering aid, the sintering aid consisting of high purity silicon dioxide.

2. The method of Claim 1, further comprising replacing a quartz component with the sintered silicon nitride component prior to plasma etching the semiconductor substrates.

3. The method of Claim 1, further comprising replacing a silicon nitride component with the sintered silicon nitride component prior to plasma etching the semiconductor substrates.

4. The method of Claim 1, wherein the component is at least one of a pin sleeve, confinement ring, hot edge ring cover or ground cover ring.

5. The method of Claim 1, wherein the plasma etching comprises etching openings in a dielectric material using fluorocarbon and/or hydrofluorocarbon etching gas.

6. The method of Claim 1, wherein the high purity silicon nitride and the high purity silicon dioxide have a metallic impurity of between 1000 ppm to 5000 ppm, between 100 ppm to 1000 ppm or below 100 ppm, the metallic impurity includes barium, calcium, cerium, chromium, copper, gallium, indium, iron, lithium, magnesium, nickel, potassium, sodium, strontium, tin, titanium, vanadium, yttrium, zinc and zirconium; and the silicon

nitride component has a density of about 95% or more of the theoretical density and/or is free of porosity.

7. The method of Claim 1, wherein the mean time between cleans is between about 800 RF hours and about 1,000 RF hours during etching a dielectric material.

8. The method of Claim 1, further comprising:

removing the semiconductor substrate from the plasma etch chamber; and

plasma cleaning an interior of the plasma etch chamber, wherein the plasma cleaning comprises generating a plasma with oxygen and/or nitrogen gases to remove polymer deposits from the interior of the plasma etch chamber and the plasma cleaning is performed after etching one substrate and before etching of another substrate.

9. A plasma processing chamber comprising:

a substrate holder for supporting a substrate within an interior of the processing chamber;

a sintered silicon nitride component having an exposed surface adjacent the substrate, wherein the component consists of between about 80 weight % and about 95 weight % high purity silicon nitride and between about 5 weight % and about 20 weight % sintering aid, the sintering aid consisting of high purity silicon dioxide;

a gas supply supplying process gas to the interior of the processing chamber; and

an energy source supplying energy into the interior of the processing chamber and energizing the process gas into a plasma state for processing the substrate, wherein the component minimizes metallic contamination on a surface of the substrate to below 100×10^{10} atoms/cm^2 during processing by the plasma.

10. The plasma processing chamber of Claim 9, wherein the component minimizes metallic contamination on the surface of the substrate to below 50 x 10^{10} atoms/cm^2 during processing by the plasma; and the component consists of between about 80 weight % and about 93 weight % high purity silicon nitride and between about 7 weight % and about 20 weight % sintering aid.

11. The plasma processing chamber of Claim 9, wherein the component minimizes metallic contamination on the surface of the substrate to below 10 x 10^{10} atoms/cm^2 during processing by the plasma.

12. The plasma processing chamber of Claim 9, wherein the component minimizes metallic contamination on the surface of the substrate to below 5 x 10^{10} atoms/cm^2 during processing by the plasma.

13. The processing chamber of Claim 9, wherein the metallic contamination includes barium, calcium, cerium, chromium, copper, gallium, indium, iron, lithium, magnesium, nickel, potassium, sodium, strontium, tin, titanium, vanadium, yttrium, zinc and zirconium.

14. The processing chamber of Claim 9, wherein the process gas comprises fluorocarbons and/or hydro fluorocarbons.

15. A method of reducing metallic contamination on a surface of a silicon substrate during plasma processing, the method of comprising:

placing a silicon substrate on a substrate support in a reaction chamber of a plasma processing apparatus, the plasma processing apparatus including one or more sintered silicon nitride components, the silicon nitride components consisting of between about 80 weight % and about 95 weight % high purity silicon nitride and between about 5 weight % and about 20 weight % sintering aid, the sintering aid consisting of high purity silicon dioxide;

introducing a process gas into the reaction chamber;
generating a plasma from the process gas; and
processing the silicon substrate with the plasma.

16. The method of Claim 15, wherein the process gas comprises fluorocarbons and/or hydro fluorocarbons.

17. The method of Claim 15, wherein the one or more silicon nitride components are pin sleeves, confinement rings, hot edge ring covers or ground cover rings.

18. The method of Claim 15, wherein the silicon substrate has a metal surface concentration of less than about 5×10^{10} atoms/cm^2 after processing the silicon substrate with the plasma.

19. The method of Claim 18, wherein the metal includes barium, calcium, cerium, copper, gallium, indium, iron, lithium, magnesium, nickel, potassium, sodium, strontium, tin, titanium, vanadium, yttrium, zinc or zirconium.

20. The method of Claim 15, wherein processing the silicon substrate includes etching.

21. A method of manufacturing a plasma etch chamber processing component exposed to ion bombardment and/or plasma erosion in a plasma etch chamber, comprising:

mixing a powder composition consisting of between about 80 weight % and about 95 weight % high purity silicon nitride and between about 5 weight % and about 20 weight % silicon dioxide;

forming a shaped component from the powder composition; and

densifying the shaped component with a simultaneous application of heat and pressure.

22. The method of Claim 21, wherein mixing the powder composition further comprises:

blending the high purity silicon nitride and the high purity silicon dioxide in an alcohol solvent; and

evaporating the alcohol solvent to form a dry powder mixture;

wherein forming the shaped component further comprises:

loading the dry powder mixture in a die set; and

subjecting the powder mixture to uniaxial pressing or cold isostatic pressing at a pressure of between about 100 MPa and about 120 MPa to form a green body pre-form; and

wherein densifying the shaped component with the simultaneous application of heat and pressure further comprises:

hot isostatic pressing the green body pre-form using glass encapsulation at a temperature of between about 1750°C and about 1900°C, at a pressure between about 175 MPa and about 225 MPa for between about 60 minutes and about 120 minutes.

23. The method of Claim 22, wherein the green body pre-form has a minimum density of 45% of the theoretical density.

24. A plasma processing component comprising:

a sintered silicon nitride component, wherein the component consists of between about 80 weight % and about 95 weight % high purity silicon nitride and between about 5 weight % and about 20 weight % sintering aid, the sintering aid consisting of high purity silicon dioxide.

25. The plasma processing component of Claim 24, wherein the component is a pin sleeve, confinement ring, hot edge ring cover or ground cover ring.