What is claimed is:

1. A semiconductor device, comprising:
a substrate;
a relaxed layer disposed over the substrate and having a semiconductor material comprising SiGe, the relaxed layer comprising:
a base portion disposed over the substrate, and
at least one p-type semiconductor body and at least one n-type semiconductor body extending from the base portion opposite from the substrate, the individual semiconductor bodies having a channel region disposed between a source region and a drain region, the individual semiconductor bodies having a lower portion adjacent the base portion and an upper portion, wherein the base portion has a higher defect concentration as compared to the upper portion;
a strained cladding layer disposed on the channel region of at least one p-type semiconductor body and at least one n-type semiconductor body, wherein the strained cladding layer is disposed on the upper portion of the at least one p-type semiconductor body and at least one n-type semiconductor body without being disposed on the lower portion of the at least one p-type semiconductor body and at least one n-type semiconductor body, and having a material that is different depending on whether the semiconductor body is p-type or n-type;
a gate dielectric layer disposed over the cladding layers;
a gate electrode disposed over the gate dielectric layers; and
source or drain material respectively disposed in each of the source and drain regions.

2. The semiconductor device of claim 1 comprising a relaxed layer disposed over the substrate and having upstanding extensions of relaxed silicon germanium (SiGe) forming both the p-type semiconductor bodies and the n-type semiconductor bodies.

3. The semiconductor device of claim 1 wherein the semiconductor bodies are formed of relaxed SiGe having a larger lattice constant than the lattice constant of the cladding layer on the n-type semiconductor body and having a smaller lattice constant than the lattice constant of the cladding layer on the p-type semiconductor body.

4. The semiconductor device of claim 1 comprising a compression stress at the cladding layer on the p-type semiconductor body, and a tensile stress at the cladding layer on the n-type semiconductor body.

5. The semiconductor device of claim 1 wherein the cladding layer on the p-type semiconductor body is SiGe or Ge, and wherein the cladding layer on the n-type semiconductor body is Si.

6. The semiconductor device of claim 5 wherein the cladding layer on the p-type semiconductor body is SiGe with a greater proportion of Ge than in the SiGe of the semiconductor body.

7. The semiconductor device of claim 1 wherein the source and drain regions comprise at least one of:
the same material as the cladding layer on the same semiconductor body, and
a material that causes strain in the source and drain regions due to proximity with relaxed material of the semiconductor body.

8. The semiconductor device of claim 1 comprising a relaxed layer disposed over the substrate and having upstanding extensions of relaxed silicon germanium (SiGe) forming both the p-type semiconductor bodies and the n-type semiconductor bodies;
wherein the semiconductor bodies are formed of relaxed SiGe having a larger lattice constant than the lattice constant of the cladding layer on the n-type semiconductor body and having a smaller lattice constant than the lattice constant of the cladding layer on the p-type semiconductor body;
the semiconductor device comprising a compression stress at the cladding layer on the p-type semiconductor body, and a tensile stress at the cladding layer on the n-type semiconductor body;
wherein at least one of:
the cladding layer on the p-type semiconductor body is SiGe or Ge, and wherein the cladding layer on the n-type semiconductor body is Si, and
the cladding layer on the p-type semiconductor body is SiGe with a greater proportion of Ge than in the SiGe of the semiconductor body;
wherein the source and drain regions comprise at least one of:
the same material as the cladding layer on the same semiconductor body, and
a material that causes strain in the source and drain regions due to proximity with relaxed material of the semiconductor body;

the semiconductor device comprising an isolation layer in contact with both the p-type semiconductor body and the n-type semiconductor body; and
wherein the semiconductor bodies are fins having sidewalls and a current flow direction extending through the channel region, and wherein the fins have lattices oriented so that the fins have (100) sidewall surfaces and (110) orientation in a channel flow direction and at the cladding layer.

9. A mobile computing platform comprising:
a microprocessor comprising:
a substrate;
a relaxed layer disposed over the substrate and having a semiconductor material comprising SiGe, the relaxed layer comprising:
a base portion disposed over the substrate, and
at least one p-type semiconductor body and at least one n-type semiconductor body extending from the base portion opposite from the substrate, the individual semiconductor bodies having a channel region disposed between a source region and a drain region, the individual semiconductor bodies having a lower portion adjacent the base portion and an upper portion, wherein the base portion has a higher defect concentration as compared to the upper portion;
a strained cladding layer disposed on a channel region of at least one p-type semiconductor body and at least one n-type semiconductor body, wherein the strained cladding layer is disposed on the upper portion of the at least one p-type semiconductor body and at least one n-type semiconductor body without being disposed on the lower portion of the at least one p-type semiconductor body and at least one n-type semiconductor body, and having a material that is different depending on whether the semiconductor body is p-type or n-type;
a gate dielectric disposed layer over the cladding layers;
a gate electrode disposed over the gate dielectric layers; and
source or drain material respectively disposed in each of the source and drain regions;
a display screen communicatively coupled to the microprocessor; and
a wireless transceiver communicatively coupled to the microprocessor.

10. The platform of claim 9 comprising a relaxed layer disposed over the substrate and having upstanding extensions of relaxed silicon germanium (SiGe) forming both the p-type semiconductor bodies and the n-type semiconductor bodies;
wherein the semiconductor bodies are formed of relaxed SiGe having a larger lattice constant

than the lattice constant of the cladding layer on the n-type semiconductor body and having a smaller lattice constant than the lattice constant of the cladding layer on the p-type semiconductor body;

the microprocessor comprising a compression stress at the cladding layer on the p-type semiconductor body, and a tensile stress at the cladding layer on the n-type semiconductor body;

wherein at least one of:

the cladding layer on the p-type semiconductor body is SiGe or Ge, and wherein the cladding layer on the n-type semiconductor body is Si, and

the cladding layer on the p-type semiconductor body is SiGe with a greater proportion of Ge than in the SiGe of the semiconductor body;

wherein the source and drain regions comprise at least one of:

the same material as the cladding layer on the same semiconductor body, and

a material that causes strain in the source and drain regions due to proximity with relaxed material of the semiconductor body;

the microprocessor comprising an isolation layer in contact with both the p-type semiconductor body and the n-type semiconductor body; and

wherein the semiconductor bodies are fins having sidewalls and a channel flow direction extending through the channel region, and wherein the fins have lattices oriented so that the fins have (100) sidewall surfaces and (110) orientation facing the channel flow direction and at the cladding layer.

11. A method of fabricating a semiconductor device, comprising:

forming a relaxed layer disposed over a substrate and having a semiconductor material comprising SiGe, the relaxed layer comprising:

a base portion disposed over the substrate, and

at least one p-type semiconductor body and at least one n-type semiconductor body extending from the base portion opposite from the substrate, wherein the semiconductor bodies have a source region, a channel region, and a drain region, and wherein at least the channel region is formed of a material that comprises SiGe, the individual semiconductor bodies having a lower portion adjacent the base portion and an upper portion, wherein the base portion has a higher defect concentration as compared to the upper portion;

depositing a removable cover layer over at least part of the semiconductor bodies of both a first carrier charge type and a second carrier charge type, wherein the first and second carrier

charge types are different and comprise p-type or n-type;
forming openings through the removable cover layer to expose at least the channel region of the semiconductor bodies of a first carrier charge type
forming a first cladding layer on the exposed semiconductor bodies of the first carrier charge type, wherein the first cladding layer is disposed on the upper portion of the exposed semiconductor bodies of the first carrier charge type without being disposed on the lower portion of the exposed semiconductor bodies of the first carrier charge type,
providing a removable cover layer over at least part of the semiconductor bodies of the first carrier charge type;
forming openings through a removable cover layer to expose at least the channel region of the semiconductor bodies of the second carrier charge type; and
forming a second cladding layer on the exposed semiconductor bodies of the second carrier charge type, wherein the second cladding layer is disposed on the upper portion of the exposed semiconductor bodies of the second carrier charge type without being disposed on the lower portion of the exposed semiconductor bodies of the second carrier charge type.

12. The method of claim 11 comprising forming the second cladding layer of a different material than the material of the first cladding layer, wherein the material is different depending, at least in part, on the type of carrier charge of the semiconductor body in contact with the cladding layer.

13. The method of claim 11 wherein forming the semiconductor bodies comprises:
forming a relaxed layer over the substrate and having upstanding extensions of relaxed silicon germanium (SiGe) forming both the p-type semiconductor bodies and the n-type semiconductor bodies.

14. The method of claim 11 wherein depositing the first cladding layer and the second cladding layer comprises selectively epitaxially growing the first and second cladding layers at the openings.

15. The method of claim 11 wherein forming the semiconductor bodies comprises forming the semiconductor bodies with relaxed SiGe having a larger lattice constant than the lattice constant of the cladding layer on the n-type semiconductor body and having a smaller lattice constant than the lattice constant of the cladding layer on the p-type semiconductor body.

16. The method of claim 11 comprising forming the cladding layer on the p-type semiconductor body of SiGe or Ge, and forming the cladding layer on the n-type semiconductor body of Si.

17. The method of claim 16 comprising forming the cladding layer on the p-type semiconductor body of SiGe with a greater proportion of Ge than in the SiGe of the semiconductor body.

18. The method of claim 11 wherein depositing the removable cover layer comprises depositing a first removable cover layer, the method comprising:
removing the first removable cover layer after the first cladding layer is formed, providing a second removable cover layer to cover the at least part of the semiconductor bodies of the first carrier charge type and the first cladding layer, and
removing the second removable cover layer after the second cladding layer is formed.

19. The method of claim 11 wherein depositing the removable cover layer comprises depositing a first removable cover layer, the method comprising:
providing a second removable cover layer to cover the at least part of the semiconductor bodies of the first carrier charge type and the first cladding layer;
forming an opening through at least the first removable cover layer to expose at least part of the semiconductor bodies of the second carrier charge type; and
removing both the first and second removable cover layers.

20. The method of claim 11 comprising forming the second cladding layer of a different material than the material of the first cladding layer, wherein the material is different depending, at least in part, on the type of carrier charge of the semiconductor body in contact with the cladding layer;
wherein forming the semiconductor bodies comprises:
forming a relaxed layer over the substrate and having upstanding extensions of relaxed silicon germanium (SiGe) forming both the p-type semiconductor bodies and the n-type semiconductor bodies;
wherein forming the first cladding layer and the second cladding layer comprises selectively epitaxially growing the first and second cladding layers at the openings;

wherein forming the semiconductor bodies comprises forming the semiconductor bodies with relaxed SiGe having a larger lattice constant than the lattice constant of the cladding layer on the n-type semiconductor body and having a smaller lattice constant than the lattice constant of the cladding layer on the p-type semiconductor body;

the method comprising forming the cladding layer on the p-type semiconductor body of SiGe or Ge, and forming the cladding layer on the n-type semiconductor body of Si;

the method comprising forming the cladding layer on the p-type semiconductor body of SiGe with a greater proportion of Ge than in the SiGe of the semiconductor body;

wherein depositing the removable cover layer comprises depositing a first removable cover layer, and the method comprising at least one of:

(1) removing the first removable cover layer after the first cladding layer is formed, providing a second removable cover layer to cover the at least part of the semiconductor bodies of the first carrier charge type and the first cladding layer, and

removing the second removable cover layer after the second cladding layer is formed, and

(2) providing a second removable cover layer to cover the at least part of the semiconductor bodies of the first carrier charge type and the first cladding layer;

forming an opening through at least the first removable cover layer to expose at least part of the semiconductor bodies of the second carrier charge type; and

removing both the first and second removable cover layers;

wherein depositing a cladding layer on the p-type semiconductor body forms a compression stress at the cladding layer, and depositing a cladding layer on the n-type semiconductor body forms a tensile stress at the cladding layer on the n-type semiconductor body;

the method comprising forming a source and drain region on either side of the channel region on at least one of the semiconductor bodies, and wherein the source and drain regions comprise at least one of:

the same material as the cladding layer on the same semiconductor body, and

a material that causes strain in the source and drain regions due to proximity with relaxed material of the semiconductor body; and

the method comprising forming an insulation layer in contact with both a p-type semiconductor body and an n-type semiconductor body; and

the method comprising forming the semiconductor bodies as fins having sidewalls and a channel flow direction extending through the channel region, and wherein the fins have lattices oriented so that the fins have (100) sidewall surfaces and (110) orientation facing the channel flow direction and at the cladding layer.