CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of fabricating an integrated circuit structure on a support structure, the method comprising:

forming a plurality of linearly extending lines of at least one material;

cutting said material lines at an angle relative a linearly extending direction to form respective angled end faces at each of the material lines, said respective angled end faces being spaced in the linearly extending direction; and

forming an extension of each of said material lines at each respective angled end face.

2. The method of claim 1, wherein said material lines are parallel material lines.

3. The method of claim 2, wherein said angled end faces are cut using a mask and etching process to form the angled end faces of the parallel material lines simultaneously.

4. The method of claim 2, wherein said angle is between 5 degrees and 30 degrees relative to the linearly extending direction.

5. The method of claim 2, wherein said parallel material lines have a half pitch of 45nm or less.

6. The method of claim 2, wherein said parallel material lines have a half pitch of 20nm or less.

7. The method of claim 2, wherein said parallel material lines are formed using a self-assembled block copolymer mask.

8. The method of claim 2, further comprising covering said parallel material lines with an encapsulation insulating material prior to cutting said parallel material lines.

9. The method of claim 1, wherein said extensions are grown via selective deposition of a pad material at said respective angled end faces.

10. The method of claim 1, further comprising etching a conductive material provided below said parallel material lines and respective extensions using said parallel material lines and respective extensions as an etch mask to form conductive lines having respective electrical contact landing pad areas.

11. The method of claim 10, wherein said at least one material is one of a photoresist, a block copolymer, a silicon, a polysilicon, and a metal.

12. The method of claim 1, wherein said at least one material is a processed block copolymer and further comprising:

etching a mask material provided below said parallel material lines and respective extensions using said parallel material lines and respective extensions as an etch mask to form a mask pattern; and

etching a conductive material provided below said mask pattern using said mask pattern as a second etch mask to form conductive lines having respective electrical contact landing pads.

13. The method of claim 1, wherein said at least one material comprises at least one conductive material and said extension is an electrically conductive contact landing pad.

14. The method of claim 13, wherein said conductive material comprises at least one of a metal, a metal silicide, and a polysilicon.

15. The method of claim 13, wherein a conductive material exposed at said angled end faces is used as a seed to grow said electrically conductive contact landing pads via selective deposition of a conductive material at said angled end.

16. A method of fabricating an integrated circuit structure, the method comprising:

forming a plurality of parallel spaced linearly extending material lines;

etching said material lines at an angle relative to the extending direction of said material lines to form respective angled end faces at each of the parallel material lines, said respective angled end faces being spaced in the linearly extending direction;

forming a contact landing pad mask in contact with each of said angled end faces; and

using said material lines and said contact landing pad masks as an etch mask to etch a conductive material below said

material lines and contact landing pad masks to form a plurality of conductive lines with a half-pitch of 45nm or less having respective conductive contact landing pad areas.

17. The method of claim 16, further comprising covering said material lines with an encapsulation insulating material prior to etching said material lines.

18. The method of claim 16, wherein said angled end faces are cut using a mask and etching process to form the angled end faces of the material lines simultaneously.

19. The method of claim 16, wherein said angle is between 5 degrees and 30 degrees relative to the linearly extending direction.

20. The method of claim 16, wherein said conductive lines have a half pitch of 20nm or less.

21. The method of claim 16, wherein said material lines comprise one of a processed photoresist, a processed block copolymer, a silicon, a polysilicon, and a metal.

22. The method of claim 16, wherein said growth includes using at least a portion of the material line at the angled end face as a seed, and growing said contact landing pad masks from the seed via selective deposition of an extension material.

23. The method of claim 22, wherein said selective deposition is one of chemical vapor deposition, atomic layer deposition, electroless plating, or epitaxial growth.

24. The method of claim 16, wherein said electrical contact landing pad areas are sufficiently large to form an area for electrical

connection to the respective conductive lines, but are spaced apart a sufficient amount to provide electrical isolation among the respective electrical contact landing pads.

25. A method of fabricating an integrated circuit structure, the method comprising:

forming a plurality of parallel spaced linearly extending conductive lines;

etching said conductive lines at an angle relative to the extending direction of said conductive lines to form respective angled end faces at each of said conductive lines, said angled end faces being spaced in the linearly extending direction; and

forming an electrical contact landing pad in contact with each of said respective angled end faces.

26. The method of claim 25, further comprising covering said conductive lines with an encapsulation insulating material prior to cutting said material lines.

27. The method of claim 25, wherein said angled end faces are cut using a mask and etching process to form the angled end faces of the conductive lines simultaneously.

28. The method of claim 25, wherein said angle is between 5 degrees and 30 degrees relative to the linearly extending direction.

29. The method of claim 25, wherein said conductive lines have a half pitch of 20nm or less.

30. The method of claim 25, wherein at least one layer of said conductive lines comprise one of a metal, a metal silicide, and a polysilicon.

31. The method of claim 25, wherein said electrical contact landing pads are formed by using at least a portion of the conductive line at the angled end face as a seed, and growing an electrical contact landing pad from the seed via selective deposition of a conductive material.

32. The method of claim 31, wherein said selective deposition is one of chemical vapor deposition, atomic layer deposition or electroless plating.

33. The method of claim 25, wherein said electrical contact landing pads are sufficiently large to form an area for electrical connection to the respective lines, but are spaced apart a sufficient amount to provide electrical isolation among the respective electrical contact landing pads.

34. An integrated circuit comprising:

a plurality of parallel linearly extending electrically conductive lines formed as part of said integrated circuit, the conductive lines each having an angled end face at a different location along the linearly extending direction of said lines; and

a contact landing pad formed in electrical contact with each angled end face.

35. The integrated circuit of claim 34, wherein said conductive lines have a half-pitch of less than 45nm.

36. The integrated circuit of claim 35, wherein said conductive lines have a half-pitch of less than 20nm.

37. The integrated circuit of claim 34, wherein said angled end faces are at an angle of between 5 degrees and 30 degrees relative to the linearly extending direction.

38. The integrated circuit of claim 34, wherein said conductive lines comprise a poly-silicon material and a metal silicide material.

39. The integrated circuit of claim 34, wherein said conductive lines comprise a metal material.

40. The integrated circuit of claim 34, wherein said conductive lines form at least one of wordlines and bitlines of a memory device.

CLAIMS

What is claimed is:

1. A method of fabricating an integrated circuit structure on a support structure, the method comprising:

forming a plurality of linearly extending lines of at least one material;

cutting said material lines at an angle relative to a linearly extending direction to form respective angled end faces at each of the material lines, said respective angled end faces being spaced in the linearly extending direction, and said respective angled end faces each having a length that is greater than a width of the respective material lines; and

forming an extension of each of said material lines at each respective angled end face.

2. The method of claim 1, wherein said material lines are parallel material lines.

3. The method of claim 1, wherein said extensions are grown via selective deposition of a pad material at said respective angled end faces.

4. The method of claim 1, further comprising etching a conductive material provided below said parallel material lines and respective extensions using said parallel material lines and respective extensions as an etch mask to form conductive lines having respective electrical contact landing pad areas.

5. The method of claim 1, wherein said at least one material is a processed block copolymer and further comprising:

etching a mask material provided below said parallel material lines and respective extensions using said parallel material lines and respective extensions as an etch mask to form a mask pattern; and

etching a conductive material provided below said mask pattern using said mask pattern as a second etch mask to form conductive lines having respective electrical contact landing pads.

6. The method of claim 1, wherein said at least one material comprises at least one conductive material and said extension is an electrically conductive contact landing pad.

7. The method of claim 2, wherein said angled end faces are cut using a mask and etching

process to form the angled end faces of the parallel material lines simultaneously.

8. The method of claim 2, wherein said angle is between 5 degrees and 30 degrees relative to the linearly extending direction.

9. The method of claim 2, wherein said parallel material lines have a half pitch of 45 nm or less.

10. The method of claim 2, wherein said parallel material lines have a half pitch of 20 nm or less.

11. The method of claim 2, further comprising covering said parallel material lines with an encapsulation insulating material prior to cutting said parallel material lines.

12. The method of claim 4, wherein said at least one material is one of a photoresist, a block copolymer, a silicon, a polysilicon, and a metal.

13. The method of claim 6, wherein said conductive material comprises at least one of a metal, a metal silicide, and a polysilicon.

14. The method of claim 6, wherein a conductive material exposed at said angled end faces is used as a seed to grow said electrically conductive contact landing pads via selective deposition of a conductive material at said angled end.

15. A method of fabricating an integrated circuit structure on a support structure, the method comprising:

forming a plurality of linearly extending lines of at least one material;

cutting said material lines at an angle relative to a linearly extending direction to form respective angled end faces at each of the material lines, said respective angled end faces being spaced in the linearly extending direction; and

forming an extension of each of said material lines at each respective angled end face,

wherein said material lines are parallel material lines, and

wherein said parallel material lines are formed using a self-assembled block copolymer mask.

16. A method of fabricating an integrated circuit structure, the method comprising:

forming a plurality of parallel spaced linearly extending material lines;

etching said material lines at an angle relative to the extending direction of said material lines to form respective angled end faces at each of the parallel material lines, said respective angled end faces being spaced in the linearly extending direction, and said respective angled end faces having a length that is greater than a width of the respective material lines;

forming a contact landing pad mask in contact with each of said angled end faces; and

using said material lines and said contact landing pad masks as an etch mask to etch a conductive material below said material lines and contact landing pad masks to form a plurality of conductive lines with a half-pitch of 45 nm or less having respective conductive contact landing pad areas.

17. The method of claim 16, further comprising covering said material lines with an encapsulation insulating material prior to etching said material lines.

18. The method of claim 16, wherein said angled end faces are cut using a mask and etching process to form the angled end faces of the material lines simultaneously.

19. The method of claim 16, wherein said angle is between 5 degrees and 30 degrees relative to the linearly extending direction.

20. The method of claim 16, wherein said conductive lines have a half pitch of 20 nm or less.

21. The method of claim 16, wherein said material lines comprise one of a processed photoresist, a processed block copolymer, a silicon, a polysilicon, and a metal.

22. The method of claim 16, wherein said growth includes using at least a portion of the material line at the angled end face as a seed, and growing said contact landing pad masks from the seed via selective deposition of an extension material.

23. The method of claim 16, wherein said electrical contact landing pad areas are sufficiently large to form an area for electrical connection to the respective conductive lines, but are spaced apart a sufficient amount to provide electrical isolation among the respective electrical contact landing pads.

24. The method of claim 22, wherein said selective deposition is one of chemical vapor deposition, atomic layer deposition, electroless plating, or epitaxial growth.

25. A method of fabricating an integrated circuit structure, the method comprising:

forming a plurality of parallel spaced linearly extending conductive lines;

etching said conductive lines at an angle relative to the extending direction of said conductive lines to form respective angled end faces at each of said conductive lines, said angled end faces being spaced in the linearly extending direction, and said respective angled end faces having a length that is greater than a width of the respective conductive lines; and

forming an electrical contact landing pad in contact with each of said respective angled end faces.

26. The method of claim 25, further comprising covering said conductive lines with an encapsulation insulating material prior to cutting said material lines.

27. The method of claim 25, wherein said angled end faces are cut using a mask and etching process to form the angled end faces of the conductive lines simultaneously.

28. The method of claim 25, wherein said angle is between 5 degrees and 30 degrees relative to the linearly extending direction.

29. The method of claim 25, wherein said conductive lines have a half pitch of 20 nm or less.

30. The method of claim 25, wherein at least one layer of said conductive lines comprise one of a metal, a metal silicide, and a polysilicon.

31. The method of claim 25, wherein said electrical contact landing pads are formed by using at least a portion of the conductive line at the angled end face as a seed, and growing an electrical contact landing pad from the seed via selective deposition of a conductive material.

32. The method of claim 25, wherein said electrical contact landing pads are sufficiently large to form an area for electrical connection to the respective lines, but are spaced apart a sufficient amount to provide electrical isolation among the respective electrical contact landing pads.

33. The method of claim 31, wherein said selective deposition is one of chemical vapor deposition, atomic layer deposition or electroless plating.

34. An integrated circuit comprising:

a plurality of parallel linearly extending electrically conductive lines formed as part of said integrated circuit, the conductive lines each having an angled end face at a different location along the linearly extending direction of said lines, said angled end faces each having a respective length that is greater than a width of the respective conductive lines; and

a contact landing pad formed in electrical contact with each angled end face.

35. The integrated circuit of claim 34, wherein said conductive lines have a half-pitch of less than 45 nm.

36. The integrated circuit of claim 35, wherein said conductive lines have a half-pitch of less than 20 nm.

37. The integrated circuit of claim 34, wherein said angled end faces are at an angle of between 5 degrees and 30 degrees relative to the linearly extending direction.

38. The integrated circuit of claim 34, wherein said conductive lines comprise a poly-silicon material and a metal silicide material.

39. The integrated circuit of claim 34, wherein said conductive lines comprise a metal material.

40. The integrated circuit of claim 34, wherein said conductive lines form at least one of wordlines and bitlines of a memory device.