WHAT IS CLAIMED IS:

1. An electronic device comprising:

a memory module including at least one dynamic random access memory; and

a processor configured to:

access the memory module,

determine a corrected error count associated with an address of a corrected error, in response to the corrected error being detected when data are read from the memory module;

read an error log associated with the corrected error;

determine a risk level of the corrected error based on whether the corrected error is a temporary error in a read retry operation; and

schedule a post package repair (PPR) for the address of the corrected error in response to the risk level being high,

wherein determining the risk level includes:

determining the risk level of the corrected error to be low in response to determining that the corrected error is a temporary error in the read retry operation; and

determining the risk level of the corrected error to be high in response to determining that the corrected error is not a temporary error in the read retry operation.

2. The electronic device of claim 1, wherein the processor is configured to:

determine the risk level of the corrected error to be high, in response to the corrected error count associated with the address of the corrected error exceeding a threshold value.

3. The electronic device of claim 1, wherein the processor is configured to:

request a read operation from the memory module based on the address;

request the read retry operation from the memory module in response to the read operation failing; and

detect the corrected error in response to the read retry operation succeeding.

4. The electronic device of claim 3, wherein the processor is configured to perform the read operation by:

requesting the memory module to perform a read phase of the read operation; and

requesting the memory module to perform a retransmission phase of the read operation in response to an error occurring in the read phase.

5. The electronic device of claim 3 or claim 4, wherein the processor is configured to perform the read retry operation by:

requesting the memory module to perform a first read phase to a fourth read phase until the read retry operation succeeds.

6. The electronic device of claim 5, wherein the processor is configured to:

determine the risk level of the corrected error to be low in response to the first read phase of the read retry operation succeeding; and

determine the risk level of the corrected error to be high in response to the first read phase of the read retry operation not succeeding.

7. The electronic device of claim 3, wherein the processor is configured to perform the read retry operation by:

requesting the memory module to perform a read phase; and

requesting the memory module to again perform the read phase N times in response to an error occurring in the read phase, N being a positive integer.

8. The electronic device of claim 5, wherein the processor is configured to:

determine the risk level of the corrected error to be low in response to an M-th read phase of the read retry operation succeeding or a previous read phase of the M-th read phase succeeding, wherein M is a positive integer smaller than N; and

determine the risk level of the corrected error to be high in response to the M-th read phase of the read retry operation failing and the previous read phase of the M-th read phase failing.

9. The electronic device of any one of claims 1 to 8, wherein the processor is configured to:

collect a list of at least one address of at least one corrected error of which the risk level is determined to be high; and

request the PPR from the memory module based on the list of the at least one address in a next power-on sequence.

10. The electronic device of any one of claims 1 to 8, wherein the processor is configured to:

request the PPR from the memory module based on the address of the corrected error in response to the risk level of the corrected error being determined to be high.

11. The electronic device of claim 10, wherein the processor is configured to:

request, based on the address of the corrected error, the PPR from the memory module within an idle time of the memory module or before accessing the memory module.

12. The electronic device of any one of claims 1 to 8, wherein the processor is configured to:

determine a risk level comparison value of the corrected error in response to the risk level of the corrected error being determined to be high.

13. The electronic device of claim 12, wherein, the processor is configured to:

request the PPR of the corrected error from the memory module in response to the risk level comparison value indicating a first risk condition; and

request the PPR of the corrected error from the memory module after a next power-on in response to the risk level comparison value indicating a second risk condition lower than the first risk condition.

14. The electronic device of claim 12, wherein the PPR includes a software PPR (sPPR) and a hardware PPR (hPPR), and the processor is configured to:

schedule the hardware PPR as the PPR of the corrected error in response to the risk level comparison value indicating a first risk condition; and

request the software PPR as the PPR of the corrected error from the memory module in response to the risk level comparison value indicating a second risk condition lower than the first risk condition.

15. The electronic device of claim 14, wherein the processor is configured to immediately request the software PPR from the memory module and request the hardware PPR from the memory module after a next power-on.

16. An operating method of an electronic device including a processor and a memory module, the method comprising:

performing, at the processor, a read operation on the memory module;

performing, at the processor, a read retry operation on the memory module in response to an error occurring in the read operation;

determining, at the processor, a risk level of a corrected error, based on whether the corrected error is a temporary error in the read retry operation; and

scheduling, at the processor, a post package repair (PPR) of the memory module based on an address of the corrected error, in response to the risk level of the corrected error being high,

wherein determining the risk level includes:

determining the risk level of the corrected error to be low in response to determining that the corrected error is a temporary error in the read retry operation; and

determining the risk level of the corrected error to be high in response to determining that the corrected error is not a temporary error in the read retry operation.

17. The method of claim 16, wherein the scheduling of the PPR includes:

scheduling one of an immediate PPR or a delayed PPR based on a risk level comparison value of the corrected error.

18. The method of claim 16, wherein the scheduling of the PPR includes:

scheduling one of a software PPR or a hardware PPR based on a risk level comparison value of the corrected error.

19. An electronic device comprising:

a basic input output system (BIOS) device including a nonvolatile memory storing a BIOS;

a storage device configured to store an operating system;

a chipset connected with the BIOS device and the storage device;

a memory module including at least one dynamic random access memory; and

a processor connected with the chipset and the memory module,

wherein, in a power-on, the processor is configured to:

load the BIOS from the BIOS device through the chipset; and

load the operating system from the storage device through the chipset, and

wherein, in response to a corrected error occurring when the processor accesses the memory module, the BIOS and/or the processor is configured to:

determine a risk level of the corrected error based on whether the corrected error is a temporary error in a read retry operation; and

register an address of the corrected error at a post package repair (PPR) address list regardless of a corrected error count of the corrected error, in response to the risk level of the corrected error being high,

wherein determining the risk level includes:

determining the risk level of the corrected error to be low in response to determining that the corrected error is a temporary error in the read retry operation; and

determining the risk level of the corrected error to be high in response to determining that the corrected error is not a temporary error in the read retry operation.