structure.) The regions do not negatively impact the bonding of the face sides of the die to the first handle and, advantageously, the regions will be removed with the protective planarized oxide layer associated with each die. This significantly increases yield of the process, wherein Known Good Die may be bonded in the final composite wafer structure.

[008] In one embodiment, the process further includes fabrication of the die device structures on distinct device wafers, protecting each of the die device structures with associated oxide layers, and singulating the die. At least one of the device die may be a compound semiconductor device (e.g., GaAs, InP, GaN, etc.). The first and/or second handles may be bonded to the die by application of a low temperature oxide bonding process, by DBH bonding, or by application of an adhesive between the uniformly thinned die back sides and first and second handle front sides. The first and/or second handles may be remove by thinning, resulting for the second handle in exposure of the device die.

[009] In another embodiment, uniform thinning of the back sides of the die may optionally be preceded by filling in gaps between each of the die bonded to the first handle with a strength enhancing polymeric material prior to thinning to help maintain the relative positioning of the die during, for example, CMP processing. Then, the polymeric fill material may be removed after thinning, either prior to deposit bonding the SiO2 layer or after removing the first handle wafer.

BRIEF DESCRIPTION OF THE FIGURES

[0010] Various aspects of at least one embodiment of the present disclosure are discussed below with reference to the accompanying figures. It will be appreciated that for simplicity and clarity of illustration, elements shown in the drawings have not necessarily been drawn accurately or to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity or several physical components may be included in one illustrated element. Further, where considered appropriate, reference numerals may be repeated among the drawings to indicate corresponding or analogous steps or components. For purposes of clarity, not every component may be labeled in every drawing. The figures are provided for the purposes of illustration and explanation and are not intended as a definition of the limits of the invention. In the figures:

steps generally corresponding to the steps set forth in method 10 of FIG. 1, for ease of discussion.

[0024] As shown in in FIG. 2, one or more die 100a-100c having variable (e.g., greater than 5 μm) thicknesses 102a-102c may have been previously fabricated in a manner known in the art on one or more device wafers and singulated. Representative die 100a includes a face (circuit) side 106a, a substrate material back side 108a, an integrated device structure 110a (e.g., a DBH structure), one or more metallized post structures 112a providing interconnection to the integrated device structure, and a protective planarized oxide layer 114a covering the post structures 112a. Within the planarized oxide layer 114a may be a region 116a of potential singulation and/or handling debris that, but for its subsequent removal by the presently disclose method 10, would otherwise lead to bonding voids and die to die variability in bonding strength due to an inability to properly CMP the composite die structure. A first silicon handle 118 including a front side 120, a back side 122, and an oxide layer 124 at the front side 120 may have also been previously fabricated. The face sides 106a-106c of the die 100a-100c and the front side 120 of the first handle wafer 118 may be prepared and temporarily bonded, such that the respective post structures 112a-112c are aligned in a common plane 126. The die 100a-100c may be precisely aligned in the X-Y plane 126 using a pick and place instrument, and may have been previously tested to be known good die. Final Z-axis alignment of the die back sides 108a-108c will be achieved by grinding and CMP. The die 100a-100c may be bonded to the front side 120 of first handle wafer 118 may be achieved through a low temperature oxide bonding process (e.g., ZiBond® bonding offered by Tessera Technologies of San Jose, California), by application of a temporary adhesive (and appropriate heat and force) between the face sides 106a-106c and first wafer front side 120, allowing tacking thereto, or by similar techniques. The temporary adhesive may comprise sacrificial adhesives, thermoplastic, thermal cure, and UV cure adhesives, and may be applied by spin coating, or other known techniques.

[0025] Temporarily bonding the die 100a-100c to the first handle wafer 118 provides necessary support in order to allow for thinning and processing of the die back sides 108a-108c without breaking, warping or folding of the die. With reference to FIG. 3, optionally a polymeric material 130 may be used to temporarily fill gaps 132 between the die 100a-100c to a level 134 approximately equal to a final desired height of the die 100a-100c, if additional mechanical reinforcement is needed. This step may require annealing (e.g., 150° C) to hold the location of

the material 130. As can be seen in FIG. 4, backgrinding and CMP may be applied to the back sides 108a-108c to thin the die 100a-100c to the final desired height 134. The grinding and thinning removes the substrate material from the back sides 108a-108c of the die 100a-100c until a desired thickness (e.g., 40 μm) is achieved. The die thicknesses are preferably controlled to within 1 μm to enable high yield bonding. If a polymeric fill material 130 has been employed, it may be removed from the wafer assembly (e.g., through heat activation).

[0026] With reference to FIG. 5, the thinned back sides 108-108c of die 100a-100c and exposed surfaces 136 of the front side 120 of the first handle wafer 118 may be prepared with a protective conformal coating 140, such as a silicon dioxide coating layer for a silicon wafer. A second handle wafer 142 may then be temporarily bonded to the prepared, planarized back sides 108a-108c of die 100a-100c. Similar bonding processes as used to bond the first wafer handle 118 to the die 100a-100c may be employed.

[0027] As shown in FIG. 6, an intermediate wafer assembly 144 may be flipped to a preferred orientation to allow processing on the first wafer handle 118. Backgrinding and CMP may then be applied to remove the first handle wafer 118 from the assembly, resulting in exposure of the protective planarized oxide layers 114a-114c covering the post structures 112a-112c. As noted, within the planarized oxide layers 114a-114c may be regions 116a-116c of potential singulation and/or handling debris. With reference to FIG. 7, if necessary another polymeric fill 150 may be applied to the gaps 132 prior to backgrinding and CMP of the protective planarized oxide layers 114a-114c on face sides 106a-106c of the die in order to remove the planarized oxide layers 114a-114c and the regions 116a-116c of potential debris, and to reveal the metalized post structures 112a-112c in common plane 126. If a polymer fill 150 was used, it may be removed, resulting in a final composite wafer structure that is ready for use in subsequent standard wafer to wafer bonding processes.

[0028] The method embodiments described above may employ existing tooling and materials, and provide advantages over currently used bonding methods including, but not limited to, the ability to integrate device dies of dissimilar thicknesses from different technologies, e.g., CMOS, optoelectronics, MEMS, and other microelectronic devices. In addition, the yield of the resulting devices may be increased by incorporating only known-good die into the devices and the elimination of potential die singulation and handling debris, thereby significantly improving yield. Furthermore, the ability to bond thin dies allows for the stacking of multiple device layers,