CLAIMS:

1. A method used in forming a memory array, comprising:

forming a substrate comprising a conductive tier, a first insulator tier above the conductive tier, a sacrificial material tier above the first insulator tier, a second insulator tier above the sacrificial material tier, and a stack comprising vertically alternating insulative tiers and wordline tiers above the second insulator tier;

forming channel material through the insulative tiers and the wordline tiers;

forming horizontally-elongated trenches through the stack to the sacrificial material tier;

etching the sacrificial material through the horizontally-elongated trenches selectively relative to material of the first insulator tier and selectively relative to material of the second insulator tier, and exposing a laterally-outer sidewall of the channel material in the sacrificial material tier; and

forming a conductive structure directly against the laterally-outer sidewall of the channel material in the sacrificial material tier, the conductive structure extending through the first insulator tier and directly electrically coupling the channel material to the conductive tier.

2. The method of claim 1 wherein the material of the first insulator tier and the material of the second insulator tier are of the same composition relative one another.

3. The method of claim 1 wherein the wordline tiers comprise the sacrificial material, and further comprising replacing the sacrificial material of the wordline tiers with conductive wordline material after forming the conductive structure.

4. The method of claim 3 comprising forming a sacrificial sidewall liner in the horizontally-elongated trenches before the etching and removing the sacrificial sidewall liner after the etching.

5. The method of claim 4 wherein the sacrificial sidewall liner is removed after forming the conductive structure.

6. The method of claim 1 comprising forming the channel material into the conductive tier, the channel material having a bottom that is nowhere directly against any conductive material in the conductive tier.

7. The method of claim 1 comprising forming a conductively-doped semiconductive material tier that is vertically between the second insulator tier and a lowest of the insulative tiers, the channel material being formed through the conductively-doped semiconductive material tier, the conductive structure being in the conductively-doped semiconductive material tier laterally between (a) the channel material that is in the conductively-doped semiconductive material tier, and (b) conductively-doped semiconductive material of the conductively-doped semiconductive material tier.

8. The method of claim 7 comprising diffusing conductivity-increasing dopant that is in the conductively-doped semiconductive material laterally through the conductive structure into the channel material and upwardly into the channel material that is above the conductively-doped semiconductive material tier.

9. The method of claim 8 wherein the conductive structure comprises conductively-doped semiconductor material comprising the conductivity-increasing dopant before and after said diffusing.

10. The method of claim 7 comprising forming a sacrificial sidewall liner in the horizontally-elongated trenches before the etching and removing the sacrificial sidewall liner after the etching, the sacrificial line being of the same composition as that of the conductively-doped semiconductive material of the conductively-doped semiconductive material tier.

11. The method of claim 1 wherein the horizontally-elongated trenches have respective bottoms that are above a bottom of the first insulator tier.

12. The method of claim 11 wherein the bottoms of the horizontally-elongated trenches are above a top of the first insulator tier.

13. The method of claim 12 wherein the bottoms of the horizontally-elongated trenches are below a top of the sacrificial material tier.

14. The method of claim 1 wherein the conductive structure comprises an annulus.

15. The method of claim 1 comprising forming CMOS under array circuitry.

16. A method used in forming a memory array, comprising:

forming a substrate comprising a conductive tier, a first insulator tier comprising an insulative metal oxide above the conductive tier, a silicon nitride tier above the first insulator tier, a second insulator tier comprising the insulative metal oxide above the silicon nitride tier, and a stack comprising vertically-alternating insulative tiers and wordline tiers above the second insulator metal oxide tier;

forming channel material through the insulative tiers and the wordline tiers and into the conductive tier;

forming horizontally-elongated trenches through the stack to the silicon nitride tier;

wet etching the silicon nitride tier through the horizontally-elongated trenches selectively relative to the insulative metal oxide of the first insulator tier and the insulative metal oxide of the second insulator tier, and exposing a laterally-outer sidewall of the channel material in the sacrificial material tier; and

forming a conductive structure directly against the laterally-outer sidewall of the channel material in the sacrificial material tier, the conductive structure extending through the first insulator tier and directly electrically coupling the channel material to the conductive tier.

17. The method of claim 16 wherein the insulative metal oxide comprises SiO_2.

18. The method of claim 16 wherein the insulative metal oxide comprises multiple elemental metals.

19. The method of claim 18 wherein one of the elemental metals is Si.

20. The method of claim 16 wherein a least a majority of the insulative metal oxide is stoichiometric.

21. The method of claim 16 wherein a least a majority of the insulative metal oxide is non-stoichiometric.

22. The method of claim 16 comprising forming a conductively-doped semiconductive material tier that is vertically between the second insulator tier and a lowest of the insulative tiers, the channel material being formed through the conductively-doped semiconductive material tier, the conductive structure being in the conductively-doped semiconductive material tier laterally between (a) the channel material that is in the conductively-doped semiconductive material tier, and (b) conductively-doped semiconductive material of the conductively-doped semiconductive material tier.

23. A memory array comprising:

a vertical stack comprising:

a conductive tier;

an insulator tier above the conductive tier;

a conductor tier above the insulator tier; and

vertically-alternating insulative tiers and wordline tiers above the conductor tier, the wordline tiers comprising gate regions of individual memory cells, individual of the gate regions comprising part of a wordline in individual of the wordline tiers;

channel material extending elevationally through the insulative tiers and the wordline tiers;

the individual memory cells comprising a memory structure between the individual gate regions and the channel material; the memory structure comprising a charge-blocking region laterally inward of the individual gate regions, a storage region laterally inward of individual of the charge-blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions; and

a conductive structure that extends through the insulator tier and directly electrically couples the channel material to the conductive tier.

24. The memory array of claim 23 comprising horizontally-elongated insulator structures extending elevationally through the insulative tiers and the wordline tiers, the horizontally-elongated insulator structures laterally separating individual wordlines in individual of the wordline tiers.

25. The memory array of claim 24 wherein the horizontally-elongated insulator structures individually have a bottom that is above a bottom of the insulator tier.

26. The memory array of claim 25 wherein the bottoms of the horizontally-elongated structures are above a top of the insulator tier.

27. The memory array of claim 26 wherein the bottoms of the horizontally-elongated structures are below a top of the conductor tier.

28. The memory array of claim 23 wherein the channel material is in the conductive tier, the channel material having a bottom that is nowhere directly against any conductive material in the conductive tier.

29. The memory array of claim 23 comprising a conductively-doped semiconductive material tier that is vertically between the insulator tier and a lowest of the insulative tiers, the channel material extending through the conductively-doped semiconductive material tier, the conductive structure being in the conductively-doped semiconductive material tier laterally between (a) the channel material that is in the conductively-doped semiconductive material tier in the conductively-doped semiconductive material tier, and (b) conductively-doped semiconductive material of the conductively-doped semiconductive material tier.

30. The memory array of claim 29 wherein the conductive structure and the conductively-doped semiconductive material are of the same composition.

31. The memory array of claim 29 comprising another insulator tier above the conductor tier and below the conductively-doped semiconductive material tier.

32. The memory array of claim 23 comprising NAND.

33. The memory array of claim 23 comprising CMOS under array circuitry.

34. A memory array comprising:

a vertical stack comprising:

a conductive tier;

an insulator tier above the conductive tier;

a conductor tier above the insulator tier; and

vertically alternating insulative tiers and wordline tiers above the conductor tier, the wordline tiers comprising gate regions of individual memory cells, individual of the gate regions comprising part of a wordline in individual of the wordline tiers;

channel material extending elevationally through the insulative tiers and the wordline tiers;

the individual memory cells comprising a memory structure between the individual gate regions and the channel material; the memory structure comprising a charge-blocking region laterally inward the individual gate regions, a storage region laterally inward of individual of the charge-blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions;

a conductive structure directly electrically coupling the channel material to the conductive tier; and

horizontally-elongated insulator structures extending elevationally through the insulative tiers and the wordline tiers, the horizontally-elongated insulator structures laterally separating individual of the wordlines and individually having a bottom that is above a bottom of the insulator tier.

35. The memory array of claim 34 wherein the bottoms of the horizontally-elongated structures are above a top of the insulator tier.

36. The memory array of claim 35 wherein the bottoms of the horizontally-elongated structures are below a top of the conductor tier.

37. A memory array comprising:

a vertical stack comprising:

a conductive tier;

a first insulator tier above the conductive tier;

a conductor tier above the insulator tier;

a second insulator tier above the conductive tier;

a conductively-doped semiconductive material tier above the second insulator tier; and

vertically-alternating insulative tiers and wordline tiers above the conductively-doped semiconductive material tier, the wordline tiers comprising gate regions of individual memory cells, individual of the gate regions comprising part of a wordline in individual of the wordline tiers;

channel material extending elevationally through the insulative tiers and the wordline tiers;

the individual memory cells comprising a memory structure between the individual gate regions and the channel material; the memory structure comprising a charge-blocking region laterally inward of the individual gate regions, a storage region laterally inward of individual of the charge-blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions; and

a conductive structure that extends through the conductively-doped semiconductive material tier, the second insulator tier, the conductor tier, and the first insulator tier; the conductive structure directly electrically coupling the channel material to the conductive tier and comprising a sidewall that is directly against a sidewall of the conductive tier.

38. The memory array of claim 37 wherein material of the first insulator tier and material of the second insulator tier are of the same composition relative one another.

39. The memory array of claim 37 wherein the first insulator tier comprises an insulative metal oxide and the second insulator tier comprises an insulative metal oxide.

40. The memory array of claim 39 wherein the insulative metal oxide of the first insulator tier and the insulative metal oxide of the second insulator tier are of the same composition relative one another.

41. The memory array of claim 40 wherein the insulative metal oxide comprises SiO_2.

42. The memory array of claim 40 wherein the insulative metal oxide comprises multiple elemental metals.

43. The memory array of claim 42 wherein one of the elemental metals is Si.

44. The memory array of claim 40 wherein a least a majority of the insulative metal oxide is stoichiometric.

45. The memory array of claim 40 wherein a least a majority of the insulative metal oxide is non-stoichiometric.

CLAIMS:

1. A method used in forming a memory array, comprising:

forming a substrate comprising a conductive tier, a first insulator tier above the conductive tier, a sacrificial material tier above the first insulator tier, a second insulator tier above the sacrificial material tier, and a stack comprising vertically-alternating insulative tiers and wordline tiers above the second insulator tier;

forming a channel opening elevationally through the stack into the conductive tier and sequentially forming a storage material, a charge-passage material, and a channel material in the channel opening;

forming horizontally-elongated trenches through the stack to the sacrificial material tier;

etching a sacrificial material of the sacrificial material tier through the horizontally-elongated trenches selectively relative to material of the first insulator tier and selectively relative to material of the second insulator tier, and exposing a laterally-outer sidewall of the channel material in the sacrificial material tier by etching portions of the storage material and the charge-passage material that are within the sacrificial material tier through the horizontally-elongated trenches selectively relative to material of the first insulator tier and selectively relative to material of the second insulator tier; and

forming through the horizontally-elongated trenches a conductive material in an air gap resulting from the etchings, thereby forming a conductive structure directly against the laterally-outer sidewall of the channel material in the sacrificial material tier and directly against a sidewall of conducting material of and within the conductive tier, the conductive structure extending through the first insulator tier and directly electrically coupling the channel material to the conductive tier.

2. The method of claim 1 comprising forming the channel material into the conductive tier, the channel material having a bottom that is nowhere directly against any conductive material in the conductive tier.

3. The method of claim 1 comprising forming a conductively-doped semiconductive material tier that is vertically between the second insulator tier and a lowest of the insulative tiers, the channel material being formed through the conductively-doped semiconductive material tier, the conductive structure being in the conductively-doped semiconductive material tier laterally between (a) the channel material that is in the conductively-doped semiconductive material tier, and (b) conductively-doped semiconductive material of the conductively-doped semiconductive material tier.

4. The method of claim 3 comprising diffusing conductivity-increasing dopant that is in the conductively-doped semiconductive material laterally through the conductive structure into the channel material and upwardly into the channel material that is above the conductively-doped semiconductive material tier.

5. The method of claim 4 wherein the conductive structure comprises conductively-doped semiconductor material comprising the conductivity-increasing dopant before and after said diffusing.

6. The method of claim 3 comprising forming a sacrificial sidewall liner in the horizontally-elongated trenches before the etching and removing the sacrificial sidewall liner after the etching, the sacrificial sidewall liner being of the same composition as that of the conductively-doped semiconductive material of the conductively-doped semiconductive material tier.

7. The method of claim 1 wherein the horizontally-elongated trenches have respective bottoms that are above a bottom of the first insulator tier.

8. A method used in forming a memory array, comprising:

forming a substrate comprising a conductive tier, a first insulator tier comprising an insulative metal oxide above the conductive tier, a silicon nitride tier above the first insulator tier, a second insulator tier comprising the insulative metal oxide above the silicon nitride tier, and a stack comprising vertically-alternating insulative tiers and wordline tiers above the second insulator tier;

forming a channel opening elevationally through the stack into the conductive tier and sequentially forming a storage material, a charge-passage material, and a channel material in the channel opening;

forming horizontally-elongated trenches through the stack to the silicon nitride tier;

wet etching silicon nitride of the silicon nitride tier through the horizontally-elongated trenches selectively relative to the insulative metal oxide of the first insulator tier and the insulative metal oxide of the second insulator tier, and exposing a laterally-outer sidewall of the channel material in the silicon nitride tier by etching portions of the storage material and the charge-passage material that are within the silicon nitride tier through the horizontally-elongated trenches; and

forming through the horizontally-elongated trenches a conductive material in an air gap resulting from the etchings, thereby forming a conductive structure directly against the laterally-outer sidewall of the channel material in the silicon nitride tier and directly against a sidewall of conducting material of and within the conductive tier, the conductive structure extending through the first insulator tier and directly electrically coupling the channel material to the conductive tier.

9. A memory array comprising:

a vertical stack comprising:

a conductive tier;

an insulator tier above the conductive tier;

a conductor tier above the insulator tier; and

vertically-alternating insulative tiers and wordline tier above the conductor tier, the wordline tiers comprising gate regions of individual memory cells, individual of the gate regions comprising part of a wordline in individual of the wordline tiers;

channel material extending elevationally through the insulative tiers and the wordline tiers;

the individual memory cells comprising a memory structure between the individual gate regions and the channel material;

the memory structure comprising a charge-blocking region laterally inward of the individual gate regions, a storage region laterally inward of individual of the charge blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions;

horizontally-elongated insulator structures extending elevationally through the insulative tiers and the wordline tiers in horizontally-elongated trenches and into a conductive material of the conductor tier, the horizontally-elongated insulator structures laterally separating individual of the wordlines; and

a conductive structure that extends elevationally through the conductive material of the conductor tier and solid material of the insulator tier and into the conductive tier, is directly against a laterally-outer sidewall of the channel material, is directly against a sidewall of the conductive material of the conductor tier, is directly against a sidewall of conducting material of and within the conductive tier, and directly electrically couples the channel material to the conductive tier.

10. A memory array comprising:

a vertical stack comprising:

a conductive tier;

an insulator tier above the conductive tier;

a conductor tier above the insulator tier; and

vertically-alternating insulative tiers and wordline tiers above the conductor tier, the wordline tiers comprising gate regions of individual memory cells, individual of the gate regions comprising part of a wordline in individual of the wordline tiers;

channel material extending elevationally through the insulative tiers and the wordline tiers;

the individual memory cells comprising a memory structure between the individual gate regions and the channel material;

the memory structure comprising a charge-blocking region laterally inward the individual gate regions, a storage region laterally inward of individual of the charge blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions;

a conductive structure that extends elevationally through a conductive material of the conductor tier and solid material of the insulator tier and into the conductive tier, is directly against a laterally-outer sidewall of the channel material, is directly against a sidewall of the conductive material of the conductor tier, is directly against a sidewall of conducting material of and within the conductive tier, and directly electrically couples the channel material to the conductive tier; and

horizontally-elongated insulator structures extending elevationally through the insulative tiers and the wordline tiers in horizontally-elongated trenches and into the conductive material of the conductor tier, the horizontally-elongated insulator structures laterally separating individual of the wordlines and individually having a bottom that is above a bottom of solid material of the insulator tier.

11. The method of claim 1 wherein the first insulator tier and the second insulator tier are solid.

12. The memory array of claim 10 wherein the bottoms of the horizontally-elongated insulator structures are above a top of the solid material of the insulator tier.

13. A method used in forming a memory array, comprising:

forming a substrate comprising a conductive tier, a first insulator tier above the conductive tier, a sacrificial material tier above the first insulator tier, a second insulator tier above the sacrificial material tier, a conductively-doped semiconductive material tier above the second insulator tier, and a stack comprising vertically-alternating insulative tiers and wordline tiers above the conductively-doped semiconductive material tier;

forming a channel opening elevationally through the stack into the conductive tier and sequentially forming a storage material, a charge-passage material, and a channel material in the channel opening;

forming horizontally-elongated trenches through the stack to the sacrificial material tier;

etching a sacrificial material of the sacrificial material tier through the horizontally-elongated trenches selectively relative to material of the first insulator tier, selectively relative to material of the second insulator tier, and selectively relative to material of the conductively-doped semiconductive material tier, and exposing a laterally-outer sidewall of the channel material in the sacrificial material tier, in the second insulator tier, in the conductively-doped semiconductive material tier, and above the conductively-doped semiconductive material tier by etching portions of the storage material and the charge-passage material that are within the sacrificial material tier through the horizontally-elongated trenches selectively relative to material of the first insulator tier and selectively relative to material of the second insulator tier; and

forming through the horizontally-elongated trenches a conductive material in an air gap resulting from the etchings, thereby forming a conductive structure directly against the laterally-outer sidewall of the channel material in the sacrificial material tier, in the second insulator tier, in the conductively-doped semiconductive material tier, and above the conductively-doped semiconductive material tier, the conductive structure extending through the first insulator tier and directly electrically coupling the channel material to the conductive tier.

14. The method of claim 13 wherein the conductive structure extends under and across the horizontally-elongated trenches, the horizontally-elongated trenches having respective bottoms that are above a bottom of the first insulator tier and that are directly against conductive material of the conductive structure.

15. A memory array comprising:

a vertical stack comprising:

a conductive tier;

a first insulator tier above the conductive tier;

a conductor tier above the first insulator tier;

a second insulator tier above the conductor tier;

a conductively-doped semiconductive material tier above the second insulator tier; and

vertically-alternating insulative tiers and wordline tiers above the conductively-doped semiconductive material tier, the wordline tiers comprising gate regions of individual memory cells, individual of the gate regions comprising part of a wordline in individual of the wordline tiers;

channel material extending elevationally through the insulative tiers and the wordline tiers;

the individual memory cells comprising a memory structure between the individual gate regions and the channel material; the memory structure comprising a charge-blocking region laterally inward of the individual gate regions, a storage region laterally inward of individual of the charge-blocking regions, and insulative charge-passage material laterally inward of individual of the storage regions;

horizontally-elongated insulator structures extending elevationally through the insulative tiers and the wordline tiers in horizontally-elongated trenches and into a conductive material of the conductor tier, the horizontally-elongated insulator structures laterally separating individual of the wordlines; and

a conductive structure that extends elevationally through the conductive material of the conductor tier and solid material of the first and the second insulator tiers and into the conductive tier, the conductive structure being directly against a sidewall of the conductive material of the conductor tier, directly against a laterally-outer sidewall of the channel material in the conductor tier, in the first and the second insulator tiers, in the conductively-doped semiconductive material tier, and above the conductively-doped semiconductive material tier, the conductive structure directly electrically coupling the channel material to the conductive tier.

16. The memory array of claim 15 comprising horizontally-elongated trenches extending through the vertically-alternating insulative tiers, the wordline tiers, the conductively-doped semiconductive material tier, and the second insulator tier; the conductive material of the conductor tier extending under and across the horizontally-elongated trenches, the horizontally-elongated trenches having respective bottoms that are above a bottom of the first insulator tier and that are directly against the conductive material of the conductor tier.