CLAIMS

1. A semiconductor device, comprising:

an active area, located in a semiconductor substrate, comprising a central area and a peripheral area surrounding the central area;

a first strained layer, formed in the peripheral area in an embedded manner, wherein the first strained layer comprises at least a first sub-portion, a second sub-portion, a third sub-portion, and a fourth sub-portion, wherein the first sub-portion and the third sub-portion are separately arranged on two sides of the central area in a first direction, and the second sub-portion and the fourth sub-portion are separately arranged on other two sides of the central area in a second direction, wherein the first direction is different from the second direction;

a gate, located on the active area, extending in the first direction and covering at least a part of the central area, at least a part of the first sub-portion, and at least a part of the third sub-portion;

a first source/drain area and a second source/drain area, wherein the first source/drain area at least partially coincides with the fourth sub-portion, and the second source/drain area at least partially coincides with the second sub-portion;

a first source/drain extension area having a doping depth less than a doping depth of the first source/drain area, wherein the first source/drain extension area is located between a channel below the gate and the first source/drain area, and at least partially coincides with the fourth sub-portion; and

a second source/drain extension area having a doping depth less than a doping depth of the second source/drain area, wherein the second source/drain extension area is located between a channel below the gate and the second source/drain area, and at least partially coincides with the second sub-portion.

2. The semiconductor device according to claim 1, wherein the central area is rectangular, and comprises a first set of parallel side edges parallel to the first direction and a second set of parallel side edges parallel to the second direction.

3. The semiconductor device according to claim 2, wherein the first sub-portion and the third sub-portion are symmetrical along a center line of the first set of parallel side edges, and the

second sub-portion and the fourth sub-portion are symmetrical along a center line of the second set of parallel side edges.

4. The semiconductor device according to claim 1, wherein the first sub-portion, the second sub-portion, the third sub-portion, and the fourth sub-portion of the first strained layer are sequentially connected to form a ring structure surrounding the central area.

5. The semiconductor device according to claim 4, wherein both ends of the first sub-portion are respectively connected and in contact with one end of the second sub-portion and one end of the fourth sub-portion, and both ends of the third sub-portion are respectively connected and in contact with another end of the second sub-portion and another end of the fourth sub-portion.

6. The semiconductor device according to claim 1, wherein the second sub-portion and the fourth sub-portion are symmetrically distributed on both sides of the gate.

7. The semiconductor device according to claim 1, wherein the first strained layer comprises a silicon germanium layer.

8. The semiconductor device according to claim 1, wherein the first strained layer is formed using an epitaxial growth process.

9. The semiconductor device according to claim 1, further comprising a second strained layer located in the central area, wherein a thickness of the first strained layer is greater than a thickness of the second strained layer.

10. The semiconductor device according to claim 9, wherein the thickness of the first strained layer is 5-10 times the thickness of the second strained layer.

11. The semiconductor device according to claim 1, wherein the semiconductor substrate is an n type substrate, and the semiconductor device is a PMOS transistor.

12. The semiconductor device according to claim 1, comprising a shallow trench isolation structure located in the semiconductor substrate to define the active area.

13. A method for manufacturing a semiconductor device, comprising:

providing a semiconductor substrate, and defining an active area in the semiconductor substrate, wherein the active area comprises a central area and a peripheral area surrounding the central area;

forming a first strained layer in the peripheral area in an embedded manner, wherein the first strained layer comprises at least a first sub-portion, a second sub-portion, a third sub-portion, and a fourth sub-portion, wherein the first sub-portion and the third sub-portion are separately arranged on two sides of the central area in a first direction, and the second sub-portion and the fourth sub-portion are separately arranged on other two sides of the central area in a second direction, wherein the first direction is different from the second direction;

forming a gate on the active area, wherein the gate extends in the first direction and covers at least a part of the central area, at least a part of the first sub-portion, and at least a part of the third sub-portion; and

doping the active area on both sides of the gate to form a first source/drain area, a first source/drain extension area, a second source/drain area, and a second source/drain extension area, wherein the first source/drain area and the first source/drain extension area at least partially coincide with the fourth sub-portion, and the second source/drain area and the second source/drain extension area at least partially coincide with the second sub-portion.

14. The method for manufacturing a semiconductor device according to claim 13, wherein the forming a first strained layer in the peripheral area in an embedded manner comprises:

forming a first trench in the peripheral area, and forming the first strained layer in the first trench by an epitaxial growth process.

15. The method for manufacturing a semiconductor device according to claim 13, further comprising: forming a second strained layer in the central area, wherein the forming a second strained layer comprises:

forming a second trench in the central area, and forming the second strained layer in the second trench by an epitaxial growth process.

16. The method for manufacturing a semiconductor device according to claim 13, wherein the defining an active area in the semiconductor substrate comprises:

forming a shallow trench isolation structure in the semiconductor substrate to define the active area.