What is claimed is:

1. A pixel collection circuit, comprising:

a photoelectric detection unit configured to output a first electric signal representing an intensity of a received optical signal in real time;

an optical flow information timing trigger unit, a first input terminal of which is coupled to an output terminal of the photoelectric detection unit, and a second input terminal of which is coupled to an optical flow information resetting line, and which is configured to output an optical flow information timing trigger signal after a resetting signal from the optical flow information resetting line has been canceled and the first electric signal has met a preset trigger condition;

an optical flow information timing control unit, a first input terminal of which is coupled to the optical flow information timing trigger unit, and a second input terminal of which is coupled to the optical flow information resetting line, and which is configured to output a timing start signal after the resetting signal from the optical flow information resetting line has been canceled and the optical flow information timing trigger signal has been received;

an optical flow information timing unit, a first input terminal of which is coupled to the optical flow information timing control unit, and a second input terminal of which is coupled to the optical flow information resetting line, and which is configured to be started and generate a timing signal after the resetting signal from the optical flow information resetting line has been canceled and the timing start signal has been received, the timing signal is used to determine whether the pixel collection circuit has been triggered at the reading time point and how long it has been triggered,

wherein the optical flow information timing unit includes: a fifth switch (K_5), a fifth capacitor (C_5) and a third transistor (T_3) connected in parallel between a fourth switch (K_4) and a terminal at a fixed potential, or a fifth switch (K_5), a fifth capacitor (C_5) and a fourth resistor (R_4) connected in parallel between a fourth switch (K_4) and a terminal at a fixed potential; the fourth switch (K_4), a first terminal of which is

coupled to the fifth switch (K_5), the fifth capacitor (C_5) and the third transistor (T_3)/ the fourth resistor (R_4), and a second terminal of which is coupled to another terminal at a fixed potential, wherein when the resetting signal is valid, the fifth switch (K_5) is turned on; and

a row selection output unit, a first input terminal of which is coupled to the optical flow information timing unit, and a second input terminal of which is coupled to an optical flow output row selection line, and which is configured to receive an optical flow row selection signal from the optical flow output row selection line, and cache and output the timing signal at a current reception time point when the optical flow row selection signal is valid.

2. The pixel collection circuit according to claim 1, further comprising an image information collection unit, a first input terminal of which is coupled to the output terminal of the photoelectric detection unit, a second input terminal of which is coupled to an image information collection line, and which is configured to receive an image information collection signal from the image information collection line, and sample and cache the first electric signal at the current reception time point, wherein a third input terminal of the row selection output unit is coupled to the image information collection unit, and a fourth input terminal of the row selection output unit is coupled to an image output row selection line, so as to receive an image row selection signal from the image output row selection line, and cache and output the first electric signal at the current reception time point when the image row selection signal is valid.

3. The image collection circuit according to claim 2, wherein the image information collection unit is further configured to sample the first electric signal at the current reception time point when the received image information collection signal is valid, and cache the sampled first electric signal when the received image information collection signal is invalid.

4. The pixel collection circuit according to claim 3, wherein the optical flow information timing trigger unit comprises: a filtration and amplification module configured to perform a preprocessing operation on the first electric signal to generate a second electric signal, the preprocessing operation comprises at least one of an amplification operation and a filtration operation; and a threshold comparison module configured to determine whether the second electric signal is greater than a first threshold and/or whether the second electric signal is smaller than a second threshold, and when the second electric signal is greater than the first threshold or smaller than the second threshold, generate the optical flow information timing trigger signal.

5. The pixel collection circuit according to claim 4, wherein the optical flow information timing control unit comprises: a latch configured to be reset when the resetting signal is valid and to be set when the optical flow information timing trigger signal has been received initially; and a pulse shaper configured to generate the timing start signal when the latch has been set.

6. The pixel collection circuit according to claim 5, wherein the photoelectric detection unit comprises: a photodiode (PD_1) whose anode is grounded; and a first transistor (T_1), a source electrode of which is coupled to a cathode of the photodiode (PD_1), and a drain electrode and a gate electrode of which are coupled to a power source (VDD).

7. The pixel collection circuit according to claim 5, wherein the photoelectric detection unit comprises: a photodiode (PD_1) whose anode is grounded; a first transistor (T_1), a source electrode of which is coupled to a cathode of the photodiode (PD_1), and a drain electrode of which is coupled to a power source (VDD); and a first amplifier (A_1) coupled between the cathode of the photodiode (PD_1) and a gate electrode of the first transistor (T_1).

8.An optical flow sensor, comprising:

a pixel collection circuit array comprising a plurality of the pixel collection circuits according to claim 7

an optical flow information reading unit configured to read timing signals outputted by at least a part of the pixel collection circuits in the pixel collection circuit array; and

a global control unit configured to generate a resetting signal, and output the resetting signal to each pixel collection circuit in the pixel collection circuit array through an optical flow information resetting line.

9.The optical flow sensor according to claim 8, further comprising an image information reading unit configured to read first electric signals outputted by at least a part of the pixel collection circuits in the pixel collection circuit array, wherein the global control unit is further configured to generate an image information collection signal, and output the image information collection signal to each pixel collection circuit in the pixel collection circuit array through an image information collection line.

10. An optical flow and image information collection system, comprising: the optical flow sensor according to claim 9; an optical flow preprocessor coupled to the optical flow information reading unit in the optical flow sensor, and configured to acquire a timing signal and generate a time-mapping image of each triggered pixel point; and an image preprocessor coupled to the image information reading unit in the optical flow sensor, and configured to acquire a first electric signal and generate a grayscale image of all pixel points.