

ABSTRACT:

Integrated circuit comprising a noise-reducing output stage.

The invention relates to an integrated circuit, comprising an output stage with at least two respective output transistors, respective main current channels of which are connected in parallel between a first supply terminal and the output. A control circuit ensures that, in response to a variation in an input signal on the input, the

5 charging of respective control electrodes of the at least two respective output transistors commences with a delay relative to one another. The peak value of the time derivative of a current output together by the at least two output transistors is thus limited. After the start of charging, a speed of charging of the control electrode of at least one of the two respective output transistors is reduced. The peak value of the time derivative of

10 the current applied to the output by the at least one of the at least two output transistors is thus reduced.

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