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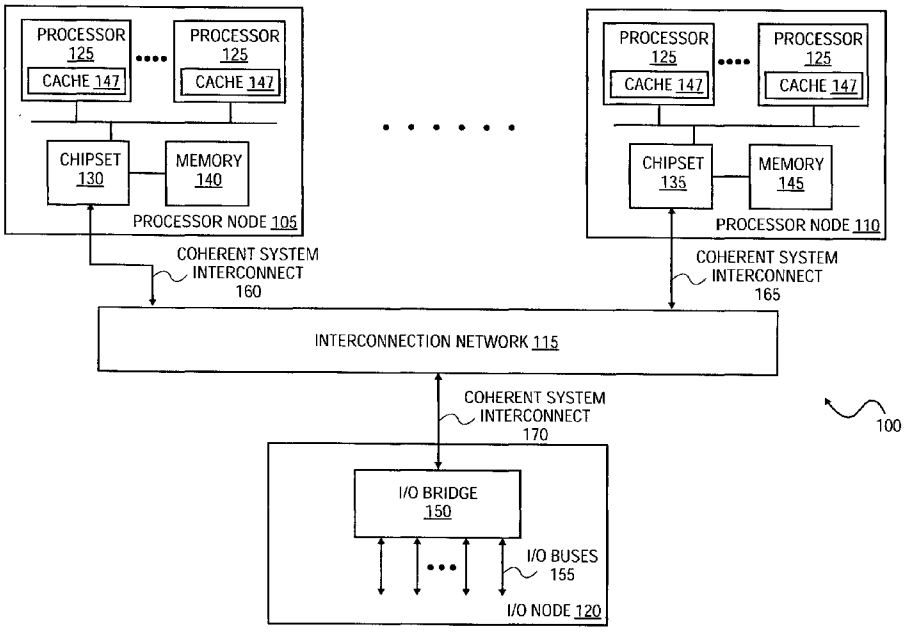
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(54) Title: METHOD AND APPARATUS FOR PIPELINING ORDERED INPUT/OUTPUT TRANSACTIONS IN A CACHE COHERENT, MULTI-PROCESSOR SYSTEM



(57) Abstract: An approach for pipelining ordered input/output transactions to coherent memory in a distributed memory, cache coherent, multi-processor system. A prefetch engine prefetches data from the distributed, coherent memory in response to a transaction from an input/output bus directed to the distributed, coherent memory. An input/output coherent cache buffer receives the prefetched data and is kept coherent with the distributed, coherent memory and with other caching agents in the system.

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