

STRUCTURE AND METHOD OF APPLYING STRESSES TO PFET AND NFET TRANSISTOR CHANNELS FOR IMPROVED PERFORMANCE

ABSTRACT

A semiconductor device structure is provided which includes a first semiconductor device (20); a second semiconductor device (10); and a unitary stressed film (900) disposed over both the first and second semiconductor devices. The stressed film (900) has a first portion (901) overlying the first semiconductor device (20), the first portion imparting a first magnitude compressive stress to a conduction channel of the first semiconductor device, the stressed film (900) further having a second portion (902) overlying the second semiconductor device (10), the second portion (902) not imparting the first magnitude compressive stress to a conduction channel of the second semiconductor device, the second portion including an ion concentration not present in the first portion such that the second portion imparts one of a compressive stress having a magnitude much lower than the first magnitude, zero stress, and a tensile stress to the conduction channel of the second semiconductor device.

Fig 1.



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