

CLAIMS

What is claimed is

1. An apparatus for catalyst influenced chemical etching, comprising:

a process chamber to house a semiconductor wafer; and

one or more actuators configured to control one or more environmental properties at one or more locations on the semiconductor wafer, wherein the one or more environmental properties comprise temperature, vapor pressure, electric field, etchant concentration, etchant composition and illumination,

wherein the catalyst influenced chemical etching is performed on the semiconductor wafer patterned with lithographic structures, wherein a surface of the semiconductor wafer is exposed in areas without the lithographic structures, wherein a catalyst is deposited on the exposed semiconductor wafer surface, wherein the semiconductor wafer and the catalyst are exposed to an etchant in the apparatus, and wherein the catalyst leads to etching solely in regions where the catalyst was deposited on top of the exposed semiconductor wafer surface.

2. The apparatus as recited in claim 1, wherein actuators of the one or more actuators configured to control temperature comprise one or more of the following: thermal chucks, micromirrors and electrodes to locally heat a solution.

3. The apparatus as recited in claim 1, wherein the process chamber comprises an electrode on one or both sides of the semiconductor wafer.

4. The apparatus as recited in claim 3, wherein the electrode is designed to allow transmission of light to one or both sides of the semiconductor wafer.

5. The apparatus as recited in claim 1, wherein a current state of catalyst influenced chemical etching (CICE) is determined *in-situ* using optical metrology on one or more of the front and back of the semiconductor wafer.

6. The apparatus as recited in claim 1, wherein an etchant is in vapor state.

7. The apparatus as recited in claim 1, wherein an etchant is in liquid state.
8. The apparatus as recited in claim 1, wherein a rinsing station is used to remove an etchant.
9. ~~A method for improving reliability of catalyst influenced chemical etching, the method comprising:~~
- ~~patterning a catalyst layer on a surface of a semiconducting material;~~
 - ~~exposing the patterned catalyst layer to one or more of the following: an etchant and a time-varying electric field, wherein the patterned catalyst layer, and one or more of the etchant and the electric field, cause etching of the semiconducting material to form nanostructures; and~~
 - ~~creating one or more layers of porosity as the etch progresses, wherein the porosity is controlled by varying one or more characteristics of the electric field.~~
10. ~~A method for improving reliability of catalyst influenced chemical etching, the method comprising:~~
- ~~providing a semiconducting material;~~
 - ~~patterning a catalyst layer on a surface of the semiconducting material, wherein the pattern comprises one or more lithographic links; and~~
 - ~~exposing the patterned catalyst layer to an etchant such that the one or more lithographic links in the patterned catalyst layer enhance etchant diffusion.~~
11. ~~A method of patterning a catalyst for catalyst influenced chemical etching, the method comprising:~~
- ~~patterning a substrate with lithographic structures, wherein a surface of the substrate is exposed in areas without the lithographic structures;~~
 - ~~selectively depositing a catalyst on the exposed substrate surface, and~~

~~exposing the substrate and the catalyst to an etchant.~~

~~12. The method as recited in claim 11, wherein the lithographic structures are designed such that the catalyst forms a connected mesh.~~

~~13. The method as recited in claim 11, wherein the lithographic structures are designed such that the catalyst comprises isolated dots, wherein a thickness of the catalyst is in a range such that the catalyst dots contain pinholes while also being thick enough to form contiguous regions.~~

~~14. A method of patterning a catalyst for catalyst influenced chemical etching, the method comprising:~~

~~depositing a catalyst on a substrate,~~

~~wherein the catalyst is patterned with lithographic structures, and~~

~~wherein the lithographic structures are used as a mask for etching of the catalyst; and~~

~~exposing the substrate and the catalyst to an etchant.~~

~~15. A method for etching a semiconducting material, the method comprising:~~

~~patterning a catalyst layer on a surface of the semiconducting material, wherein the catalyst layer comprises a plurality of features; and~~

~~exposing the patterned catalyst layer to an etchant, wherein the patterned catalyst layer and the etchant cause etching of the semiconducting material to form nanostructures,~~

~~wherein material of the catalyst layer contains ruthenium.~~

~~16. A method for etching semiconducting material, the method comprising:~~

~~patterning a catalyst layer on a surface of the semiconducting material, wherein the catalyst layer comprises a plurality of features; and~~

~~exposing the patterned catalyst layer to an etchant, wherein the patterned catalyst layer and the etchant cause etching of the semiconducting material to form nanostructures;~~

~~wherein material of the catalyst layer is an alloy of two or more materials.~~

~~17. The method as recited in claim 16, wherein the two or more materials comprise one or more of the following:~~

~~Au, Pt, Pd, Ru, Ag, Co, Cu, Ni, W, TiN, TaN, RuO₂, IrO₂, C, Mo, Cr, semiconductors including III-V, II-VI, Ge, metal and semiconductor oxides, metal and semiconductor nitrides.~~

~~18. A method for etching semiconducting material, the method comprising:~~

~~providing a substrate with at least one layer of the semiconducting material;~~

~~patterning a catalyst layer on a surface of the semiconducting material, wherein the catalyst layer comprises a plurality of features;~~

~~exposing the patterned catalyst layer to an etchant, wherein the patterned catalyst layer and the etchant cause etching of the semiconducting material to form nanostructures; and~~

~~modifying doping of at least one layer of the semiconducting material.~~

~~19. A method for preventing substantial collapse of high aspect ratio semiconducting structures formed by catalyst influenced chemical etching, the method comprising:~~

~~creating a support structure by depositing a material on two or more uncollapsed semiconductor structures; and~~

~~exposing the support structure to an etchant to form higher aspect ratio semiconductor structures with material of the higher aspect ratio semiconductor structures increasing a critical height of features before collapse to prevent substantial collapse of the higher aspect ratio semiconducting structures.~~

~~20. The method as recited in claim 19, wherein the material comprises one or more of the following: a polymer, a semiconductor, a metal and a metal oxide.~~