"Multilayer structure and its fabrication process"

Technical field and prior art

The present invention relates to a process for fabricating multilayer composite structures making it easier to integrate electronic, optoelectronic and/or power components/functionalities.

The production of structures for integrating, on one and the same platform, electronic components of the MOS type (for example CMOS circuits) and electronic, optoelectronic and/or power components of the III-V type (for example transistors or optical sources/detectors) relies on the capability of combining, on the same substrate:

- single-crystal silicon layers of high crystalline quality, allowing the production of MOS electronic components; and
- III-V materials (GaAs, InP and alloys thereof) for the production of III-V electronic, optoelectronic and/or power components.

Many techniques have been experimented by research teams in order to find a satisfactory methodology for fabricating these layers.

The direct epitaxial growth of III-V materials (for example GaAs, InP, alloys, etc.) on silicon by the CVD (Chemical Vapor Deposition) technique or the MBE (Molecular Beam Epitaxy) technique has been studied over recent decades without, however, obtaining good results in terms of crystalline quality (problems of emergent dislocations, antiphase domains, point defects, etc.).

According to another known technique, it is possible to physically transfer thin single-crystal films of InP or GaAs material on to a silicon substrate without

significantly impairing the intrinsic crystalline quality of these films, as for example described in the document by Jalaguier: "*Transfer of 3 in GaAs film on silicon substrate*", Electronics Letters, February 19, 1998, Vol. 34, No. 4, pp. 408-409). This film transfer is carried out using the well-known Smart-Cut™ technology, an implementation example of which is in particular described in the document US 5 374 564 or in the article by A.J. Auberton-Hervé *et al.* entitled "*Why can Smart-Cut change the future of microelectronics?*", International Journal of High-Speed Electronics and Systems, Vol. 10, No. 1, 2000, pp. 131-146.

Furthermore, it has been demonstrated that it is possible to combine the growth techniques with film transfer techniques in order to integrate silicon and III-V materials on the same mechanical platform.

According to a first method of implementation, one way of obtaining GaAs on a 200 mm diameter silicon wafer, without having a GaAs donor substrate, consists in growing GaAs on a single-crystal germanium (Ge) substrate. Growing GaAs on germanium makes it possible to obtain very high-quality thin films owing to the very small lattice parameter mismatch between these two materials. However, because of the cost and mechanical fragility of these bulk substrates, it is more advantageous to transfer a thin germanium film on silicon (such as GaAs and InP) and then carry out crystalline growth of GaAs. The GaAs thus obtained has a quality equivalent to GaAs grown epitaxially on a bulk GaAs substrate.

GeOI structure (germanium on silicon with an intermediate insulating film) has been demonstrated on large diameters, that is to say up to 200 mm in diameter. To date, this is the most direct methodology for combining silicon and GaAs.

However, for the intended application in the present invention, namely the integration of microelectronic, optoelectronic and/or power functions on silicon and III-V materials, this structure is not the best possible. This is because with an epitaxially grown GaAs/Ge transferred structure, it is difficult to produce CMOS components on the silicon support substrate because it is firstly necessary to locally expose the silicon in order to fabricate the circuit thereon. In addition to the problem of specific thermal budget during the fabrication, there is a topology that makes it tricky, or impossible, for the circuit to be electrically connected to the optical component.

According to a second method of implementing this technique, structures with a silicon active layer for the surface CMOS components and an optically active layer beneath the silicon layer have thus been developed for overcoming these drawbacks.

Documents US 6 645 829 and US 6 677 655 thus describe the fabrication of structures that include buried active optical layers, such as:

- [Si substrate/oxide (SiO_2)/Ge layer/Si layer] or else
- [Si substrate/oxide (SiO_2)/Si layer/Ge layer/oxide (SiO_2)/Si layer].

However, in such structures of this type, the optically active layer is always in direct contact with a silicon layer of better or lesser quality depending on the method of fabrication (epitaxy or bonding) used for producing this silicon layer.

Moreover, document US 2004/0252931 proposes forming multilayer structures by bonding a multilayer monolithic electronic device, which includes an electrically active layer and an optically active

layer, on to another layer, the electrical and optical layers possibly being SOI layers transferred on to a support substrate.

Summary of the invention

To avoid the aforementioned drawbacks, the present invention proposes a solution for producing a multilayer structure that homogeneously integrates III-V materials and silicon active layers, while at the same time simplifying the number of steps needed, so as to improve the fabrication yield.

For this purpose, the invention relates to a process for fabricating a multilayer structure, comprising at least the following steps:

a) epitaxial growth of a growth layer on a silicon substrate;

b) formation of at least one pattern in the growth layer;

c) deposition of an oxide layer on the silicon substrate;

d) transfer of a silicon layer onto the oxide layer;

e) formation of a cavity in the silicon layer and in the oxide layer above each pattern; and

f) growth in the cavity of a III-V material from each exposed pattern of the growth layer.

The process of the invention proposes a structure comprising, directly on the surface, both an active silicon layer for MOS components and one or more islands of III-V materials for electronic, optoelectronic and/or power components. This structure is furthermore produced more simply than with the prior processes, in particular owing to the fact that the process of the invention involves only a single layer transfer through the entire fabrication cycle.

According to one aspect of the invention, in step b), each pattern is produced by chemically etching the growth layer through a first aperture mask applied on said growth layer. The number and form of the patterns may vary. In the case of forming a plurality of patterns, these are preferably uniformly spaced apart from each other.

According to another aspect of the invention, in step e), the cavity is produced by chemically etching the silicon active layer and the oxide layer through a second aperture mask applied on said silicon active layer, said mask being aligned with respect to each pattern of the growth layer.

In step d), the silicon active layer may be transferred by bonding an SOI structure onto the oxide layer, the base substrate of the SOI structure being removed after bonding.

The silicon substrate is preferably but not exclusively a misoriented silicon substrate.

The growth layer may be a germanium layer and the III-V material may be a material chosen from at least gallium arsenide (GaAs), AlGaAs and InGaAs.

Moreover, the growth layer may also be an aluminum nitride layer (AlN). In this case, the III-V material may be a material chosen from at least GaN, AlGaN, InGaN and ZnGaN.

The process may furthermore include, after step b) and before step c), at least one heat treatment step so as to allow the dislocations to migrate toward the edges of each pattern and to be annihilated.

The present invention also relates to a multilayer structure comprising:

- a silicon substrate;
- at least one pattern in a growth layer of a III-V material;
- an oxide layer on the silicon substrate; and
- a silicon active layer on the oxide layer,

the oxide layer and the silicon active layer having a cavity above each pattern of the growth layer, said cavity being filled with a III-V material.

Brief description of the figures

The features and advantages of the present invention will become more clearly apparent from the following description, given by way of nonlimiting indication, in conjunction with the appended drawings in which:

- figures 1A to 1K are schematic sectional views showing the fabrication of a multilayer structure according to one method of implementing the invention; and
- figure 2 is a flowchart of the steps implemented in figures 1A to 1K.

Detailed description of embodiments of the invention

The present invention applies in general to the production of multilayer structures, preferably in the form of wafers, allowing easy integration of electronic components (for example FET, MOSFET or HBT transistors), optoelectronic components (for example light sources/detectors) and/or power components (for example an HEMT (high electron mobility transistor)) based on III-V materials on a microelectronic circuit based on silicon technology. This type of circuit may comprise all the components usually encountered in silicon technology, such as those for producing logic and/or analog functions, memory functions, etc.

For this purpose, the multilayer structure of the present invention includes an active silicon surface

layer and one or more islands of III-V material emerging from this silicon layer.

One process for fabricating a multilayer structure according to one embodiment of the invention will now be described with reference to figures 1A to 1K and figure 2.

The first step consists in forming, by epitaxial growth, a germanium layer 2 on a silicon substrate 1 (step S1, figure 1A). The germanium layer 2 corresponds to a growth layer, that is to say a growth nucleation or seed layer, from which a III-V material will subsequently be formed by selective epitaxial regrowth. Epitaxial growth is a well-known technique and will consequently not be described in greater detail.

The germanium layer 2 thus formed has a thickness of between approximately 100 nanometers and 10 microns and has a dislocation density of between approximately $1\times10^{6}/cm^{2}$ and $1\times10^{8}/cm^{2}$.

The silicon substrate 1 may be formed from an oriented silicon substrate (the crystal axis and the (100) surface normal being aligned) or a misoriented silicon substrate (there being an angle, also called "miscut" or "offcut", between the crystal axis and the (100) surface normal). The substrate 1 is preferably, but not necessarily, a misoriented silicon substrate as it allows an epitaxial growth layer to be obtained with very few defects.

The second step consists in forming one or more germanium patterns from the germanium layer 2. In the example described here, a mask 10 is applied on the germanium layer 2, for example by lithography (step S2, figure 1B) and then those parts of the germanium layer 2 that are exposed through the apertures in the mask 10 are chemically etched (step S3, figure 1C). Once the

etching has been completed and the mask removed, a germanium pattern 20 remains on the silicon substrate 1, as shown in figure 1C.

In the example described here, only a single germanium pattern is formed. However, according to the present invention, several patterns may be formed from the growth layer. Likewise, each pattern is not limited to a particular shape. The patterns may be of any type of shape (square, round, annular, etc.), depending on the requirements. The formation of one or more patterns may furthermore be obtained using other etching techniques, such as for example plasma etching or ion etching.

When several patterns are formed, these are preferably uniformly spaced apart on the silicon substrate 1. The silicon substrate 1 with the germanium pattern 20 may furthermore undergo a thermal cycling for removing practically all the dislocations at the pattern 20 by the dislocations migrating toward the edges of the pattern followed by annihilation (step S4). Such thermal cycling is for example described in the document by Luan *et al.*, "High-quality Ge epilayers on Si with low threading-dislocation densities", APL 75 No. 19, November 1999, pp. 2909-2911). This cycling is carried out at temperatures of around 800 to 1000°C for a time ranging from a few tens of minutes to a few hours. Several thermal cycles may sometimes be necessary.

Next, a thick oxide bonding layer 3 is deposited on the silicon substrate 1 and on the germanium pattern 20 (step S5, figure 1D). The oxide bonding layer is for example an SiO_2 layer with a thickness of a few hundred nanometers if the germanium layer 2 is unpatterned (i.e. no patterns formed). Otherwise, the SiO_2 layer has a thickness of about three times the height of the germanium pattern(s) formed. The surface of the oxide

bonding layer 3 is planarized (step S6), for example by CMP (chemical-mechanical polishing).

An SOI structure 4 is then bonded on to the surface of the oxide bonding layer 3 (step S7, figure 1E). The SOI structure 4 comprises, as is well known per se, a silicon substrate 43, a buried oxide (SiO_2) layer 42 and a silicon active layer 41, that is to say a single-crystal silicon layer of high crystalline quality, allowing the production of MOS electronic components. Such an SOI (silicon-on-insulator) structure may be produced, in a known manner, using the Smart Cut™ technology, which comprises the following steps:

- implantation of gaseous species (H, He, etc., separately or in combination) in an oxidized silicon first substrate in order to form a weakened zone in said substrate, defining a donor silicon wafer;
- bonding, for example by molecular adhesion, the first silicon substrate to a second silicon substrate corresponding to the support substrate prepared as described above;
- splitting (thermally and/or mechanically) the donor silicon wafer at the zone weakened by the implantation; and, optionally,
- finishing by chemical etching, polishing/planarization and/or heat treatment.

An SOI structure (identical to structure 4), comprising a silicon support substrate with a buried oxide layer (identical to the silicon substrate 43 with the buried oxide (SiO_2) layer 42) and a silicon film obtained by transferring the donor silicon wafer (corresponding to the silicon active layer 41), is thus obtained.

The SOI structure 4 is bonded to the oxide bonding layer 3 by means of very low-temperature bonding, which can be achieved for example with molecular adhesion bonding via plasma activation (oxygen plasma, nitrogen plasma, etc.). Annealing in a temperature range between

approximately 600°C and 1100°C may be applied so as to reinforce the bonding interface between the oxide bonding layer 3 and the SOI structure 4 (step S8), but also to restore the initial properties of the silicon.

Next, the silicon substrate 43 is removed by wafer grinding, by polishing (CMP) and by chemical etching (step S9, figure 1F). The buried oxide layer is also removed (step S10, figure 1G), for example by dry chemical etching (e.g. plasma etching) or wet chemical etching, or else by selective etching using TMAH (tetramethylammonium hydroxide).

As shown in figure 1G, what is thus obtained is a bilayer structure of the SOI on silicon substrate type containing a germanium pattern 20.

The next two steps consist in forming a cavity for opening the structure above the germanium pattern 20. As during step S3, an aperture mask 11 is applied on the silicon active layer 41 (step S11, figure 1H), for example by lithography, and then those parts of the silicon active layer 41 which are exposed through the aperture of the mask 11 are chemically etched (step S12, figure 1I). The aperture mask 11 must be aligned so as to open the layer 41 above the germanium pattern 20. The mask 11 corresponds to the countertype of the mask 10 used in step S3. Once the etching has been completed and the mask removed, the silicon active layer 41 has a cavity 12 that lies above the germanium pattern 20, as shown in figure 1I. Next, the part of the oxide layer 3 lying between the germanium pattern 20 and the cavity 12 is removed, by dry chemical etching (e.g. plasma etching) or wet etching, so as to extend said cavity down to the pattern 20 (step S13, figure 1J).

Once the germanium pattern has been exposed, a selective epitaxial regrowth of gallium arsenide (GaAs)

is carried out (step S14, figure 1K). This regrowth allows the cavity 12 to be filled with a GaAs island or pattern 5, consisting here of gallium arsenide (GaAs) emerging level with the surface of the silicon active layer 41.

GaAs is not the only III-V material that can be formed on a germanium layer or pattern by epitaxial regrowth. For example, AlGaAs or InGaAs may also be formed from a germanium growth layer.

Moreover, the material of the growth layer is not only limited to germanium. The growth layer may also be an aluminum nitride (AlN) layer formed on a (110) or (100) silicon substrate and from which it is possible to form III-V materials such as GaN and/or AlGaN and/or InGaN and/or ZnGaN.

The fabrication process of the present invention makes it possible for III-V materials and silicon to be homogeneously integrated on one and the same mechanical support, irrespective of the size of the wafers to be produced, such as for example 200 mm or 300 mm diameter wafers.

Many advantageous applications are possible with the multilayer structure of the present invention. In particular, the island(s) of III-V materials formed may be used to produce optoelectronic components of the source or detector type, which can be used as connection means. The electronic chips fabricated from such a structure may then be connected to external devices via optical links (for example connection to optical fibers or waveguides) and benefit from larger bandwidths and datarates than with electrical connections and links.

According to another advantageous application, the structure of the invention may be used for placing,

within a silicon circuit, a set of transistors based on III-V material of greater intrinsic performance (switching speed, through-current, etc.) than MOS transistors.

CLAIMS

1. A process for fabricating a multilayer structure, comprising at least the following steps:

a) epitaxial growth of a growth layer (2) on a silicon substrate (1);

b) formation of at least one pattern (20) in the growth layer (2);

c) deposition of an oxide layer (3) on the silicon substrate (1);

d) transfer of a silicon active layer (41) onto the oxide layer (3);

e) formation of a cavity (12) in the silicon active layer (41) and in the oxide layer (3) above each pattern (20); and

f) growth in the cavity (12) of a III-V material (5) from each exposed pattern (20) of the growth layer (2).

2. The process as claimed in claim 1, wherein, in step b), each pattern (20) is produced by chemically etching the growth layer (2) through an aperture mask (10) applied on said growth layer.

3. The process as claimed in claim 1 or 2, wherein, in step e), the cavity (12) is produced by chemically etching the silicon active layer (41) and the oxide layer (3) through an aperture mask (11) applied on said silicon active layer, said mask being aligned with respect to each pattern (20) of the growth layer (2).

4. The process as claimed in any one of claims 1 to 3, wherein, in step d), the silicon active layer (41) is transferred by bonding an SOI structure (4) onto the oxide layer (3), the base substrate (43) of the SOI structure (4) being removed after bonding.

5. The process as claimed in any one of claims 1 to 4, wherein the silicon substrate (1) is a misoriented silicon substrate.

6. The process as claimed in any one of claims 1 to 5, wherein the growth layer (2) is a germanium layer.

7. The process as claimed in claim 6, which furthermore includes, after step b) and before step c), at least one heat treatment step so as to allow the dislocations to migrate toward the edges of each pattern (20) and to be annihilated thereat.

8. The process as claimed in claim 6 or 7, wherein the III-V material (5) is chosen from at least one of the following materials: gallium arsenide (GaAs), AlGaAs and InGaAs.

9. The process as claimed in any one of claims 1 to 5, wherein the growth layer is an aluminum nitride layer.

10. The process as claimed in claim 9, wherein the III-V material is chosen from at least one of the following materials: GaN, AlGaN, InGaN and ZnGaN.