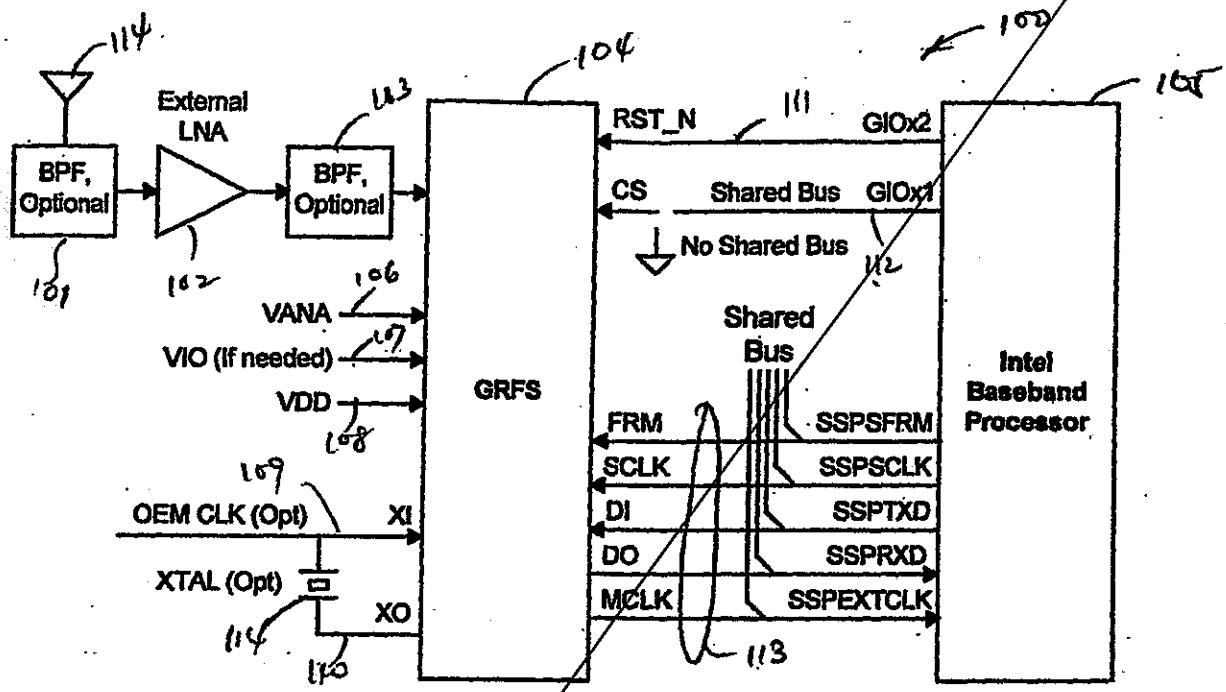


FIGURE 1

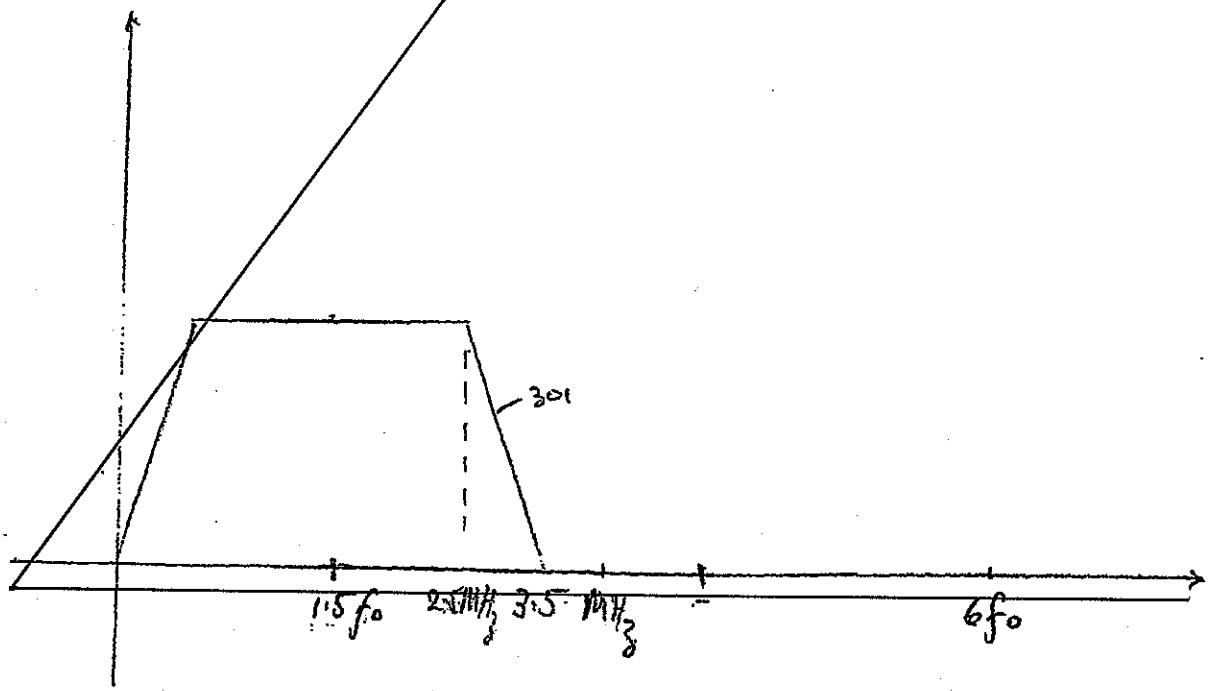


FIGURE 3

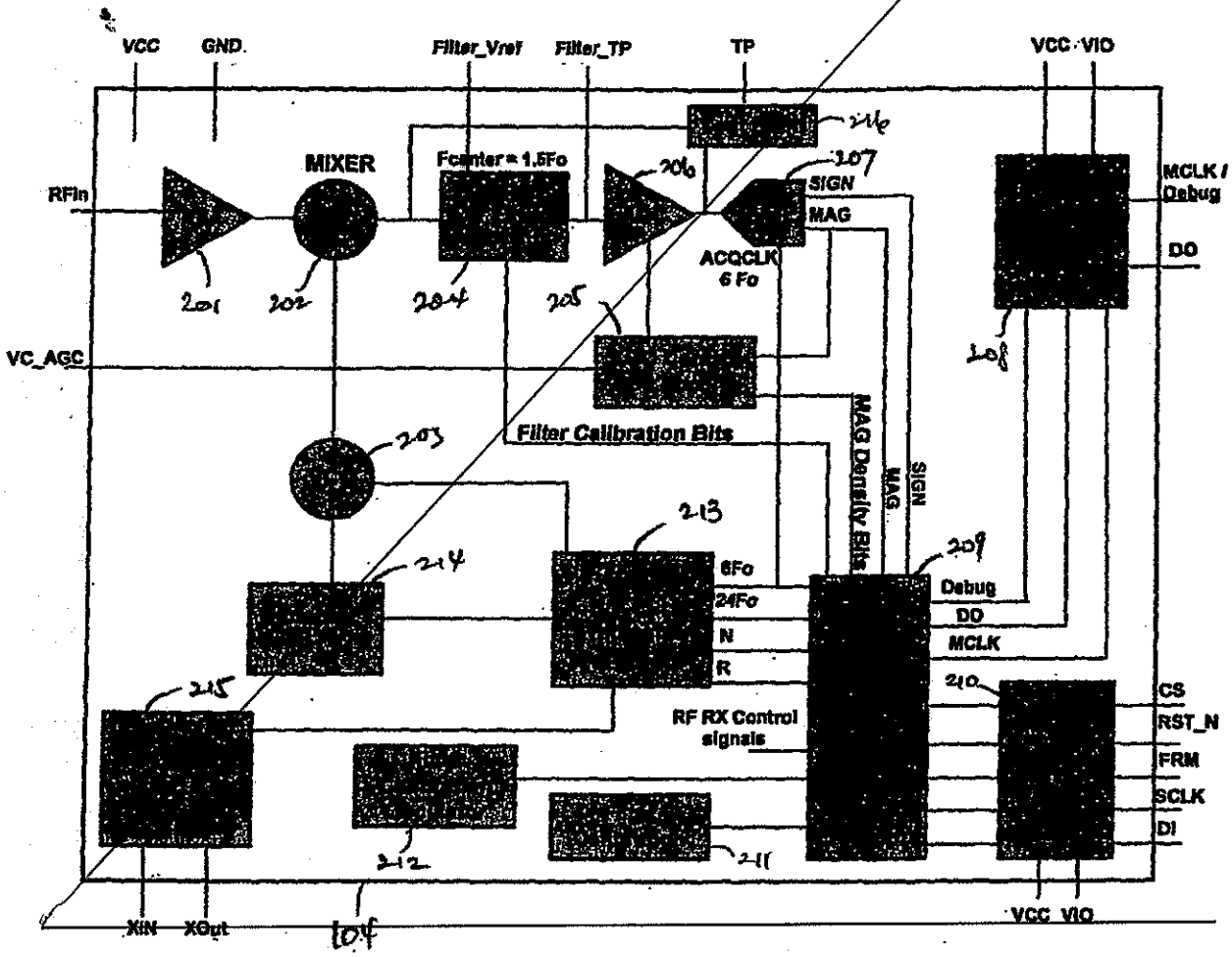

VCC
GND
Filter_Vref
Filter_TP
TP
VCC_VIO
MIXER
Fcenter = 1.5Fo
RFin
SIGN
MAG
ACQCLK
6 Fo
MCLK / Debug
DO
VC_AGC
Filter Calibration Bits
MAG Density Bits
SIGN
MAG
6Fo
24Fo
N
R
Debug
DO
MCLK
RF RX Control signals
CS
RST_N
FRM
SCLK
DI
XIN
XOut
VCC_VIO

FIGURE 2

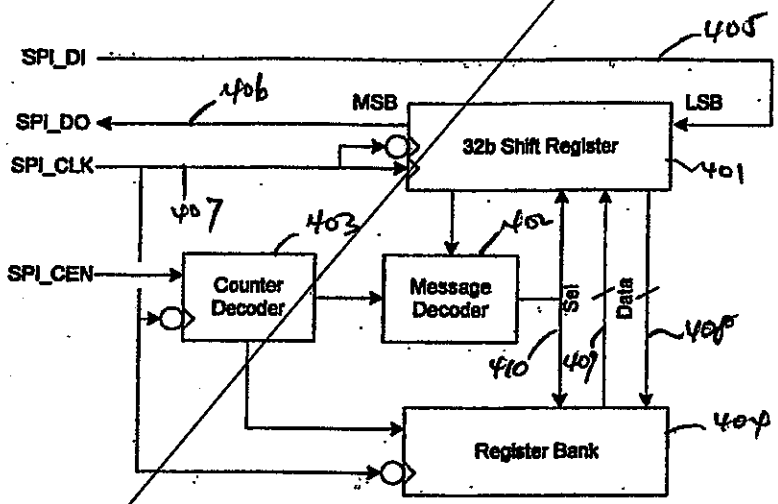

SPI_DI
405
406
SPI_DO
MSB
LSB
32b Shift Register
SPI_CLK
401
407
403
402
SPI_CEN
Counter Decoder
Message Decoder
Sel
Data
408
410
409
Register Bank
404

FIGURE 4

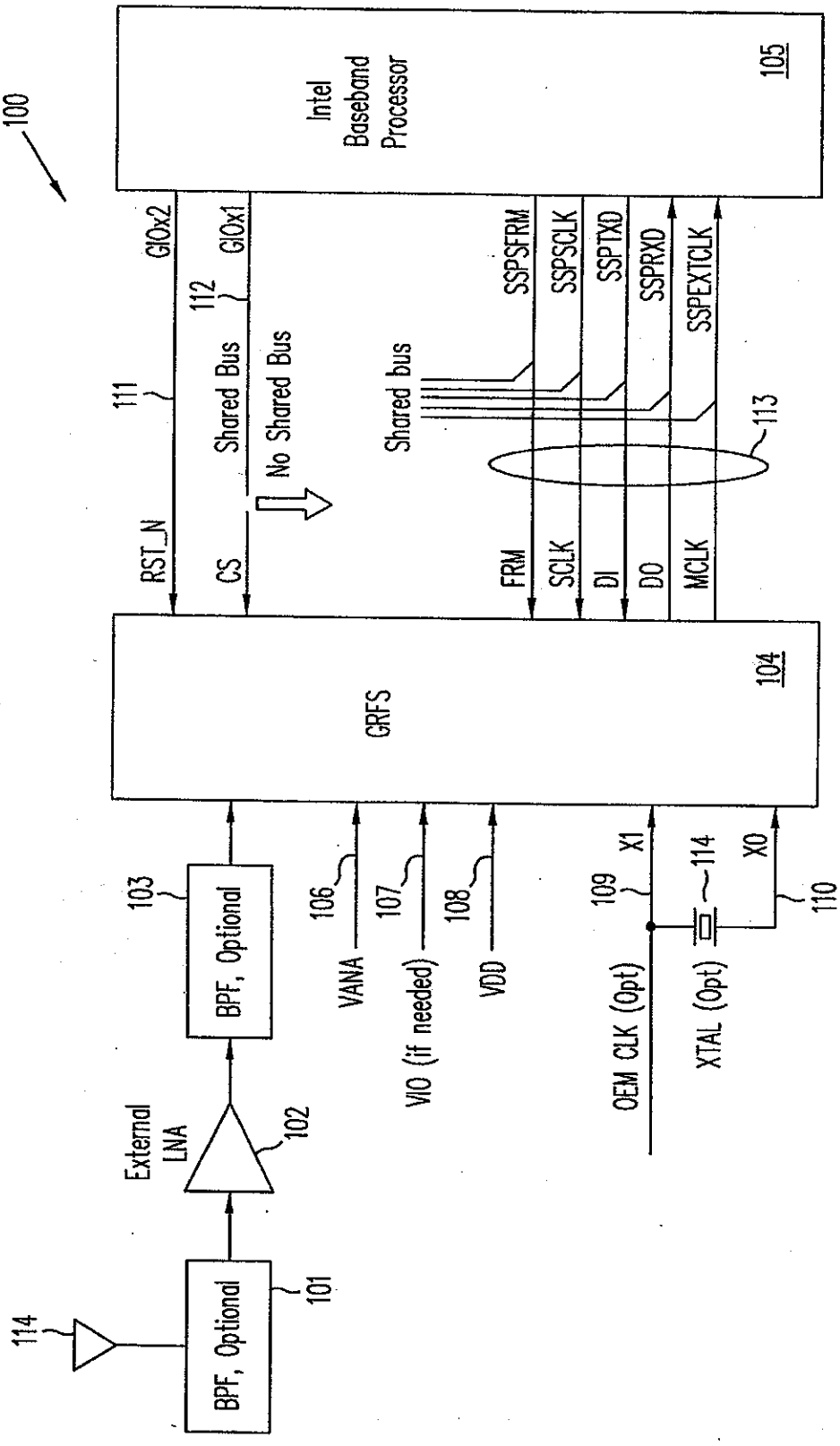

100
Intel Baseband Processor
105
GIOx2
GIOx1
112
111
Shared Bus
No Shared Bus
Shared bus
SSPSFRM
SSPSCLK
SSPTXD
SSPRXD
SSPEXTCLK
113
RST_N
CS
FRM
SCLK
DI
DO
MCLK
GRFS
104
114
BPF, Optional
101
External LNA
102
BPF, Optional
103
106
VANA
107
VIO (if needed)
108
VDD
109
X1
OEM CLK (Opt)
114
XTAL (Opt)
X0
110

FIG. 1

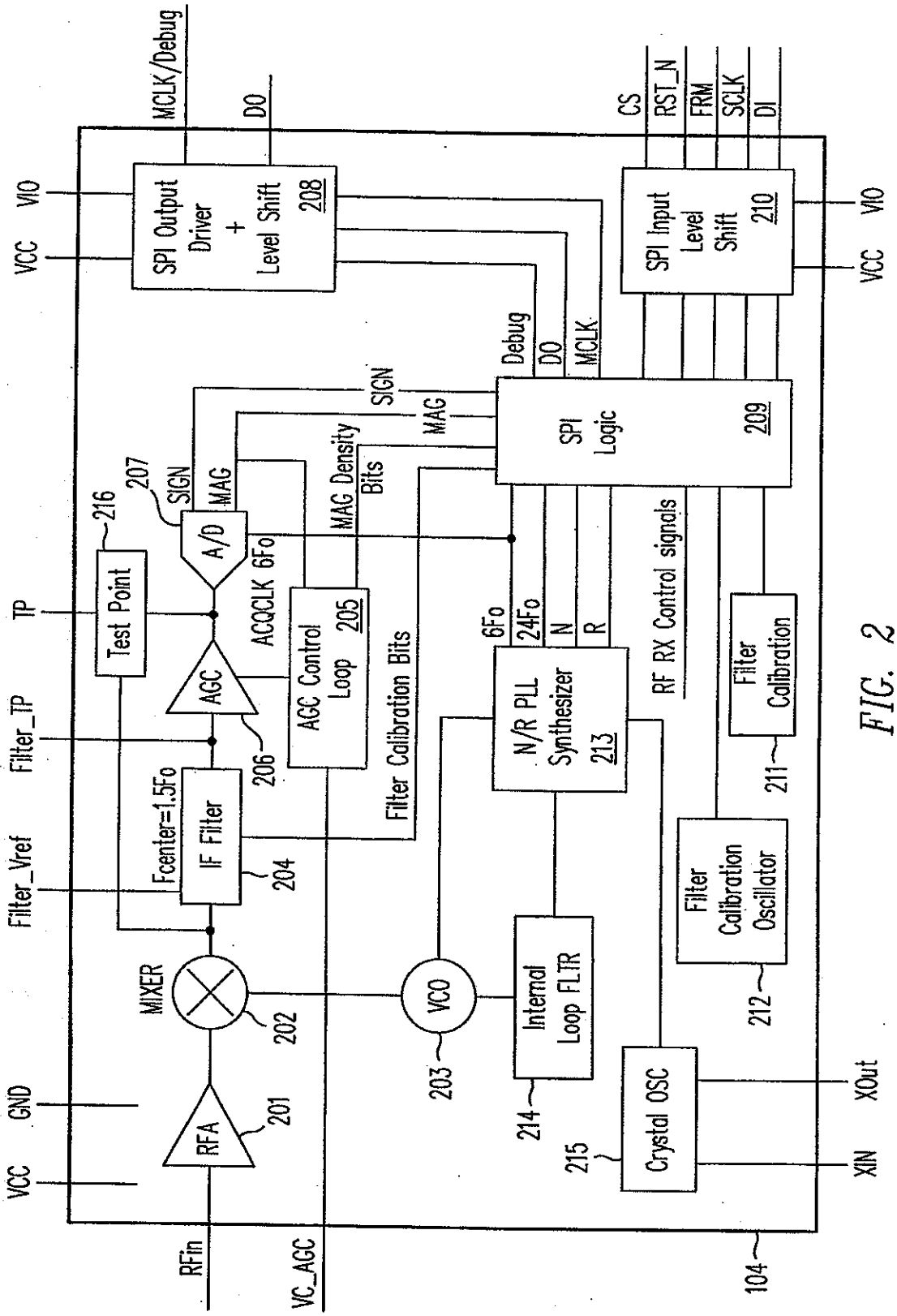

MCLK/Debug
DO
CS
RST_N
FRM
SCLK
DI
VIO
VCC
SPI Output Driver + Level Shift 208
SPI Input Level Shift 210
Debug
DO
MCLK
SIGN
MAG
SPI Logic 209
MAG Density Bits
216
207
SIGN
MAG
A/D
6Fo
ACQCLK
TP
Test Point
AGC
AGC Control Loop 205
206
Filter_TP
Filter Calibration Bits
6Fo
24Fo
N
R
RF RX Control signals
N/R PLL Synthesizer 213
Filter Calibration
211
Filter_Vref
Fcenter=1.5Fo
IF Filter
204
Filter Calibration Oscillator
212
MIXER
202
VCO
203
Internal Loop FLTR
214
GND
VCC
RFA
201
215
Crystal OSC
XOut
XIN
RFin
VC_AGC
104

FIG. 2

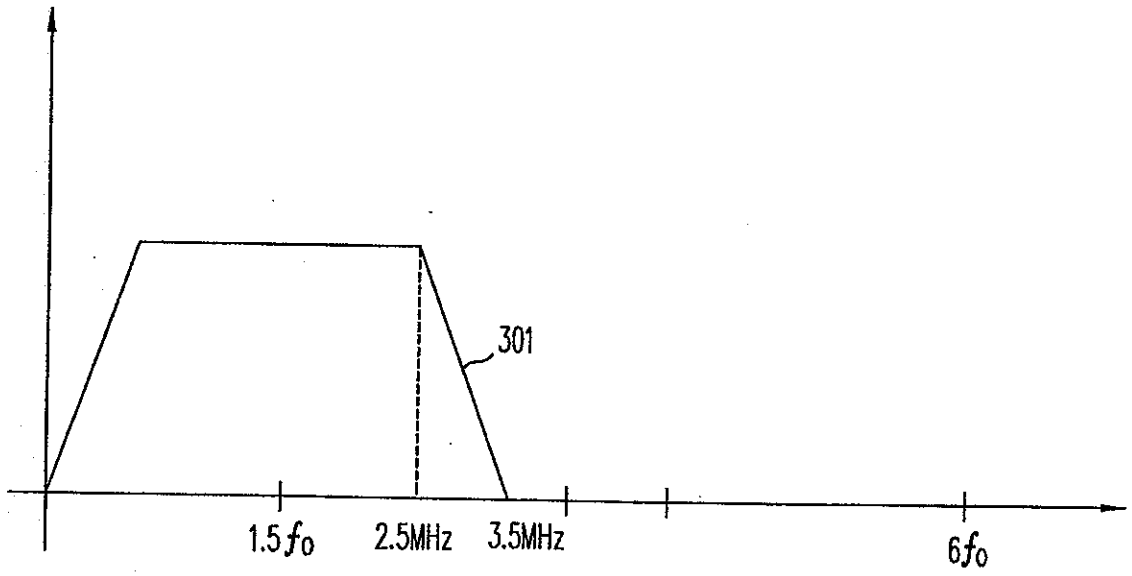

301
1.5f_0
2.5MHz
3.5MHz
6f_0

FIG. 3

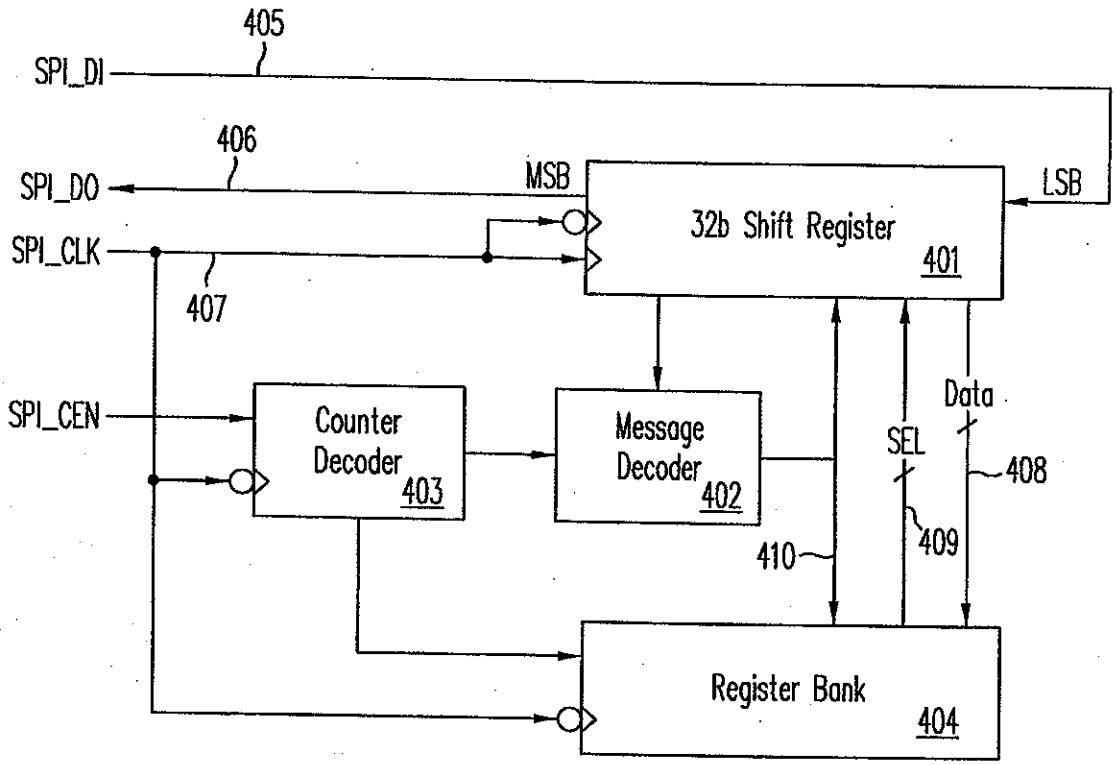

405
SPI_DI
406
SPI_DO
MSB
LSB
32b Shift Register
401
SPI_CLK
407
SPI_CEN
Counter
Decoder
403
Message
Decoder
402
Data
SEL
408
409
410
Register Bank
404

FIG. 4