ABSTRACT

Provided are a timing calibration method and a timing calibration system. The timing calibration method is used for performing timing calibration on test signals in a number of test channels of a digital tester. The method includes: gating any two test channels of the digital tester to output test signals; comparing, by using a window comparator, the test signals output by the two gated test channels, and outputting a comparison result to an FPGA; transmitting, via a clock buffer, the test signal output by one of the two gated test channels to the FPGA, the test signal serving as a sampling clock; the FPGA collecting the comparison result output by the window comparator according to the sampling clock, and sending comparison result to a control terminal; and the control terminal adjusting a clock phase of the test signal in a corresponding test channel according to the comparison result output by the FPGA, to complete timing calibration of the test channel.

[Fig. 2]