Description

The invention relates to a data processing apparatus comprising:

- a data processing element (20, 78) having an operating mode and a stop mode, and comprising a data input, a first data output, a reset signal input, a clock input, a stop signal output and first power supply terminal means for supplying power to the data processing element;
- oscillator means (22, 82) for feeding said clock input with clock pulses, having second power supply terminal means (29) for power reception;
- a data receiving module (24, 70, 72, 74, 76) for receiving external data, said module having a second data output connected to the data input;

wherein said data processing element (20, 78) has reset means for under combined control of a reset signal and a series of clock pulses attaining an initial state within a predetermined time interval.

Reducing energy consumption is of interest in environments of limited available power, e.g. in implanted medical devices, portable equipment or space satellites and in devices in which energy dissipation should be limited, e.g. in VLSI circuits.

A first method for reducing energy consumption in a clocked data processing apparatus, designed in a low-power technology, would be to lower the frequency of the clock as far as possible regarding the required data throughput. Problems then occur, in that DC-current paths, which can be hidden in the design of the data processing element, will be open for a longer period, thereby partially undoing this reduction, and also on that real-time processing may be no longer possible.

A second method for reducing energy consumption would be to use a data processing element, having an operating mode and a mode of reduced activity, and to switch between these modes, keeping the element in the latter mode as long as no operating is required, in which mode the consuming of energy is less than in the former mode. A data processing element having an operating mode and modes of reduced activity is for example the single-chip 8-bit microcontroller PCB80C31, (Philips Data Handbook IC14N, 1984, pp. 187-213). This element has a mode of reduced activity called the idle mode, in which mode the CPU is frozen, while the RAM, timers, etcetera continue functioning, and a mode of further reduced activity, called the stop mode, in which mode the RAM contents are saved but the oscillator is frozen causing all other chip functions to be inoperative. The energy consumed in the stop mode per unit time can be ignored with respect to the energy consumed in the idle mode. The idle mode as well as the stop mode are activated by software.

It is an object of the present invention to reduce the energy consumption by using a data processing element, having an operating mode and a stop mode, in which latter mode all element functions are inoperative but memory contents are saved, and connected to an oscillator, which oscillator is frozen in a stand-by mode while the data processing element is in the stop mode and which oscillator is operative while the data processing element is in the operating mode.

The invention is characterized in that the data processing apparatus further comprises:

- switching means (28, 84), interconnected between said first and second power supply terminal means, and having a first control input for detecting an interrupt signal from said data receiving module for thereupon driving said switching means to transmit operating power to said second supply terminal means and a second control input fed by said stop signal output for upon detection of a stop signal driving said switching means (28, 84) to transmit stand-by power to said second supply terminal means;
- a transition signal detector (30, 86) connected to said switching means (28, 84) for upon detecting any transition from said stand-by power transmitting state to said operating power transmitting state generating said reset signal, that has a trailing edge only after termination of said time interval.

The invention may adjust the oscillator frequency at the most advantageous value, regarding the system's task and limitations.

A direct consequence of freezing the oscillator in applications of a radio with a highly sensitive receiving part (e.g. a MODEM) is to diminish interference.

An eventual consequence of the invention is to realize a real-time processing in an economical way, as the clock frequency needs not be lowered.

BRIEF DESCRIPTION OF THE DRAWINGS.

The invention will be described with reference to some Figures.

Figure 1 shows a first block diagram of a data processing apparatus according to the invention.

Figure 2 represents the behaviour of the apparatus of Figure 1 with time.

Figure 3a, 3b, 3c comprise the formulae according to which the optimal oscillator frequency can be determined.

Equations (1) through (9) determine the optimal oscillator frequency.

Equations (10) and (11) determine a frequency interval in which the oscillator frequency must lie in order to have an energy consumption higher by a fraction δ than the minimum. One can choose δ to be equal to, say, 10%, 50% or another value depending on one's preference.

Equations (12) through (15) determine a frequency interval in which the oscillator frequency must lie in order to keep the energy consumption, when the data processing element is switched between the operating mode and the stop mode, below the minimum of the energy consumption, when switching occurs between the operating mode and the idle mode.

Figure 4 is a typical graph of the average current consumed by the apparatus between two successive interrupts as a function of the frequency, according to the formulae of Figure 3.

Figure 5 pictures a circuit diagram of an oscillator, switching means and second signal detector, used in the preferred embodiment of the invention according to Figure 1.

Figure 6 gives a second block diagram of a data processing apparatus according to the invention.

Figure 7 is a hardware implementation of a preferred exemplary embodiment of the invention according to Figure 6.

DESCRIPTION OF THE PREFERRED EMBODIMENT.

Figure 1 is a first block diagram of a data processing apparatus according to the invention. We assume data processing element 20 to be initially in the stop mode and oscillator 22 is stand-by on a power supply level too low to enable oscillating. In this state energy consumption of the apparatus is negligible. At a certain moment data receiving module 24 receives data from an environment and sends an interrupt pulse to a signal detector 26. Upon receiving this pulse signal detector 26 gives off a signal to switching element 28, which thereupon provides full operating power to oscillator 22 via line 29. Thereupon oscillator 22 starts oscillating while signal detector 30 detects a voltage change on line 29 and for that sends a pulse of predetermined width to the reset signal input of data processing element 20. The width of the reset pulse is chosen to be larger than the time necessary to reach stable oscillation plus the time necessary for the reset operationproper. After termination of the reset pulse, data processing element 20 reads the data from data receiving module 24, processes the data as far as necessary and accordingly writes out data to data controlled module 32. When this task has been performed, data processing element 20 goes into the stop mode, which is activated by software, and sends thereby a stop signal via signal detector 25 to switching element 28, which thereupon switches the power supply to oscillator 22 from full supply to a stand-by supply.

BEHAVIOUR OF APPARATUS WITH TIME.

Figure 2 shows an exemplary behaviour of the apparatus between two interrupts, lying a time T_x apart.As soon as an interrupt is detected, which occurs at an instant A, the oscillator switches from its stand-by, non-oscillating mode to its oscillating mode, while the data processing element is reset into an initial state. This operation is completed before the end of the reset pulse. The length of the reset pulse t_o is larger than the settling time of the oscillator as the reset operation requires stable oscillations. In practice t_o is made much larger than this settling time of the oscillator in order to stay within a safety range to guarantee a reset taking place under varying conditions (e.g. temperature drift). After termination of the reset pulse the data processing element becomes operating. The task of the data processing element takes a time t_t. At the end of this time interval t_t the data processing element goes into the stop mode under software control, whereby putting the oscillator into the stand-by mode via a stop signal, the data processing element requiring a time t_o to settle in its stop mode. For conversion it is assumed that the time t_o for reaching the initial state equals the time for reaching the stop mode. At instant B the apparatus is ready again to accept a next interrupt.

CALCULATION OF THE ENERGY CONSUMPTION.

Figure 3 comprises the formulae according to which the optimal oscillator frequency is determined in order to minimize energy consumption. In formula (1) is defined the duty cycle of the system which is the fraction of the interval between two successive interrupts, in which the system is operating. As indicated this duty cycle is represented by a number between zero and one. Because the supplies voltages (V_{CC} and V_{SS}) are kept constant, the averate current I_{av} must be minimized. In formula (2) is given the average amount of current passing through the data processing element between two successive interrupts. In the first instance the oscillator current is ignored because it is relatively small. This average current consists of a first part, present during operation, and a second part, present during the stop mode. The current I_{op} necessary in the operating mode depends approximately linearly on the clock frequency f and also on parameters α and β, determined by thesilicon

characteristics of the data processing element, within the frequency interval of interest and is stated by formula (3). The current in the stop mode I_{stop} is a constant and very much smaller than the operating current and is given by formula (4). The duty cycle (1) too depends on the frequency via the duration of the period, in which the data processing element is in the operating mode, this period being a function of the frequency, the number of instructions N executed within this period and the average number of clock cycles per instruction C. The expression for this period in these terms is formula (5). As the duty cycle (1) equals one or is smaller than one, formulae (1) and (5) determine a lower limit for the usable oscillator frequency, at which it is just possible to execute the give number of instructions between two successive interrupts. This lowest usable frequency is given in formula (6). Substituting (3) and (4) into (2), (5) into (1), and (1) thereafter into (2), gives formula (7).Minimizing expression (7) with respect to the frequency leads to the optimal frequency f_{opt} of formula (8). Finally, the current consumed by the data processing element, clocked with frequency (8) in the operation mode, is the minimum, represented by formula (9). However, it must be checked whether this optimal frequency is permitted, since there exists a lower frequency limit, which is given by formula (6). This problem will be discussed in the light of Figure 4.

DESCRIPTION OF A TYPICAL REALIZATION.

An exemplary data processing apparatus is a portable telephone forming a part of a Portable Automatic Telephone System. Such a portable telephone comprises a modulator/demodulator connected to a microcontroller, e.g. a PCB80C31 (Philips Data Handbook IC14N, 1985, pp. 187-213). Typical values for some quantitites characterizing a PCB80C31 - microcontroller are: $\alpha = 1.3\times10^{-9}$Asec; $\beta = 8\times10^{-4}$A; $\theta = 5\times10^{-5}$A; $t_o = 10^{-3}$sec; C = 20. If information packets enter the telephone every T = 0.5 sec, each packet requiring an amount of N = 2000 instructions to be executed, the most profitable oscillator frequency is equal to 3.5 MHz, as can be calculated with the formulae in Figure 3. In this application the invention yields profit in that the frozen oscillator cannot cause interference with identification bits in each information packet. As a consequence the receiving part of the data processing apparatus may be constructed as a highly sensitive receiver.

TYPICAL GRAPH OF ENERGY CONSUMPTION VERSUS FREQUENCY.

Figure 4 is a typical graph of the average current consumed by the data processing element between two successive interrupts as a function of the clock frequency, this information being comprised in formula (7) and being of the form:
$I_{av} = Kf + \frac{M}{f} + L$, K, L, M are constants specified in formulae (1) through (5).
We distinguish two cases:

1) The lowest usable frequency, as given in formula (6), is smaller than or equal to the optical frequency of formula (8).
2) The lowest usable frequency (6) is larger than or equal to the optimal frequency (8).

Whether the optimal frequency is larger than the lowest usable frequency or not depends on the silicon parameters in formula (3), on the amount of clock cycles, necessary for the data processing element to execute the required instructions, on the interrupt rate and on the settling time of the data processing element.
In case 1) the most profitable frequency is equal to the optimal frequency of formula (8) in order to have a minimum energy consumption.
In case 2) the most profitable frequency at which the energy consumption is at a minimum equals the lowest usable frequency. For case 1) the lowest usable frequency lies on the left of the optical frequency in Figure 4 and is marked with a single asterisk, whereas for case 2) the lowest usable frequency lies on the right of the optimal freuqency and is marked with double asterisks.

CALCULATION OF A NEAR OPTIMUM REGION.

To obtain a low energy consumption within a fraction δ of the attainable minimum in practice, say 10%, the frequency must lie in the frequency interval given by formulae (10) in case 1), or in the frequency interval of formulae (11) in case 2) as can readily be deduced from formulae (6) to (9). When, instead of switching between the stop mode and the operating mode, the switching between the idle mode and the operating mode is used, the settling time, the amount of instructions to be executed and the interrupt rate being the same, the average current consumption is given by formula (13), in which formula is substituted the (approximate) current - against-frequency - characteristic of the data processing element in the idle mode (12) within the frequency interval of interest. Typical values for the parameters characteristic for a PCB80C31 microcontroller are: $\Sigma = 2.5\times10^{-10}$Asec; $\lambda = 7\times10^{-4}$A. Optimizing formula (13) with respect to the frequency delivers the minimum current consumption (14). This minimum current consumption (14) when the idle mode is used exceeds the minimum current consumption (9) using the stop mode. For keeping the energy consumption of the data processing element, when

switched between the operating mode and the stop mode, below the energy consumption of the data processing element that can be attained by switching between the operating mode and the idle mode, the clock frequency must lie in the frequency interval of expression (15) as can be calculated by using formulae (7) and (14).

DETAILED DESCRIPTION OF AN EXEMPLARY CIRCUIT.

Figure 5 pictures a circuit diagram of the oscillator, switching element and the second signal detector, used in the preferred embodiment of the invention according to the block diagram of Figure 1.

In Figure 5 the switching element comprises a reset-set-flipflop 50, pnp-transistor 52, resistor 54 and a signal detecting circuit 56. The oscillator 58 is chosen to be a Colpitts-oscillator for its excellent frequency stability, short response time and high oscillating frequency. The output signal is buffered by amplifier A_1. The signal detector 60 is a differentiating circuit, having a diode D_1 connected to its output, in order to reset the data processing element only when the detector senses an upgoing voltage change. Resistor 54 is chosen to be of high resistance to supply the oscillator 58 with a stand-by current in its stand-by mode, in order to prevent the parasitic capacitor C_p between the control electrode and collector of transistor T_2 in the oscillator 58 from discharging completely, this capacitor being charged while the oscillator is in the operating mode. In this way the settling time of the oscillator is kept sufficiently low. The reset input of flipflop 50 is connected to the output terminal of the first signal detector 26 in Figure 1, the set input of flipflop 50 is connected to the stop signal output of the data processing element 20 via a signal detecting circuit 56, which takes care of supplying the flipflop with a set signal of the right polarity and duration. The data processing apparatus can be made accessible for other than the previously mentioned interrupt signal for generating a reset of the data processing element e.g. by feeding the reset terminal of flip-flop 50 via an OR-gate (not shown). Amplifiers A_1, A_2 and A_3 are fully supplied via transistor 52 when the oscillator needs operating and are kept on a small stand-by supply when theoscillator is in the stand-by mode. A second interrupt following immediately a first interrupt is harmless because of the input/output characteristics of reset-set-flipflop 50.

DESCRIPTION OF AN EXTENDED EMBODIMENT.

In Figure 6 is given a second block diagram of a data processing apparatus according to the invention. This second block diagram differs from that of Figure 1 in having three data receiving modules for receiving data from an environment 70, 72 and 74 instead of one, a selection device 76 connected between these data receiving modules and the data input of data processing element 78, and a clock 82, comprising three different oscillator circuits instead of one oscillator as is the case in Figure 1.

Upon reception of an interrupt signal from one data receiving module, for example data receiving module 70,eselection device 76 conencts the data output of data receiving module 70 to the data input of data processing element 78, feeds this interrupt signal to signal detector 80 and selects in clock 82 an oscillator circuit, thereby disabling transmission of data or of interrupt signals from data receiving modules 72 and 74 to said data input or signal detector 80 respectively. The selected oscillator circuit comprises a resonance circuit which fixes the adapted clock frequency of the pulses, fed into the clock input of data processing element 78. The adapted clock frequencies are determined as is described with the help of Figures 3 and 4 and depend among others on the amount of instructions to be executed, required by the data throughput of the data receiving modules 70.

After execution of the instructions required by data receiving module 70, data processing element 78 sends a stop signal to selection device 76 via signal detector 92, which thereby disconnects the data output of data receiving module 70 from said data input and restores the connection from the interrupt signal outputs of data receiving modules 72 and 74 to signal detector 80. The operation of the apparatus of Figure 6 is further analogous to that of the apparatus of Figure 1.

DETAILED DESCRIPTION OF A SECOND EXEMPLARY CIRCUIT.

In Figure 7 a hardware implementation is given of the selection device 76 and clock circuit 82 in Figure 6. Although the embodiment of the invention in Figure 6 comprises only three data receiving modules, extension to more data receiving modules is straightforward. Therefore the former case will be examined.

Data receiving modules 70, 72 and 74 in Figure 6 have their data outputs connected to the data input of data processing element 78 via transistors 228, 230 and 232 respectively, and have their interrupt signal outputs connected to the reset terminals of reset-set-latches 222, 224 and 226 via two transistors in series 210/212, 214/216 and 218/220 respectively.

The set terminal of each reset-set-latch is connected to the stop signal output of data processing

element 78 via a signal detector 92. The first latch output terminals of reset-set-latches 222, 224 and 226 are connected to the control electrode of transistors 228, 230 and 232 respectively. The second latch output terminal of reset-set-latch 222 is connected to the control electrode of transistors 214 and 218, the second latch output terminal of reset-set-latch 224 is connected to the control electrode of transistor 210 and 220 and the second latch output terminal of reset-set-latch 226 is connected to the control electrode of transistors 212 and 216. The reset terminal of each reset-set-latch is connected to an input terminal of an OR-gate 23. The output terminal of said OR-gate is connected to the input of signal detector 80 in Figure 6. The first latch output terminals of reset-set-latches 22, 224 and 226 are connected to the control electrode of transistors 238, 240 and 242 respectively.

We assume the data processing element 78 in Figure 6 initially to be in the stop mode, which mode determines the initial state of reset-set-latches 222, 224 and 226. In this initial state transistors 228, 230, 232 238, 240 and 242 are blocked, while transistors 210/212, 214/216 and 218/220 are conducting. At a certain moment one of the data receiving modules sends an interrupt signal, for instance data receiving module 70. This signal passes through transistors 210/212 and switches the state of reset-set-latch 222. Thereupon transistor 228 is rendered conducting thereby connecting the data output of data receiving module 70 to said data input and transistors 214 and 218 are blocked, thereby preventing reset-set-latches 224 and 226 from switching. At the same time, signal detector 80 receives via OR-gate 234 the interrupt signal and an oscillator circuit, comprising resonant circuit 244, is selected in clock circuit. As soon as the data processing element sends a stop signal, reset-set-latch 222 is switched back, which leads to the blocking of transistors 228 and 238 and the conducting of transistors 214 and 218. Then the apparatus is ready again to manage a new interrupt signal.

Claims

1. A data processing apparatus comprising:
   - a data processing element (20, 78) having an operating mode and a stop mode, and comprising a data input, a first data output, a reset signal input, a clock input, a stop signal output and first power supply terminal means for supplying power to the data processing element;
   - oscillator means (22, 82) for feeding said clock input with clock pulses, having second power supply terminal means (29) for power reception;
   - a data receiving module (24, 70, 72, 74, 76) for receiving external data, said module having a second data output connected to the data input;
   wherein said data processing element (20, 78) has reset means for under combined control of a reset signal and a series of clock pulses attaining an initial state within a predetermined time interval, characterized in that the apparatus further comprises:
   - switching means (28, 84), interconnected between said first and second power supply terminal means, and having a first control input for detecting an interrupt signal from said data receiving module for thereupon driving said switching means to transmit operating power to said second supply terminal means and a second control input fed by said stop signal output for upon detection of a stop signal driving said switching means (28, 84) to transmit stand-by power to said second supply terminal means;
   - a transition signal detector (30, 86) connected to said switching means (28, 84) for upon detecting any transition from said stand-by power transmitting state to said operating power transmitting state generating said reset signal, that has a trailing edge only after termination of said time interval.

2. A data processing apparatus as claimed in claim 1, characterized in that said switching means (28, 84) comprise a reset-set-latch (50) having its reset input fed by an interrupt-signal-detector (26, 80) that is connected to said first control input for detecting the interrupt signal produced by said data receiving module (24, 76), its set input connected to a stop-signal detector (25, 92, 56), that is connected to said second control input and that is fed by said stop signal output for detecting the stop signal, and having an output terminal connected to a control electrode of a transistor, that has its conduction path connected between an input of said transition-signal detector (30, 86) and said second power supply terminal means.

3. A data processing apparatus as claimed in claims 1 or 2, comprising at least a first (70) and a second (72) data receiving module, each having a respective second data output for forwarding data to said data processing element and a respective interrupt signal output for forwarding the interrupt signal characterized

element 78 via a signal detector 92. The first latch output terminals of reset-set-latches 222, 224 and 226 are connected to the control electrode of transistors 228, 230 and 232 respectively. The second latch output terminal of reset-set-latch 222 is connected to the control electrode of transistors 214 and 218, the second latch output terminal of reset-set-latch 224 is connected to the control electrode of transistor 210 and 220 and the second latch output terminal of reset-set-latch 226 is connected to the control electrode of transistors 212 and 216. The reset terminal of each reset-set-latch is connected to an input terminal of an OR-gate 23. The output terminal of said OR-gate is connected to the input of signal detector 80 in Figure 6. The first latch output terminals of reset-set-latches 22, 224 and 226 are connected to the control electrode of transistors 238, 240 and 242 respectively.

We assume the data processing element 78 in gure 6 initially to be in the stop mode, which mode determines the initial state of reset-set-latches 222, 224 and 226. In this initial state transistors 228, 230, 232 238, 240 and 242 are blocked, while transistors 210/212, 214/216 and 218/220 are conducting. At a certain moment one of the data receiving modules sends an interrupt signal, for instance data receiving module 70. This signal passes through transistors 210/212 and switches the state of reset-set-latch 222. Thereupon transistor 228 is rendered conducting thereby connecting the data output of data receiving module 70 to said data input and transistors 214 and 218 are blocked, thereby preventing reset-set-latches 224 and 226 from switching. At the same time, signal detector 80 receives via OR-gate 234 the interrupt signal and an oscillator circuit, comprising resonant circuit 244, is selected in clock circuit. As soon as the data processing element ends a stop signal, reset-set-latch 222 is switched back, which leads to the blocking of transistors 228 and 238 and the conducting of transistors 214 and 218. Then the apparatus is ready again to manage a new interrupt signal.

Claims

1. A data processing apparatus comprising:
   - a data processing element (20, 78) having an operating mode and a stop mode, and comprising a data input, a first data output, a reset signal input, a clock input, a stop signal output and first power supply terminal means for supplying power to the data processing element;
   - oscillator means (22, 82) for feeding said clock input with clock pulses, having second power supply terminal means (29) for power reception;
   - a data receiving module (24, 70, 72, 74, 76) for receiving external data, said module having a second data output connected to the data input;

   wherein said data processing element (20, 78) has reset means for under combined control of a reset signal and a series of clock pulses attaining an initial state within a predetermined time interval, characterized in that the apparatus further comprises:
   - switching means (28, 84), interconnected between said first and second power supply terminal means, and having a first control input for detecting an interrupt signal from said data receiving module for thereupon driving said switching means to transmit operating power to said second supply terminal means and a second control input fed by said stop signal output for upon detection of a stop signal driving said switching means (28, 84) to transmit stand-by power to said second supply terminal means;
   - a transition signal detector (30, 86) connected to said switching means (28, 84) for upon detecting any transition from said stand-by power transmitting state to said operating power transmitting state generating said reset signal, that has a trailing edge only after termination of said time interval.

2. A data processing apparatus as claimed in claim 1, characterized in that said switching means (28, 84) comprise a reset-set-latch (50) having its reset input fed by an interrupt-signal-detector (26, 80) that is connected to said first control input for detecting the interrupt signal produced by said data receiving module (24, 76), its set input connected to a stop-signal detector (25, 92, 56), that is connected to said second control input and that is fed by said stop signal output for detecting the stop signal, and having an output terminal connected to a control electrode of a transistor, that has its conduction path connected between an input of said transition-signal detector (30, 86) and said second power supply terminal means.

3. A data processing apparatus as claimed in claims 1 or 2, comprising at least a first (70) and a second (72) data receiving module, each having a respective second data output for forwarding data to said data processing element and a respective interrupt signal output for forwarding the interrupt signal characterized

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in that the data processing apparatus furthermore comprises:

- a selection means (76) fed in parallel by said second data outputs and fed in parallel by said interrupt signal outputs, said selection means having:
- first gating means (210, 212, 214, 216, 218, 220) for gating a first received interrupt signal to said first control input;
- second gating means (228, 230, 232) for gating data associated to said first received interrupt signal to said data processing element (78);
- disabling means (222, 224, 226) for upon reception of said first received interrupt signal disabling said first and second gating means for gating any interrupt signal or data from another data receiving module than the one generating said first received interrupt signal;
- enabling means (222, 224, 226) connected to said second control input for upon reception of said stop signal reenabling said first and second gating means.

4. A data processing apparatus as claimed in claim 2 and 3, having a number of $j \geq 2$ data receiving modules (70, 72, 74), each having a respective second data output and a respective interrupt signal output, characterized in that said selection means comprises:

- a number of j reset-set-latches (222, 224, 226), each having its set terminal connected to said stop-signal detector;
- a number of j AND-gating means ((210, 212), (214, 216), (218, 220)), each having (j-1) gate inputs and connecting a respective interrupt signal output to an associated reset terminal;
- a number of j interface gating means (228, 230, 232), each connecting a respective second data output to the data input and having a blocking state, a passing state and a state control input connected to a first output terminal of an associated reset-set-latch (222, 224, 226), for upon reception of a blocking-signal being driven to the blocking state and upon reception of a pass-signal being driven to the passing state;
- a j-input OR-gating means (234) fed by said j reset terminals and feeding the interrupt-signal detector;

whereby AND-gating means of rank number k, $1 \leq k \leq j$, connecting data receiving module number k to reset-set-latch number k, has its (j-1) gate inputs connected to respective second output terminals of reset-set-latches with numbers $m \neq k$, $1 \leq m \leq j$.

5. A data processing apparatus as claimed in claim 4 or 5, characterized in that said oscillator means (22, 82) comprise a plurality of oscillator circuits (244, 246, 248), each for generating clock pulses of an associated frequency, and a selection input (238, 240, 242) connected to said selection means for upon reception of a selection signal thereupon selecting one oscillator circuit to be connected to said clock output, between said selection means receiving an interrupt signal and the next following stop signal.

6. A data processing apparatus as claimed in any of the preceding claims, characterized in that while said data processing elements (20, 78) is in said stop mode a resistor (54) is connected between said second power supply terminal means and said oscillator means (62, 82) as a pass-by for a stand-by current.

7. A data processing apparatus as claimed in any of the preceding claims, characterized in that the data processing apparatus further comprises first amplifier means having third power supply terminal means connected to said second power supply terminal means, for amplifying said clock pulses.

8. A data processing apparatus as claimed in any of the preceding claims, characterized in that the data processing apparatus further comprises second amplifier means having fourth power supply terminal means connected to said second power supply terminal means, for amplifying said stop signal.

9. A data processing apparatus as claimed in any one of the preceding claims, characterized in that at least one data controlled module (32) is connected to said first data output.

Revendications

1. Appareil de traitement de données comportant:
   - un élément de traitement de données (20, 78) ayant un mode de fonctionnement et un mode d'arrêt et comportant une entrée de données, une première sortie de données, une entrée de signal de rétablissement, une entrée d'horloge, une sortie de signal d'arrêt et une première borne d'alimentation pour alimenter l'élément de traitement de données;
   - des moyens oscillateurs (22, 82) pour fournir des impulsions d'horloge à ladite

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entrée d'horloge, moyens présentant une deuxième borne d'alimentation pour la réception de puissance;

- un module de réception de données (24, 70, 72, 74, 76) pour recevoir des données externes, ledit module présentant une deuxième sortie de données reliée à l'entrée de données;

appareil dans lequel ledit élément de traitement de données (20, 78) présente des moyens de rétablissement pour atteindre un état initial dans un intervalle de temps prédéterminé, sous la commande combinée d'un signal de rétablissement et d'une série d'impulsions d'horloge, caractérisé en ce que l'appareil comporte en outre:

- des moyens de commutation (28,84) reliés entre lesdites premières et deuxièmes bornes d'alimentation et présentant une première entrée de commande pour détecter un signal d'interruption en provenance dudit module de réception de données pour exciter ensuite lesdits moyens de commutation aiin de transmettre la puissance de fonctionnement auxdites deuxièmes bornes d'alimentation, et présentant une deuxième entrée de commande alimentée par ladite sortie de signal d'arrêt pour exciter, lors de la détection d'un signal d'arrêt, lesdits moyens de commutation (28, 84), afin de transmettre une puissance d'attente auxdites deuxièmes bornes d'alimentation;
- un détecteur de signaux de transition (30, 86) relié auxdits moyens de commutation (28, 84) pour engendrer ledit signal de rétablissement lors de la détection de toute autre transition dudit état de transmission de puissance d'attente audit état de transmission de puissance de fonctionnement, le signal de rétablissement ne présentant un flanc arrière qu'après la fin dudit intervalle de temps.

2. Appareil de traitement de données selon la revendication 1, caractérisé en ce que lesdits moyens de commutation (28, 84) comportent une bascule de rétablissement-établissement (50) ayant une entrée de rétablissement alimentée par un détecteur de signaux d'interruption (26, 80) relié à ladite première entrée de commande pour détecter le signal d'interruption fourni par ledit module de réception de données (24, 76), et une entrée d'établissement reliée à un détecteur de signaux d'arrêt (25, 92, 56) relié à ladite deuxième entrée de commande et alimenté par ladite sortie de signal d'arrêt pour détecter le signal d'arrêt, ainsi qu'une borne de sortie reliée à une électrode de grille d'un transistor dont le trajet de conduction est relié entre une entrée dudit détecteur de signaux de transition (30, 86) et lesdits deuxièmes bornes d'alimentation.

3. Appareil de traitement de données selon les revendications 1 ou 2, comportant au moins un premier (70) et un deuxième (72) module de réception de données ayant chacun une deuxième sortie de données pour envoyer des données auxdits éléments de traitement de données ainsi qu'une sortie de signal d'interruption pour acheminer le signal d'interruption, caractérisé en ce que l'appareil de traitement de données comporte en outre:

- des moyens de sélection (76) alimentés en parallèle par lesdites deuxièmes sorties de données et alimentés en parallèle par lesdites sorties de signal d'interruption,

lesdits moyens de sélection présentant:

- de premiers moyens de porte (210, 212, 214, 216, 218, 220) pour laisser passer vers ladite première entrée de commande un signal d'interruption reçu en premier lieu
- de deuxièmes moyens de porte (228, 230, 232) pour laisser passer vers ledit élément de traitement de données (78) des données associées audit signal d'interruption reçu en premier lieu;
- des moyens de blocage (222, 224, 226) pour empêcher, lors de la réception du premier signal d'interruption reçu, lesdits premiers et deuxièmes moyens de porte de laisser passer tout autre signal d'interruption ou données d'un autre module de réception de données que celui engendrant ledit signal d'interruption reçu en premier lieu;
- des moyens de déclenchement (222, 224, 226) reliés à ladite deuxième entrée de commande pour redéclencher lesdits premiers et deuxièmes moyens de porte lors de la réception dudit signal d'arrêt.

4. Appareil de traitement de données selon les revendications 2 et 3, ayant un nombre $j \geq 2$ de modules de réception de données (70, 72, 74) ayant chacun une deuxième sortie de données et une sortie de signal d'interruption, caractérisé en ce que lesdits moyens de sélection comportent:

- un nombre j de bascules de rétablissement-établissement (222, 224, 226), la borne d'établissement de chaque

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bascule étant reliée audit détecteur de signaux d'arrêt;

- un nombre j de moyens de porte ET (-(210, 212,), (214, 216), (218, 220)), ayant chacun (j-1) entrées de porte et reliant une sortie de signal d'interruption à une borne de rétablissement associée;
- un nombre j de moyens de porte d'interface (228, 230, 232) reliant chacun une deuxième sortie de données à l'entrée de données et présentant un état de blocage et un état passant ainsi qu'une entrée de commande d'état reliée à une première borne de sortie d'une bascule de rétablissement-établissement associé (222, 224, 226) pour être mis en état de blocage lors de la réception d'un signal de blocage et en état passant lors de la réception d'un signal de passage.
- une porte OU (234) à j entrées alimentés par lesdites j bornes de rétablissement et alimentant le détecteur de signaux d'interruption;

le moyen de porte ET de numéro d'ordre k, $1 \leq k \leq j$, qui relie le module de réception de données de numéro k à la bascule de (j-1) rétablissement-établissement de numéro k, ayant ses entrées de porte reliées à des deuxièmes bornes de sortie respectives des bascules de rétablissement-établissement ayant les numéros $m \neq k$, $1 \leq m \leq j$.

5. Appareil de traitement de données selon la revendication 4 ou 5, caractérisé en ce que lesdits moyens oscillateurs (22, 82) comportent une pluralité de circuits oscillateurs (244, 246, 248), destinés à engendrer chacun des impulsions d'horloge de fréquence associée, et une entrée de sélection (238, 240, 242) reliée auxdits moyens de sélection pour sélectionner, après la réception d'un signal de sélection, un circuit oscillateur devant être relié à ladite sortie d'horloge entre l'instant où lesdits moyens de sélection reçoivent un signal d'interruption et l'instant où ils reçoivent le signal d'arrêt suivant.

6. Appareil de traitement de données selon l'une quelconque des revendications précédentes, caractérisé en ce que, pendant que lesdits éléments de traitement (20, 78) sont en mode d'arrêt, une résistance (54) est reliée entre lesdites deuxièmes bornes d'alimentation et lesdits moyens oscillateurs comme dérivation pour un courant d'attente.

7. Appareil de traitement de donnés selon l'une quelconque des revendications précédentes, caractérisé en ce que l'appareil de traitement de données comporte en outre de premiers moyens amplificateurs présentant de troisièmes bornes d'alimentation reliées auxdites deuxièmes bornes d'alimentation pour amplifier lesdites impulsions d'horloge.

8. Appareil de traitement de données selon l'une quelconque des revendications précédentes, caractérisé en ce que l'appareil de traitement de données comporte en outre de deuxièmes moyens amplificateurs ayant de quatrième bornes d'alimentation reliées auxdites deuxièmes bornes d'alimentation pour amplifier ledit signal d'arrêt.

9. Appareil de traitement de données selon l'une quelconque des revendications précédentes, caractérisé en ce qu'au moins un module commandé par des données (32) est relié à ladite première sortie de données.

Patentansprüche

1. Datenverarbeitungsanordnung mit:
   - einem Datenverarbeitungselement (20, 78) mit einer Arbeitsbetriebsart und einer Stoppbetriebsart, das einen Dateneingang, einen ersten Datenausgang, einen Rücksetzsignaleingang, einen Takteingang, einen Stoppsignalausgang und erste Speisestromanschlußmittel zur Stromversorgung des Datenverarbeitungselements umfaßt;
   - Oszillatormitteln (22, 82) zur Speisung des Takteingangs mit Taktimpulsen, die zweite Speisestromanschlußmittel (29) zum Empfang eines Speisestroms haben;
   - einem Datenempfangsmodul (24, 70, 72, 74, 76) zum Empfang externer Daten, das einen zweiten mit dem Dateneingang verbundenen Datenausgang hat;

   worin das Datenverarbeitungselement (20, 78) Rücksetzmittel zum Erreichen eines Anfangszustandes innerhalb eines vorgegebenen Zeintintervalls bei kombinierter Steuerung eines Rücksetzsignals und einer Reihe von Taktimpulsen hat, dadurch gekennzeichnet, daß die Anordnung außerdem:
   - Schaltmittel (28, 84) umfaßt, die zwischen die ersten und zweiten Speisestromanschlußmittel geschaltet sind und einen ersten Steuereingang zur Detektion eines von dem Datenempfangsmodul stammenden Unterbrechungssignals haben, um daraufhin die Schaltmittel dazu-

zubringen, den zweiten Speisestromanschlußmitteln Arbeitsspeisestrom zuzuführen, und einen zweiten Steuereingang, der von dem Stoppsignalausgang gespeist wird, um nach Detektion eines Stoppsignals die Schaltmittel (28, 84) dazuzubringen, den zweiten Speisestromanschlußmitteln Stand-by-Speisestrom zuzuführen;

- einen mit den Schaltmitteln (28, 84) verbundenen Übergangssignaldetektor (30,86), um bei Detektion jedes Übergangs vom Zustand der Stand-by-Speisestromzuführung zum Zustand der Arbeitspeisestromzuführung das genannte Rücksetzsignal zu erzeugen, das nur nach Ablauf des genannten Zeitintervalls eine Hinterflanke aufweist.

Datenverarbeitungsanordnung nach Anspruch 1, dadurch gekennzeichnet, daß die Schaltmittel (28, 84) einen Rücksetz-Setz-Latch (50) enthalten, dessen Rücksetzeingang von einem mit dem ersten Steuereingang verbundenen Unterbrechungssignaldetektor (26, 80) zur Detektion des von dem Datenempfangsmodul (24, 76) erzeugten Unterbrechungssignals gespeist wird, dessen Setzeingang mit einem Stoppsignaldetektor (25, 92, 56) verbunden ist, der mit dem zweiten Steuereingang verbunden ist und der von dem Stoppsignalausgang zur Detektion des Stoppsignals gespeist wird, und der einen mit einer Steuerelektrode eines Transistors verbundenen Ausgangsanschluß hat, wobei der Leitungspfad des Transistors zwischen einen Eingang des Übergangssignaldetektors (30, 86) und die zweiten Speisestromanschlußmittel geschaltet ist.

3. Datenverarbeitungsanordnung nach Anspruch 1 oder 2, mit mindestens einem ersten (70) und einem zweiten (72) Datenempfangsmodul, die jeweils einen jeweiligen zweiten Datenausgang zum Weitersenden von Daten zu dem Datenverarbeitungselement und einen jeweiligen Unterbrechungssignalausgang zum Weitersenden des Unterbrechungssignals umfassen, dadurch gekennzeichnet, daß die Datenverarbeitungsanordnung außerdem enthält:

- ein Selektionsmittel (76), das von den zweiten Datenausgängen parallel gespeist und von den Unterbrechungssignalausgänge parallel gespeist wird, wobei das Selektionsmittel:
- erste Gatterschaltungsmittel (210, 212, 214, 216, 218, 220) zum Durchschalten eines ersten empfangenen Unterbrechungssignals an den genannten ersten Steuereingang enthält;
- zweite Gatterschaltungsmittel (228, 230, 232) zum Durchschalten von mit dem ersten Unterbrechungssignal verknüpften Daten an das Datenverarbeitungselement (78);
- Abschaltmittel (222, 224, 226,), um beim Empfang des ersten empfangenen Unterbrechungssignals die ersten und zweiten Gatterschaltungsmittel zum Durchschalten jedes Unterbrechungssignals oder jeder Daten von einem anderen als dem das erste empfangene Unterbrechungssignal erzeugende Datenempfangsmodul abzuschalten;
- in Arbeitslage schaltende Mittel (222, 224, 226), die mit dem zweiten Steuereingang verbunden sind, um beim Empfang des Stoppsignals die ersten und zweiten Gatterschaltungsmittel erneut in Arbeitslage zu schalten.

4. Datenverarbeitungsanordnung nach den Ansprüchen 2 und 3, mit einer Anzahl von $j \geq 2$ Datenempfangsmodulen (70,72, 74), die je einen zweiten Dateneingang und einen Unterbrechungssignaleingang haben, dadurch gekennzeichnet, daß die genannten Selektionsmittel:

- eine Anzahl von j Rücksetz-Setz-Latches (222, 234, 226), die jeweils einen mit dem Stoppsignaldetektor verbundenen Anschluß haben;
- eine Anzahl von j UND-Gatterschaltungsmitteln (210, 212), (214, 216), (218, 220), die jeweils (j-1) Toreingänge haben und einen jeweiligen Unterbrechungssignalausgang mit einem zugehörigen Rücksetzanschluß verbinden;
- eine Anzahl von j Schnittstellen-Gatterschaltungsmitteln (228, 230, 232), die je einen zweiten Datenausgang mit dem Dateneingang verbinden und einen Sperrzustand, einen Durchlaßzustand und einen mit einem ersten Ausgangsanschluß eines zugehörigen Rücksetz-Setz-Latches (222, 224, 226) verbundenen Zustandssteuereingang haben, um bei Empfang eines Sperrsignals in den Sperrzustand und bei Empfang eines Durchlaßsignals in den Durchlaßzustand gebracht zu werden;
- ein j-Eingang-ODER-Gatterschaltungsmittel (234), das von den j Rücksetzeingängen gespeist wird und den Unterbrechungssignaldetektor speist; umfassen,

wobei die (j-1) Gattereingänge des UND-Gatterschaltungsmittels mit der Ordnungszahl k, $1 \leq k \leq j$, die das Datenempfangsmodul k mit

dem Rücksetz-Setz-Latch der Zahl k verbinden, mit den jeweiligen zweiten Ausgangsklemmen von Rücksetz-Setz-Latches mit den Zahlen $m \neq k$, $1 \leq m \leq j$ verbunden sind.

5. Datenverarbeitungsanordnung nach Anspruch 4 oder 5, dadurch gekennzeichnet, daß das Oszillatormittel (22, 82) eine Vielzahl von Oszillatorschaltungen (244, 246, 248) umfaßt, jede zur Erzeugung von Taktimpulsen einer zugehörigen Frequenz, und einen mit den Selektionsmitteln verbundenen Selektionseingang (238, 240, 242), zur Selektion einer bei Empfang eines Selektionssignals mit dem Taktusgang zu verbindenden Oszillatorschaltung, zwischen dem Empfang eines Unterbrechungssignals durch die Selektionsmittel und dem nächsten folgenden Stoppsignal.

6. Datenverarbeitungsanordnung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß ein Widerstand (54) zwischen die zweiten Speisestromanschlußmittel und das Oszillatormittel (62, 82) als Umgehung für einen Stand-by-Strom geschaltet wird, solange die Datenverarbeitungselemente (20, 78) in der genannten Stoppbetriebsart sind.

7. Datenverarbeitungsanordnung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die Datenverarbeitungsanordnung außerdem erste Verstärkermittel umfaßt, deren dritte Speisestromanschlußmittel mit den zweiten Speisestromanschlußmitteln verbunden sind, um die Taktimpulse zu verstärken.

8. Datenverarbeitungsanordnung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die Datenverarbeitungsanordnung außerdem zweite Verstärkermittel umfaßt, deren vierte Speisestromanschlußmittel mit den zweiten Speisestromanschlußmitteln verbunden sind, um das Stoppsignal zu verstärken.

9. Datenverarbeitungsanordnung nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß mindestens ein datengesteuertes Modul (32) mit dem ersten Datenausgang verbunden ist.