

SPECIFICATION

Electronic fuze

5 This invention relates to an electronic fuze for a projectile, having a generator for producing the ignition energy, a storage capacitor in which the energy produced by the generator on firing the projectile is stored, a priming cap which is ignited by the energy stored in the storage capacitor, and an electronic circuit controlling safety in front of the barrel, delay on impact, undelayed ignition on impact and self-destruction.

The object of the present invention is to provide an electronic fuze which has an electronic circuit controlling safety in front of the barrel, self-destruction and, alternatively, delay on impact or immediate ignition on impact and which requires such a small current that the energy of a single storage capacitor is sufficient.

According to the invention, the fuze also comprises a stabiliser connected to the storage capacitor, arranged to keep substantially constant the voltage of the electrical energy supplied from the capacitor to the electronic circuit, a switching-on element located between the stabiliser and the electronic circuit, arranged to ensure the functioning of inverters, gates and the like, of the electronic circuit, and delay elements in the line between the storage capacitor and the priming cap, arranged to control the energy supply to the priming cap, wherein the electronic circuit, the stabiliser, the switching-on element and the delay elements together form a solid-state circuit.

An illustrative embodiment of the fuze according to the invention is described in detail in the following text by reference to the drawings, in which:-

Figure 1 shows a fuze;

Figure 2 shows a stabiliser;

Figure 3 shows switching-on elements, and

Figure 4 shows delay elements in a diagrammatic representation.

As shown in *Figure 1*, the fuze has a generator 1, which can be a surge generator, and which produces the energy required for the fuze by means of the acceleration on firing. It is, however, also possible to use a rotary generator which produces the energy required for the fuze by means of spinning acceleration.

The generator 1 is connected to a bridge-connected rectifier 2 which makes it possible to store the energy produced by the generator 1 in a storage capacitor 3.

Since the electrical energy contained in the storage capacitor 3 decreases rapidly on withdrawal and is thus not constant, and in order to reduce the current consumption, the storage capacitor 3 is connected to a stabiliser 4 which regulates the supply voltage to a lower level and which is shown more accurately in *Figure 2* and described in more detail further below.

The stabiliser 4 is connected on one side to a switching-on element 8 and on the other side to an end stage 5 for igniting a priming cap 7. A lock-out element 6 ensures that the priming cap 7 cannot be

ignited prematurely.

The lock-out 6 is shown more accurately in *Figure 3* and described in more detail further below. The end stage 5 contains a thyristor or a transistor as a power switch. The switching-on element 8 is connected to three resetting switches 10, 11 and 12 by means of which a counter 19 and an element 18 for safety in front of the barrel can be reset to their starting position. The counter 19 is connected to a decoder 9, by means of which the priming cap 7 can be triggered.

The last-mentioned elements which are framed by a broken line 22, are shown more accurately in *Figure 3* and described in more detail further below.

The switching-on element 8 is also connected to two oscillators 16 and 17, the oscillations of which can be counted by two counters 19 and 20, for example in order to ensure safety in front of the barrel and self-disintegration. Elements 21 for a delay program are connected on one side to the oscillator 17 and on the other side to the lock-out 6. The counter 19 can be set corresponding to the desired safety in front of the barrel and to the desired self destruction time, and the counter 20 is adjustable corresponding to the desired delay time on impact.

The decoder 9 has programming inputs for setting the self-destruction time.

The two oscillators 16 and 17, the counter 20 and the elements 21 for the delay program, which are framed by a broken line 23, are shown more accurately in *Figure 4* and described in more detail further below.

Finally, the fuze also has an impact switch 13 which is connected via two lock-outs 14 and 15 to the elements 21 for the delay program. The lock-out 14 is controlled by the resetting switches 10 and 11, and the lock-out 15 is controlled by the element 18 for safety in front of the barrel.

The elements 21 for the delay program make a time delay of ignition possible, even in the case of impact ignition by means of the impact switch 13, so that, for example, the projectile can penetrate into the target.

As shown in *Figure 2*, the stabiliser comprises eight MOS-FET transistors T_1 - T_8 (MOS-FET = metal oxide semiconductor field effect transistor). The construction and mode of action of this type of transistors are presumed to be known and are thus not described here in more detail. Each of the transistors T_1 - T_8 has three connections which are designated as source S, drain D and gate G. The transistors T_1 , T_2 , T_4 and T_6 possess P-channels and the transistors T_3 , T_5 , T_7 and T_8 possess N-channels.

A voltage source, in particular the storage capacitor 3 shown in *Figure 1*, is connected to the terminals 24 and 25, and the consumer, that is to say the elements which are framed in *Figure 1* by the broken lines 22 and 23, is connected to the terminals 26 and 27. The storage capacitor delivers the voltage U_1 . The consumer requires a voltage U_2 .

The terminals 24 and 25 are connected to one another on one side by two transistors T_2 and T_8 and on the other side, parallel thereto, by six transistors T_1 , T_3 , T_4 , T_5 , T_6 and T_7 . The terminals 26 and 27 are

connected to one another by the four transistors T_4 , T_5 , T_6 and T_7 .

In the transistor T_1 , the gate and drain are connected to one another and this brings about an approximately constant voltage U_4 between the terminal 24 and a terminal 28. The gate G of the transistor T_2 is connected to this terminal 28. Thus, the transistor T_1 controls the transistor T_2 and brings about a constant current in the connection between the transistor T_2 and the transistor T_8 .

In the transistors T_4 , T_5 and T_6 , the gate and drain are connected to one another, and this brings about a constant voltage drop between the terminal 26 and a terminal 26'. The voltage U_5 is thus dependent on the voltage U_2 . The transistor T_8 is controlled by the voltage difference U_5 .

The mode of action of the stabiliser described is as follows:

The current demand of the consumer changes and brings about fluctuations of the voltage U_2 and hence also of the voltage difference U_5 . When the current demand by the consumer is high, the voltage U_2 falls and the voltage difference U_5 likewise falls. This reduction of the voltage U_5 has the consequence that the resistance of the transistor T_8 increases, and the voltage at the terminal 29 and at the gate G of the transistor T_3 thus also increases and more current flows through the transistor T_3 . This has the consequence that the voltage U_2 rises again.

When the current demand by the consumer is small, the voltage U_2 rises, and thus the voltage U_5 also rises. This increase in the voltage difference U_5 has the consequence that the resistance of the transistor T_8 becomes smaller, and the voltage at the terminal 29 and at the gate G of the transistor T_3 is thus reduced and less current flows through the transistor T_3 . This has the consequence that the voltage U_2 falls again.

In addition to the properties of the transistor T_1 , the voltage drop U_4 is also dependent on the load current i_L in the consumer. With a high current i_L , the voltage difference U_4 becomes greater and the resistance of the transistor T_2 thus becomes smaller. More current flows through the transistor T_2 and more current flows through the transistor T_1 . With a small current i_L , the voltage difference U_4 becomes smaller, and the resistance of the transistor T_2 thus becomes greater. Virtually the same amount of current flows through the transistor T_2 and through the transistor T_1 .

The transistor T_1 , T_2 , T_4 , T_5 , T_6 and T_7 run in the saturation range. The transistor T_3 acts as an impedance transformer. The reference voltage is the threshold voltage of the transistor T_8 . Corresponding to its properties and the magnitude of the consumer current $i_L \times i_L$, the transistor T_1 produces the voltage difference U_4 . Analogously, the transistor T_7 produces the voltage difference U_5 , corresponding to its properties and to the current i_L flowing through the transistors T_4 , T_5 , T_6 and T_7 .

The voltage difference U_4 makes it possible to control the transistor T_2 which serves as the current source. The voltage difference U_5 makes it possible to control the transistor T_8 . The transistors T_4 , T_5 , T_6 ,

and T_7 serve as voltage dividers.

As shown in Figure 3, the switching-on element 8 (Figure 1) comprises three inverters J_1 , J_2 and J_3 as well as two transistors T_{10} and T_{11} and a constant-current source 30. The supply voltage for these three inverters J_1 , J_2 and J_3 is delivered by the stabiliser 4 (Figure 1) and, for this reason, the inverters J_1 , J_2 and J_3 are connected to the output terminals 26 and 27 of the stabiliser 4 according to Figure 2. The inputs of the three inverters J_1 , J_2 and J_3 are connected to the constant-current source 30 which is connected to the input terminal 24 of the stabiliser 4 (Figure 1) and, via the transistor T_{10} (Figure 3), also to the output terminal 27. The outputs of the three inverters J_1 , J_2 and J_3 are connected via a resistor R_3 and via the transistor T_{11} to the output terminal 26 of the stabiliser 4.

The first resetting switch 10 (Figure 1), consisting of a fourth inverter J_4 , the supply voltage of which is likewise delivered by the stabiliser 4, that is to say by the terminals 26 and 27, is connected to the output of the switching-on element 8 (Figure 1), that is to say to the outputs of the inverters J_1 , J_2 and J_3 .

In addition to the switching-on element 8 and the resetting switch 10, there is also a second resetting switch 11 which consists of two switching elements 31 and 32 and of a gate 33. The first switching element 31 has two inputs d and e , of which the input d is connected to the terminal 26 and the other input e is connected to the output of the switching-on element 8, that is to say to the outputs of the inverters J_1 , J_2 and J_3 . Moreover, the first switching element 31 has two outputs, of which one is connected to a gate 33 and the other is connected to the first input g of the switching element 32. The second switching element 32 likewise has two inputs g and f , of which one is connected to the output of the switching element 31 and the other is connected to the oscillator 16 (Figures 1 and 3). Furthermore, the second switching element has two outputs, of which one is connected to a third input of the first switching element 31 and the other is connected to the said gate 33.

The third resetting switch 12 consists of two gates 35 and 36, which form an intermediate store, and of two gates 37 and 38 which form a flip-flop circuit. There is a further gate 39 between the gates 35, 36 and 37, 38. The resetting switch 12 is connected on one side to the resetting switch 10, that is to say to the inverter J_4 , and on the other side to the resetting switch 11, that is to say to the common gate 33 of the two switching elements 31 and 32. In the resetting switch 12, the output of one gate 35 is connected to one input of the other gate 36, the output of which is likewise connected to one input of the gate 35. In the same way, the output of one gate 37 in the resetting switch 12 is connected to one input of the other gate 38, the output of which is in turn connected to one input of the gate 37. The gates 35, 36 on the one hand and the gates 37, 38 on the other hand thus each form a flip-flop circuit. The output of the gate 39, located between the gates 35, 36 and 37, 38, is connected to one input of the gate 38, and the two inputs of the gate 39 are connected on one side to the gates 35, 36 and on the other side to the said

common gate 33 of the two switching-on elements 31 and 32 of the resetting switch 11.

The mode of action of the switching-on and resetting elements described is as follows:

- 5 When the projectile is fired, the generator 1 (Figure 1) produces a current which, via the bridge-connected rectifier 2 (Figure 1) and via the internal resistance of the generator 1, charges the storage capacitor 3 (Figure 1), the voltage U_1 (Figure 10 3) being built up. A constant-current source 30 (Figure 3), not described here in more detail, delivers a current, as a result of which the voltage at the inputs of the three inverters J_1 , J_2 and J_3 also rises approximately to the voltage U_1 , as long as the
- 15 transistor T_{10} is still in the locking condition. The said input voltage U_1 has the effect that the inverters J_1 , J_2 and J_3 become conductive, and the earth potential U_0 is built up at their outputs. Since the outputs of the inverters J_1 , J_2 and J_3 are also connected to the
- 20 gates of the transistors T_{10} and T_{11} via the resistor R_3 , the transistor T_{11} becomes conductive as soon as the stabiliser generates the voltage U_2 . As a result, a current flows from the terminal 26 via the transistor T_{11} to the outputs of the three inverters J_1 , J_2 and J_3 .
- 25 This current is increasing and has the effect that the transistor T_{10} also becomes conductive, as a result of which the input voltage of the inverters J_1 , J_2 and J_3 falls from the value U_1 to the value zero. The disappearance of the input voltage U_1 on the
- 30 inverters J_1 , J_2 and J_3 and the build-up of their supply voltage U_2 have the consequence that the voltage U_3 is built up also at their outputs. The procedure is accelerated by the resistor R_3 which acts as a positive feed-back.
- 35 The converse procedure takes place on the inverter J_4 . Initially, the voltage U_0 which was generated, as described further above, at the outputs of the three inverters J_1 , J_2 and J_3 , prevails at the input of the inverter J_4 . Thus, the voltage U_2 is
- 40 likewise produced at the output of the inverter J_4 and generates a first resetting pulse. This first resetting pulse disappears as soon as the voltage U_2 is produced at the outputs of the inverters J_1 , J_2 and J_3 .
- The said first resetting pulse has the following
- 45 effect:
 - 1) The switching element 32 receives the first resetting pulse at the input *a* (reset input).
 - 2) The switching element 31 also receives a voltage pulse U_2 at the input *d*.
 - 50 3) This voltage pulse U_2 , however, becomes effective only when the switching element 31 receives, at the input *e*, the voltage pulse U_3 from the switching-on element 8.
 - 4) The switching element 31 changes its state from 0
 - 55 to 1 synchronously with the pulse U_3 .
 - 5) The voltage U_3 also switches on the oscillator 16.
 - 6) As soon as the oscillator 16 emits a first oscillation pulse to the switching element 32 at the point *f*, the output pulse 1 of the switching
 - 60 31 is transmitted to the point *g* of the switching element 32 and the output *h* of the switching element 32 delivers a pulse 1 to the gate 33.
 - 7) As mentioned under 3, the switching element 31 has received the voltage pulse U_3 at the input *e* and
 - 65 generates an output pulse which is likewise passed to

the gate 33.

- 8) As soon as the oscillator 16 emits a second oscillation pulse, the switching element 32 is switched over and delivers a pulse 0 to 33.
- 70 9) The switching element 31 thus continuously delivers a pulse 0 to the gate 33 and, under the second oscillation pulse of the oscillator 16, the switching element 32 likewise delivers a pulse 0 to the gate 33, as a result of which the gate 33 delivers a
- 75 second resetting pulse.

The two resetting pulses have the following effect:

- 1) The gates 35, 36 of the resetting switch 12 are switched on by the first resetting pulse and switched back by the second resetting pulse. They serve only
- 80 as an intermediate store since the edge steepness of the switching-on element 8 causes a delay in the second resetting pulse.
- 2) By contrast, the gates 37, 38 are switched on either by the first resetting pulse or by the second
- 85 resetting pulse and are switched back again only when the second resetting pulse disappears.
- 3) The signal generated by the resetting switch 12 cancels the locking of the counter 19.

The operation of the resetting switch 12 is

- 90 presumed as known.
- The delay elements shown in Figure 4 comprise two oscillators 16 and 17 which, although they are shown separately in Figure 1, have a partially common resistance-capacitance member. For the
- 95 oscillator 16, this resistance-capacitance member consists of the capacitance C and the resistance R_1 and, for the oscillator 17, it consists of the same capacitance C and another resistance R_2 . The remaining components of the two oscillators 16-17
- 100 are arranged in a common housing designated as 16-17. The complete oscillator 16 is indicated by the broken field 16, and the complete oscillator 17 is indicated by the broken field 17.

At the point *a*, the oscillator 16 is connected via

- 105 two gates 60 and 61 to the counter 19 (Figure 1) for safety in front of the barrel. At the point *b*, the oscillator 17 is connected via two gates 63 and 64 to the delay program 21 shown in Figures 1 and 4.
- A group of eight transistors T_{21} , T_{22} , T_{23} , T_{24} , T_{25} ,
- 110 T_{26} , T_{27} and T_{28} serves, together with the three gates 62, 63 and 64, for switching over the two oscillators 16 and 17, for example for switching off the oscillator 16 and for switching on the oscillator 17.

This switch-over is necessary since the frequency

- 115 for safety in front of the barrel must be different from that for the delay on impact. A frequency of, for example, 500 Hz is used for safety in front of the barrel and a frequency of, for example, 35 kHz is used for delay on impact.
- 120 Via two diodes D_{13} and D_{14} , the voltage U_3 is applied to one side and the voltage U_0 is applied to the other side of the said eight transistors T_{21} - T_{28} , in order to avoid feedback from the oscillators 16 on the voltage source, which would entail a change in
- 125 frequency.

In addition to the two oscillators 16 and 17, the delay elements also comprise a group of ten gates 50-59. Of these ten gates 50-59, the two inputs of the gate 50 are connected on one side to the impact

- 130 switch 13 (Figure 1) and on the other side to the

element 18 for safety in front of the barrel (Figure 1).

The flip-flop circuit of the gates 51 and 52 is connected to the gate 50 and to the element 18.

One input on one side of the gate 53 is connected to the output of the flip-flop circuit 51, 52 and a second input on the other side is connected to a program switch P4. This program switch P4 emits a pulse 1 when a delay is desired on impact, and it delivers a pulse 0 if no delay is desired. The two inputs of the gate 54 are also connected to this program switch P4. The output of the gate 53 leads to the gates 62 and 60 of the oscillators 16 and 17 and to the delay counter 20.

One side of the gate 56 is connected to the output of the flip-flop circuit 51, 52 and the other side is connected to the gate 54.

One input of the gate 55 is connected to the program switch 4 and the other input is connected to the delay counter 20 (Figures 1 and 4) which exclusively counts the pulses from the oscillator 17.

The two inputs of the gate 57 lead to the outputs of the gates 55 and 56. One input of the gate 58 leads to the output of the gate 57, whilst the other input of the gate 58 leads to the decoder 9 for self-destruction. Finally, one input of the gate 59 leads to the output of the gate 58, whilst the other input of the gate 59 leads to the element 18 for safety in front of the barrel. The output of the gate 59 is connected to the end stage 5 (Figure 1) which contains a thyristor for igniting the priming cap 7 (Figure 1). A lock-out 70, which is not shown in more detail, is likewise connected to the end stage 5. The lock-out 70 can be controlled by the resetting switch 12 (Figure 1). This lock-out 70 is able to prevent a pulse from the gate 59 from reaching the end stage 5.

The mode of action of the delay elements described is as follows:

1. Initially, it is assumed that no delay on impact is desired. The program switch P4 thus delivers a pulse 0. As soon as the projectile hits a target object, the impact switch 13 generates a pulse 1. If, on impact, the projectile has already moved sufficiently far away from the gun, the element 18 for safety in front of the barrel also delivers a pulse 1. Thus, the gate 50 switches over from pulse 1 to pulse 0, and the flip-flop circuit 51 and 52 likewise switches over and transmits the pulse 1 to the inputs of the gates 53 and 56. As stated, the program switch P4 delivers the pulse 0 to the gates 53 and 54. At the output of the gate 53, the pulse 1 is therefore generated. Thus, the oscillator 16 is working and the oscillator 17 remains blocked. Since the inverter output 62 is zero, the transistors T₂₇, T₂₈ are blocked. The inverter output 64 is also zero. The inverter output 53 is one. T₂₁, T₂₂ are blocked. The output of the inverter (formed by the transistors T₂₃ to T₂₆) thus represents such a high resistance that the resistance R₂ has no influence on the frequency response of the oscillator 16. At the output of the gate 54, however, the pulse 1 is generated and, at the output of the gate 56, the pulse 0 is likewise generated.

The gate 55 received the pulse 0 from the program switch P4 and the pulse 0 from the counter 20, and it thus generates a pulse 1. The gate 57 thus receives a

pulse 1 from the gate 55 and a pulse 0 from the gate 56, and therefore, generates a pulse 1.

Before the self-disintegration time, the decoder 9 emits a pulse 0 and the gate 58 receives a pulse 1 from the gate 57 and a pulse 0 from the decoder 9 and in turn generates a pulse 0. As mentioned above, the element 18 for safety in front of the barrel generates the pulse 1 and, after the time for safety in front of the barrel has expired, switches over to "0". The gate 59 thus receives the pulse 0 from both the gate 58 and the element 18 and generates a pulse 1 which is transmitted to the end stage 5, if the lockout 70 is lifted. Ignition thus occurs without delay.

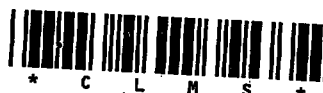
2. If a delay on impact is desired, the program switch P4 delivers the pulse 1.

As soon as the projectile hits a target object, the impact switch 13 generates a pulse 1. If, on impact, the projectile has already moved sufficiently far away from the gun, the element 18 for safety in front of the barrel also delivers a pulse 1. The gate 50 thus switches over from pulse 1 to pulse 0 and the flip-flop circuit 51 and 52 likewise switches over and emits the pulse 1 to the inputs of the gates 53 and 56. As stated, the program switch P4 also delivers the pulse 1 to the gates 53 and 54. At the output of the gate 53, the pulse 0 is thus generated, which is passed on to the oscillator 17. At the output of the gate 54, a pulse 0 is generated, and the gate 56 thus also generates a pulse 1 and ignition without delay is impossible since the gate 57 is now blocking.

The pulse 0 from the gate 53 reaches the gate 60 so that the gate 60 blocks and the counter 19 is switched off. Moreover, the pulse 0 from the gate 53 reaches the gate 62 and the transistors T₂₁ and T₂₂ and, via the gate 62, the transistors T₂₇ and T₂₈. The oscillator output *b* is conductively connected via the gates 63 and 64 to the transistors T₂₃, T₂₄, T₂₅ and T₂₆. These act as inverters and their common output is connected to the resistance R₂, R₂ being R₁. The oscillator 17 thus oscillates at the higher frequency of, for example, 35 kHz and emits pulses to the counter 20. The program switch emits the pulse 1 and the inverter output 51 likewise emits the pulse 1, and the inverter 53 thus emits the pulse 0 at the output and the counter 20 can start to count. As soon as the requisite number of pulses has been counted by the counter 20, a pulse 1 is transmitted to the gate 55 which likewise receives a pulse 1 from P4. As described further above, the end stage 5 can thus be excited via the gates 57, 58 and 59, and the fuze 7 can be ignited.

CLAIMS

1. An electronic fuze for a projectile, comprising a generator for producing the ignition energy, a storage capacitor in which the energy produced by the generator on firing the projectile is stored, a priming cap which is ignited by the energy stored in the storage capacitor, an electronic circuit between the capacitor and the priming cap controlling safety in front of the barrel, delay on impact, undelayed ignition on impact and self-destruction, a stabiliser connected to the storage capacitor, arranged to keep substantially constant the voltage of the electrical



element 18 for safety in front of the barrel (Figure 1).

The flip-flop circuit of the gates 51 and 52 is connected to the gate 50 and to the element 18.

One input on one side of the gate 53 is connected to the output of the flip-flop circuit 51, 52 and a second input on the other side is connected to a program switch P₄. This program switch P₄ emits a pulse 1 when a delay is desired on impact, and it delivers a pulse 0 if no delay is desired. The two inputs of the gate 54 are also connected to this program switch P₄. The output of the gate 53 leads to the gates 62 and 60 of the oscillators 16 and 17 and to the delay counter 20.

One side of the gate 56 is connected to the output of the flip-flop circuit 51, 52 and the other side is connected to the gate 54.

One input of the gate 55 is connected to the program switch 4 and the other input is connected to the delay counter 20 (Figures 1 and 4) which exclusively counts the pulses from the oscillator 17.

The two inputs of the gate 57 lead to the outputs of the gates 55 and 56. One input of the gate 58 leads to the output of the gate 57, whilst the other input of the gate 58 leads to the decoder 9 for self-destruction. Finally, one input of the gate 59 leads to the output of the gate 58, whilst the other input of the gate 59 leads to the element 18 for safety in front of the barrel. The output of the gate 59 is connected to the end stage 5 (Figure 1) which contains a thyristor for igniting the priming cap 7 (Figure 1). A lock-out 70, which is not shown in more detail, is likewise connected to the end stage 5. The lock-out 70 can be controlled by the resetting switch 12 (Figure 1). This lock-out 70 is able to prevent a pulse from the gate 59 from reaching the end stage 5.

The mode of action of the delay elements described is as follows:

1. Initially, it is assumed that no delay on impact is desired. The program switch P₄ thus delivers a pulse 0. As soon as the projectile hits a target object, the impact switch 13 generates a pulse 1. If, on impact, the projectile has already moved sufficiently far away from the gun, the element 18 for safety in front of the barrel also delivers a pulse 1. Thus, the gate 50 switches over from pulse 1 to pulse 0, and the flip-flop circuit 51 and 52 likewise switches over and transmits the pulse 1 to the inputs of the gates 53 and 56. As stated, the program switch P₄ delivers the pulse 0 to the gates 53 and 54. At the output of the gate 53, the pulse 1 is therefore generated. Thus, the oscillator 16 is working and the oscillator 17 remains blocked. Since the inverter output 62 is zero, the transistors T₂₇, T₂₈ are blocked. The inverter output 64 is also zero. The inverter output 53 is one. T₂₁, T₂₂ are blocked. The output of the inverter (formed by the transistors T₂₃ to T₂₆) thus represents such a high resistance that the resistance R₂ has no influence on the frequency response of the oscillator 16. At the output of the gate 54, however, the pulse 1 is generated and, at the output of the gate 56, the pulse 0 is likewise generated.

The gate 55 received the pulse 0 from the program switch P₄ and the pulse 0 from the counter 20, and it thus generates a pulse 1. The gate 57 thus receives a

pulse 1 from the gate 55 and a pulse 0 from the gate 56, and therefore, generates a pulse 1.

Before the self-disintegration time, the decoder 9 emits a pulse 0 and the gate 58 receives a pulse 1 from the gate 57 and a pulse 0 from the decoder 9 and in turn generates a pulse 0. As mentioned above, the element 18 for safety in front of the barrel generates the pulse 1 and, after the time for safety in front of the barrel has expired, switches over to "0". The gate 59 thus receives the pulse 0 from both the gate 58 and the element 18 and generates a pulse 1 which is transmitted to the end stage 5, if the lockout 70 is lifted. Ignition thus occurs without delay.

2. If a delay on impact is desired, the program switch P₄ delivers the pulse 1.

As soon as the projectile hits a target object, the impact switch 13 generates a pulse 1. If, on impact, the projectile has already moved sufficiently far away from the gun, the element 18 for safety in front of the barrel also delivers a pulse 1. The gate 50 thus switches over from pulse 1 to pulse 0 and the flip-flop circuit 51 and 52 likewise switches over and emits the pulse 1 to the inputs of the gates 53 and 56. As stated, the program switch P₄ also delivers the pulse 1 to the gates 53 and 54. At the output of the gate 53, the pulse 0 is thus generated, which is passed on to the oscillator 17. At the output of the gate 54, a pulse 0 is generated, and the gate 56 thus also generates a pulse 1 and ignition without delay is impossible since the gate 57 is now blocking.

The pulse 0 from the gate 53 reaches the gate 60 so that the gate 60 blocks and the counter 19 is switched off. Moreover, the pulse 0 from the gate 53 reaches the gate 62 and the transistors T₂₁ and T₂₂ and, via the gate 62, the transistors T₂₇ and T₂₈. The oscillator output b is conductively connected via the gates 63 and 64 to the transistors T₂₃, T₂₄, T₂₅ and T₂₆. These act as inverters and their common output is connected to the resistance R₂, R₂ being R₁. The oscillator 17 thus oscillates at the higher frequency of, for example, 35 kHz and emits pulses to the counter 20. The program switch emits the pulse 1 and the inverter output 51 likewise emits the pulse 1, and the inverter 53 thus emits the pulse 0 at the output and the counter 20 can start to count. As soon as the requisite number of pulses has been counted by the counter 20, a pulse 1 is transmitted to the gate 55 which likewise receives a pulse 1 from P₄. As described further above, the end stage 5 can thus be excited via the gates 57, 58 and 59, and the fuze 7 can be ignited.

CLAIMS

1. An electronic fuze for a projectile, comprising a generator for producing the ignition energy, a storage capacitor in which the energy produced by the generator on firing the projectile is stored, a priming cap which is ignited by the energy stored in the storage capacitor, an electronic circuit between the capacitor and the priming cap controlling safety in front of the barrel, delay on impact, undelayed ignition on impact and self-destruction, a stabiliser connected to the storage capacitor, arranged to keep substantially constant the voltage of the electrical



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energy supplied from the capacitor to the electronic circuit, a switching-on element located between the stabiliser and the electronic circuit, arranged to ensure the functioning of inverters, gates and the like, of the electronic circuit, and delay elements in the line between the storage capacitor and the priming cap, arranged to control the energy supply to the priming cap, wherein the electronic circuit, the stabiliser, the switching-on element and the delay elements together form a solid-state circuit.

2. A fuze according to Claim 1, wherein the stabiliser comprises a constant-current source having an element providing a reference voltage and a resistance controllable by this element, the current flowing through the resistance being approximately constant and the current flowing through the element being variable, an impedance transformer controllable by the starting voltage, a voltage divider for generating a component voltage, and a reference source which controls the impedance transformer, as a function of the component voltage the stabiliser containing only MOS field effect transistors of the enhancement type, in the element for the reference voltage the drain and the gate being mutually connected, and the gate of the controllable resistance being connected to the gate of the said element.

3. A fuze according to Claim 1, wherein the switching-on element comprises three inverters, the inputs of which are connected to a constant-current source, the inputs of the three inverters can be connected to earth via a field effect transistor, the gate of the field effect transistor being connected to a stabiliser via a second transistor and to the outputs of the three inverters via a resistor, first resetting switch is connected to the switching-on element and a second resetting switch is connected to the stabiliser, and a third resetting switch is connected to the first and second resetting switches.

4. A fuze according to Claim 1, wherein the delay elements contain a first oscillator with a first counter for controlling safety in front of the barrel, a second oscillator with a second counter for controlling the delay on impact, and an impact switch, the two oscillators comprising a partially common resistance/capacitance member wherein the capacitance is common, each oscillator having its own resistance, and a transistor circuit for alternatively switching on one or the other oscillator.

5. An electronic fuze for a projectile, substantially as described with reference with the drawing.