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A METHOD OF PLANARIZATION OF AN INTERMETAL DIELECTRIC LAYER USING CHEMICAL MECHANICAL POLISHING

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

This invention relates to the planarization of an intermetal dielectric layer comprising spin on glass and more particularly to planarization using chemical mechanical polishing without etchback and having an automatic end point.

(2) DESCRIPTION OF THE RELATED ART

U.S. Pat. No. 5,094,972 to Pierce et al. describes the formation of a stop layer of CVD silicon nitride or CVD carbon on the surface of an integrated circuit wafer. Holes are formed in the stop layer and wells are formed in the material below the openings. After processing the device is planarized to the stop layer using abrasive mechanical polishing.

U.S. Pat. No. 4,956,313 to Cote et al. describes forming an insulator layer with holes. The holes are then filled with CVD tungsten which is also formed on the insulator layer. The metal layer and the insulator layer are then subjected to a polish etch in the presence of an abrasive slurry to remove the metal not filling the holes and to planarize the insulator layer.

U.S. Pat. No. 5,472,825 to Sayka describes planarizing a spin on glass layer without the use of a stop layer.

U.S. Pat. No. 4,997,789 to Keller et al. describes planarization using etchback with an aluminum etch stop layer.

U.S. Pat. No. 5,275,963 to Cedarbaum et al. describes planarizing a layer of phosphosilicate glass using chemical mechanical polishing without a stop layer.

This invention describes using chemical mechanical polishing to planarize an intermetal dielectric without using an etchback step. A hard metal cap formed on an electrode pattern is used as a stop for the chemical mechanical polishing step.

SUMMARY OF THE INVENTION

Intermetal dielectric is used to separate levels of metal electrodes in integrated circuit wafers. For dense integrated circuit structures the intermetal dielectric has a very irregular top surface and must be planarized before the next level of metal electrodes can be formed. Spin on glass, SOG, is often used to fill the narrow gaps between the electrodes.

A conventional method of forming and planarizing the intermetal dielectric, IMD, is shown in Figs. 1A and 1B. Fig. 1A shows an integrated circuit wafer 10 with devices formed therein, not shown. A dielectric layer, not shown, may or may not be formed directly over the integrated circuit wafer 10. Metal electrodes 12 are formed on the integrated circuit wafer using blanket deposition of metal and well known photolithographic techniques. A layer of spin on glass 14 is then formed on the integrated circuit wafer 10 filling the gaps between the electrodes 12 but having a very irregular surface. The layer of spin on glass is then etched back and a layer of oxide 16 is formed on the etched back layer of spin on glass.

As shown in Fig. 1B the intermetal dielectric is then planarized using chemical mechanical polishing to remove that part of the layer of oxide 16 and that part of the layer of spin on glass 14 which is above the plane formed by the top surface of the electrodes 12. During the chemical mechanical polishing step the tops of the metal electrodes are exposed. Another layer of oxide or other dielectric, not shown, can then be formed on the intermetal dielectric layer and another layer of metal electrodes can be formed, not shown.

Some of the disadvantages of the conventional method of planarization just described are the cost of the etch back step and the determination of the end point of the chemical mechanical polishing, or CMP, step. If the CMP step is continued too long part of the metal electrodes will be polished away. If the CMP step is stopped too soon there will be dielectric material left over the top of the electrodes.

It is an objective of this invention to provide a method of planarization of an intermetal dielectric which does not require an etch back step and uses a chemical mechanical polishing step which has an automatic end point determination.

This objective is achieved by forming a hard metal cap, such as tungsten, on the soft metal electrodes. The intermetal dielectric is then formed over the electrodes formed of the normal soft metal with a hard metal cap. The intermetal dielectric is then planarized using CMP with an oxide slurry. The hard metal cap will not be polished away by the CMP step and will form an automatic end point to the CMP step. The hard metal cap will not be scratched, corroded, or smeared by the CMP step. Monitoring the current of the motor driving the CMP will provide good endpoint determination since the load on the motor will change significantly when the hard metal cap is reached.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A shows a cross section view of an integrated circuit wafer being planarized using a conventional method after etchback of the spin on glass and formation of the oxide layer and prior to the chemical mechanical polishing.

Fig. 1B shows a cross section view of an integrated circuit wafer being planarized using a conventional method after completion of the chemical mechanical polishing.

Fig. 2 shows a cross section view of an integrated circuit wafer with a layer of soft metal formed on the integrated circuit wafer and a layer of hard metal formed on the layer of soft metal.

Fig. 3 shows a cross section view of an integrated circuit wafer with an electrode pattern formed in the layer of soft metal and the layer of hard metal. A layer of first oxide is formed on the wafer covering the electrode pattern.

Fig. 4 shows a cross section view of an integrated circuit wafer with an electrode pattern formed in the layer of soft metal and the layer of hard metal, a layer of first oxide formed on the wafer covering the electrode pattern, and a layer of spin on glass formed on the layer of first oxide.

Fig. 5 shows a cross section view of an integrated circuit wafer with an electrode pattern formed in the layer of soft metal and the layer of hard metal, a layer of first oxide formed on the wafer covering the electrode pattern, a layer of spin on glass formed on the layer of first oxide, and a layer of second oxide formed on the layer of first oxide.

Fig. 6 shows a cross section view of an integrated circuit wafer with the intermetal dielectric planarized using chemical mechanical polishing.

Fig. 7 shows a cross section view of an integrated circuit wafer after planarization of the intermetal dielectric with a layer of third oxide formed on the planarized intermetal dielectric.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Refer now to Figs. 2-7, there is shown an embodiment of the planarization method of this invention. Fig. 2 shows an integrated circuit wafer 20 with devices formed therein, not shown, and a dielectric layer formed thereon, not shown. A layer of first metal 21, such as Al/Cu/Si, Al/Cu, or the like, having a thickness of between about 3000 and 10,000 Angstroms is formed on the integrated circuit wafer. The first metal is typically soft and would be easily polished away during a chemical mechanical polishing step. Next a layer of second metal 23, such as tungsten, tungsten nitride, titanium nitride, or the like having a first surface 25, a second surface 27, and a thickness of between about 200 and 2000 Angstroms, is formed on the layer of first metal 21. The second surface 27 of the layer of second metal 23 contacts the layer of first metal 21. The first surface 25 of the layer of second metal 23 forms a first plane wherein the integrated circuit wafer 20, the layer of first metal 21, and the layer of second metal 23 are below the first plane. The second metal is sufficiently hard, having a Knoop hardness value equal to or greater than 485 kg/nm^2, that the second metal will resist being polished away by the chemical mechanical polishing step.

Next as shown in Fig. 3 a first pattern is formed in the layer of first metal 22 and the same first pattern is formed in the layer of second metal 24. A layer of first oxide 26, having a thickness of between about 500 and 6000 Angstroms, is then formed on the integrated circuit wafer 20 by means of chemical vapor deposition covering the first pattern formed of the first metal 22 and the second metal 24. As shown in Fig. 4 a layer of spin on glass 28, having a thickness of between about 2000 and 8000 Angstroms, is then formed on the layer of first oxide 26. The layer of spin on glass is then baked at a temperature of between about 150° C and 300° C for between about 0.5 and 5 minutes and cured at a temperature of between about 350° C and 500° C for between about 30 and 240 minutes.

Next, as shown in Fig. 5, a layer of second oxide 30 having a high density and a thickness of between about 3000 and 20,000 Angstroms is formed over the cured layer of spin on glass 28 using plasma assisted chemical vapor deposition. The layer of first oxide 26, the layer of spin on glass 28, and the layer of second oxide 30 make up a first dielectric. Part of the layer of first oxide 26, part of the layer of spin on glass 28, and part of the layer of second oxide 30 are above the first plane defined by the first surface of the layer of second metal.

Next, as shown in Fig. 6, the first dielectric is planarized using chemical mechanical polishing using an oxide slurry, such as colloidal silica. That part of the layer of first oxide 26 above the first plane, that part of the layer of spin on glass 28 above the first plane, and that part of the layer of second oxide 30 above the first plane are removed by the chemical mechanical polishing, or CMP. When the CMP reaches the first pattern formed in the second metal 24 the CMP is unable to remove the hard second metal. The hard second metal stops the progress of the CMP at the first plane. In this way the first pattern formed in the hard second metal 24 provides an automatic end point to the CMP step.

The CMP step is driven by an electric motor powered by an electric current. When the CMP reaches the hard second metal the load on the motor will change significantly and will cause and increase of the electric current powering the CMP step. By monitoring this electric current the endpoint of the CMP step can be easily and accurately determined.

As shown in Fig. 6, that part of the layer of first oxide 26 below the first plane, that part of the layer of spin on glass 28 below the first plane, and that part of the layer of second oxide 30 below the first plane remain

after the chemical mechanical polishing, or CMP, has been completed. Next, as shown in Fig. 7, a layer of third oxide 32 is formed over the planarized first dielectric and processing of the integrated circuit wafer proceeds in a conventional manner.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of planarization, comprising the steps of:

providing an integrated circuit wafer with devices formed therein;

forming a layer of first metal on said integrated circuit wafer;

forming a layer of second metal, having a first surface and a second surface, on said layer of first metal wherein said second metal has a Knoop hardness value equal to or greater than 485 kg/nm^2, said second surface of said layer of said second metal contacts said layer of first metal, and said first surface of said layer of said second metal forms a first plane wherein said layer of said second metal and said layer of first metal are below said first plane;

forming a first pattern in said layer of first metal and said layer of second metal;

forming a layer of first dielectric on said integrated circuit wafer covering said first pattern formed in said layer of first metal and said layer of second metal, wherein part of said layer of first dielectric is above said first plane and part of said layer of first dielectric is below said first plane;

removing that part of said layer of first dielectric above said first plane, thereby planarizing said layer of first dielectric, by means of chemical mechanical polishing wherein said chemical mechanical continues until stopped by said first pattern formed in said layer of second metal;



cleaning said planarized layer of first dielectric; and

forming a layer of second dielectric on said planarized layer of first dielectric.

2. The method of claim 1 wherein forming said layer of first dielectric comprises the steps of:

forming a layer of first oxide on said integrated circuit wafer covering said first pattern formed in said layer of first metal and said layer of second metal, wherein part of said layer of first oxide is above said first plane and part of said layer of first oxide is below said first plane;

forming a layer of spin on glass on said layer of first oxide, wherein part of said layer of spin on glass is above said first plane and part of said layer of spin on glass is below said first plane;

curing said layer of spin on glass; and

forming a layer of second oxide on said layer of spin on glass, wherein part of said layer of second oxide is above said first plane and part of said layer of second oxide is below said first plane.

3. The method of claim 2 wherein said layer of first oxide has a thickness of between about 500 and 6000 Angstroms and is formed using chemical vapor deposition.

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4. The method of claim 2 wherein said layer of spin on glass has a thickness of between about 2000 and 8000 Angstroms.

5. The method of claim 2 wherein said layer of second oxide has a thickness of between about 3000 and 20,000 Angstroms and is formed using plasma assisted chemical vapor deposition.

6. The method of claim 1 wherein said first metal is Aluminum/Silicon/Copper having a thickness of between about 3000 and 10,000 Angstroms.

7. The method of claim 1 wherein said first metal is Aluminum/Copper having a thickness of between about 3000 and 10,000 Angstroms.

8. The method of claim 1 wherein said second metal is Tungsten having a thickness of between about 200 and 2000 Angstroms.

9. The method of claim 1 wherein said second metal is Tungsten Nitride having a thickness of between about 200 and 2000 Angstroms.



10. The method of claim 1 wherein said second metal is Titanium Nitride having a thickness of between about 200 and 2000 Angstroms.

11. The method of claim 1 wherein said chemical mechanical polishing uses an oxide slurry.

12. A method of planarization, comprising the steps of:

providing an integrated circuit wafer with devices formed therein;

forming a layer of first metal on said integrated circuit wafer;

forming a layer of second metal, having a first surface and a second surface, on said layer of first metal wherein said second metal has a Knoop hardness value equal to or greater than 485 kg/nm^2, said second surface of said layer of said second metal contacts said layer of first metal, and said first surface of said layer of said second metal forms a first plane wherein said layer of said second metal and said layer of first metal are below said first plane;

forming a first pattern in said layer of first metal and said layer of second metal;

forming a layer of first dielectric on said integrated circuit wafer covering said first pattern formed in said layer of first metal and said layer of second metal, wherein part of said layer of first dielectric is above said first

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plane and part of said layer of first dielectric is below said first plane;

removing that part of said layer of first dielectric above said first plane, thereby planarizing said layer of first dielectric, by means of chemical mechanical polishing until an endpoint is reached wherein said chemical mechanical polishing uses an electric motor powered by an electric current and said endpoint is determined by monitoring said electric current;

cleaning said planarized layer of first dielectric; and

forming a layer of second dielectric on said planarized layer of first dielectric.

13. The method of claim 12 wherein forming said layer of first dielectric comprises the steps of:

forming a layer of first oxide on said integrated circuit wafer covering said first pattern formed in said layer of first metal and said layer of second metal, wherein part of said layer of first oxide is above said first plane and part of said layer of first oxide is below said first plane;

forming a layer of spin on glass on said layer of first oxide, wherein part of said layer of spin on glass is above said first plane and part of said layer of spin on glass is below said first plane;

curing said layer of spin on glass; and



forming a layer of second oxide on said layer of spin on glass, wherein part of said layer of second oxide is above said first plane and part of said layer of second oxide is below said first plane.

14. The method of claim 13 wherein said layer of first oxide has a thickness of between about 500 and 6000 Angstroms and is formed using chemical vapor deposition.

15. The method of claim 13 wherein said layer of spin on glass has a thickness of between about 2000 and 8000 Angstroms.

16. The method of claim 13 wherein said layer of second oxide has a thickness of between about 3000 and 20,000 Angstroms and is formed using plasma assisted chemical vapor deposition.

17. The method of claim 12 wherein said first metal is Aluminum/Silicon/Copper having a thickness of between about 3000 and 10,000 Angstroms.

18. The method of claim 12 wherein said first metal is Aluminum/Copper having a thickness of between about 3000 and 10,000 Angstroms.

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19. The method of claim 12 wherein said second metal is Tungsten having a thickness of between about 200 and 2000 Angstroms.

20. The method of claim 12 wherein said second metal is Tungsten Nitride having a thickness of between about 200 and 2000 Angstroms.

21. The method of claim 12 wherein said second metal is Titanium Nitride having a thickness of between about 200 and 2000 Angstroms.

22. The method of claim 12 wherein said chemical mechanical polishing uses an oxide slurry.

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