

Abstract**SEMICONDUCTOR-INTEGRATED-CIRCUIT SRAM-CELL
ARRAY WITH SINGLE-ENDED CURRENT-SENSING**

Each memory (200) cell in an SRAM array contains an auxiliary reading
5 (MR1) transistor connected across one of the transistors (MP1) in each cell. A row
read line (RRi) controls the ON-OFF condition of this auxiliary reading transistor.
In addition, each cell has two access transistors (MW1,MW2) for connecting the cell
to complementary column bit lines ($B_j, \bar{B}_j$). The ON-OFF condition of both of these
access transistors is controlled by a row write line (RWi). Each cell has two power
10 nodes (N3,N4), one connected to a power source such as VDD and the other
connected to a column detector line (Dj) that terminates in a current sensor. The
state of the memory cell is sensed by this current sensor. In one embodiment, the
power line that brings the voltage VDD to the cells is a column line; in another
embodiment, it is a row line. Thus there are a total of four column lines and two row
15 lines in the one embodiment, and a total of three column lines and three row lines in
the other embodiment.

