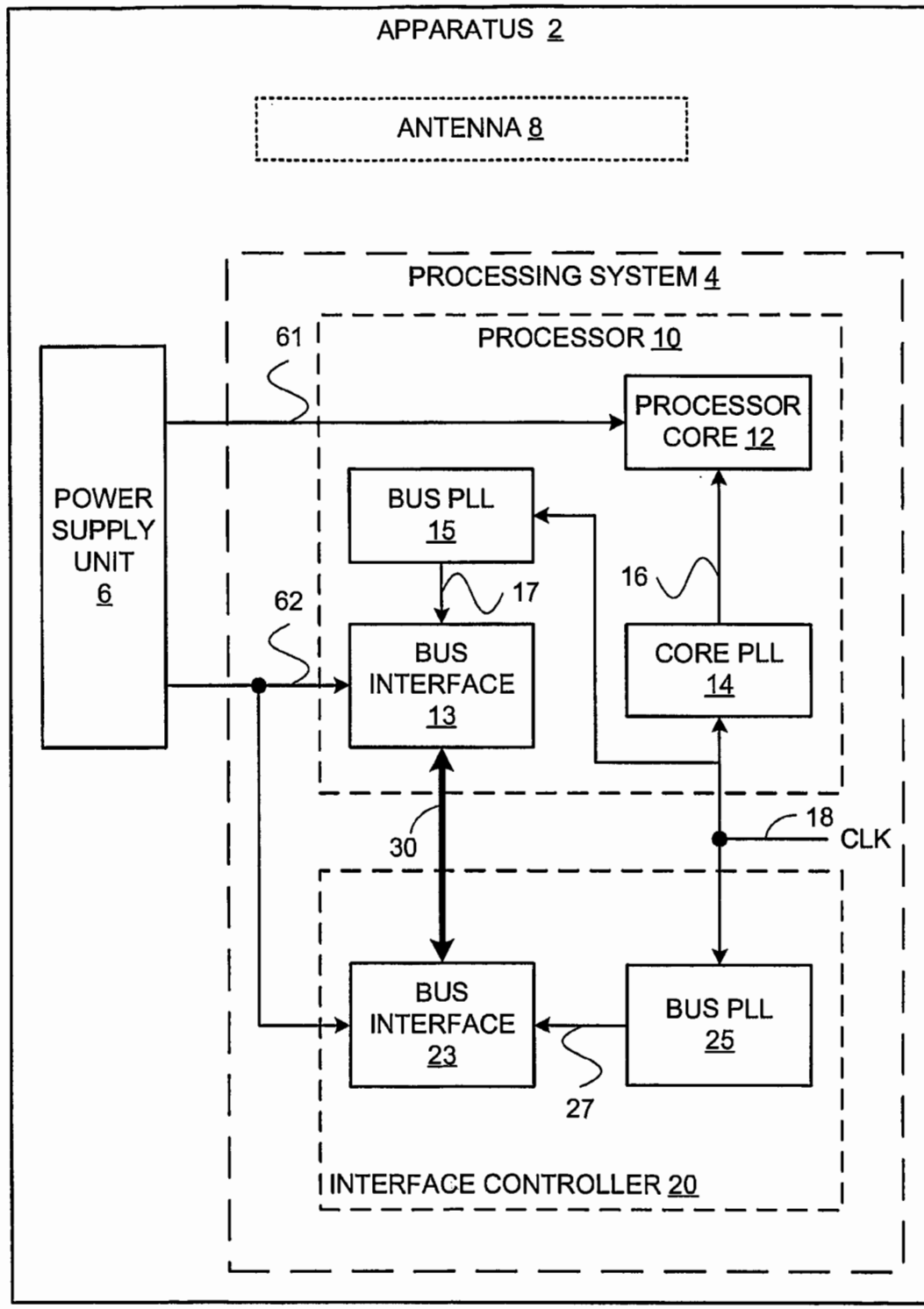

APPARATUS 2
ANTENNA 8
PROCESSING SYSTEM 4
PROCESSOR 10
61
PROCESSOR CORE 12
POWER SUPPLY UNIT 6
BUS PLL 15
16
17
62
BUS INTERFACE 13
CORE PLL 14
18
CLK
30
BUS INTERFACE 23
BUS PLL 25
27
INTERFACE CONTROLLER 20

FIG. 1

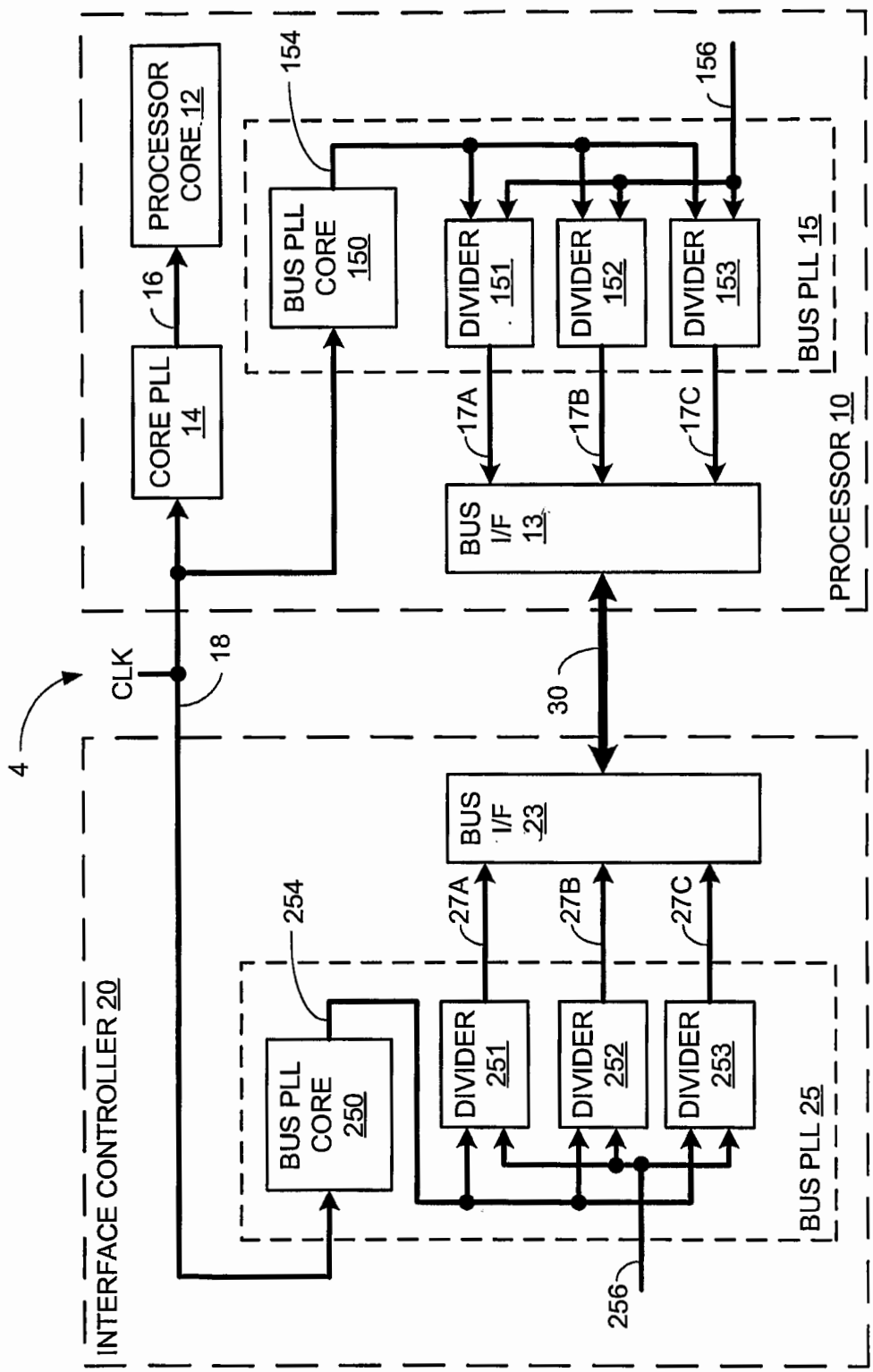

4
INTERFACE CONTROLLER 20
CLK
18
PROCESSOR CORE 12
16
CORE PLL 14
154
BUS PLL CORE 150
DIVIDER 151
DIVIDER 152
DIVIDER 153
156
BUS PLL 15
17A
17B
17C
BUS I/F 13
PROCESSOR 10
30
BUS I/F 23
27A
27B
27C
254
BUS PLL CORE 250
DIVIDER 251
DIVIDER 252
DIVIDER 253
BUS PLL 25
256

FIG. 2

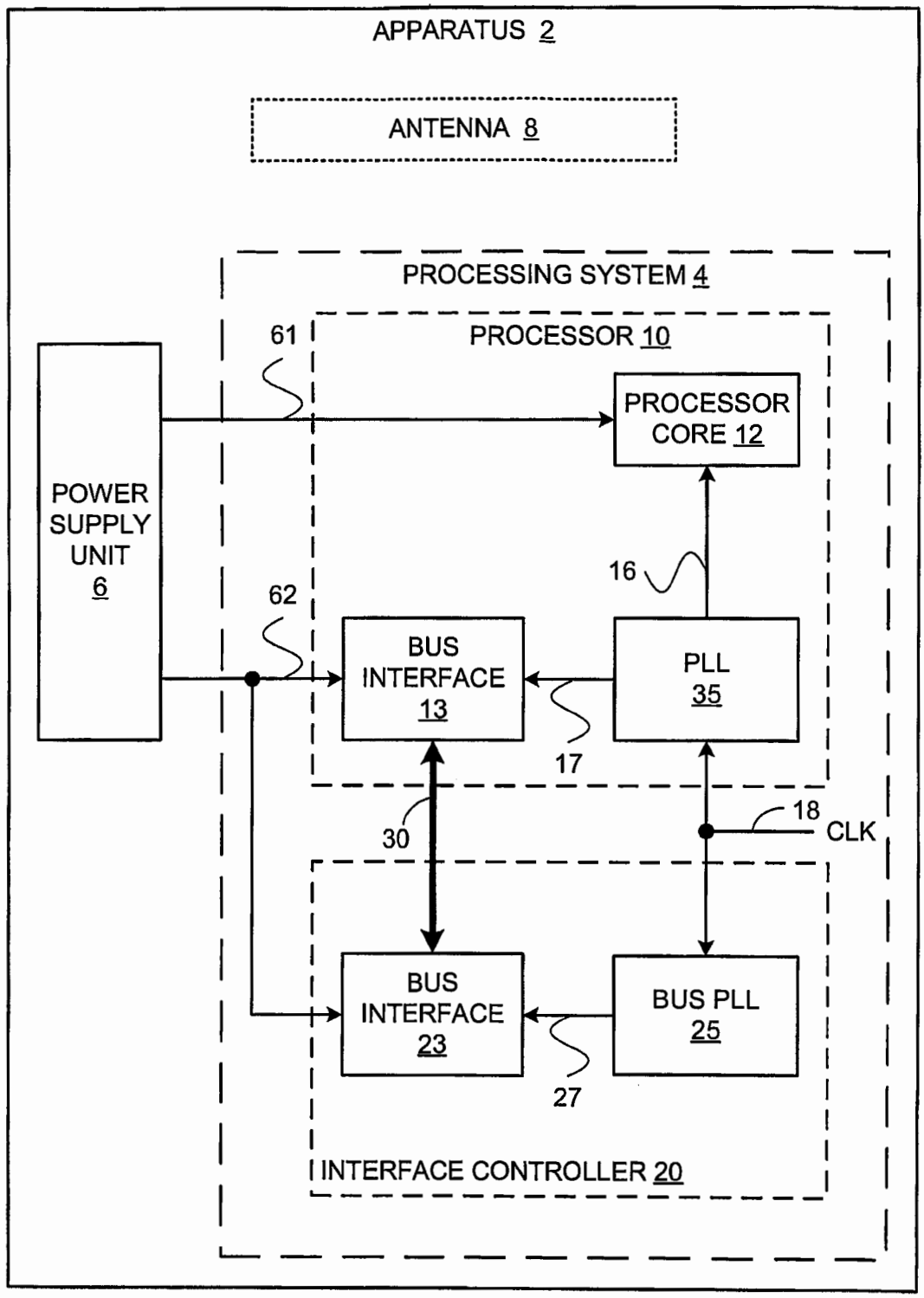

APPARATUS 2
ANTENNA 8
PROCESSING SYSTEM 4
PROCESSOR 10
61
PROCESSOR CORE 12
POWER SUPPLY UNIT 6
16
62
BUS INTERFACE 13
PLL 35
17
18
CLK
30
BUS INTERFACE 23
BUS PLL 25
27
INTERFACE CONTROLLER 20

FIG. 3

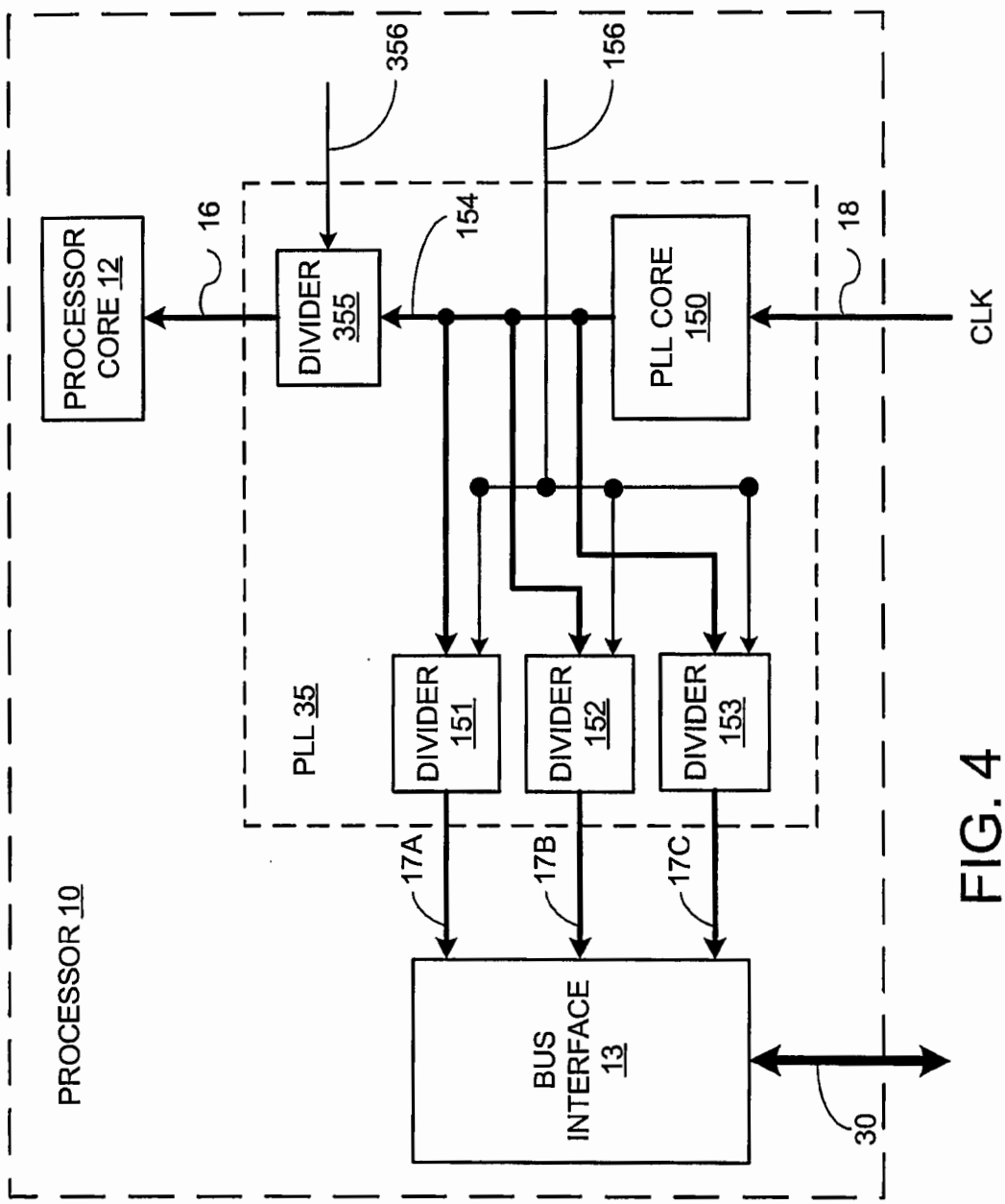

PROCESSOR 10
PROCESSOR CORE 12
16
DIVIDER 355
356
154
156
PLL CORE 150
18
CLK
PLL 35
DIVIDER 151
DIVIDER 152
DIVIDER 153
17A
17B
17C
BUS INTERFACE 13
30

FIG. 4