

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
10 May 2002 (10.05.2002)

PCT

(10) International Publication Number
WO 02/037270 A3

(51) International Patent Classification⁷: **G06F 9/32**, 9/38

Titchester Court, Austin, TX 78729 (US) **OVERKAMP, Gregory, A.**, P.O. Box 163442, Austin, TX 78716 (US)

(21) International Application Number: PCT/US01/46063

(22) International Filing Date: 31 October 2001 (31.10.2001)

(74) Agent: **HARRIS, Scott, C.**, Fish & Richardson P.C., Suite 500, 4350 La Jolla Village Drive, San Diego, CA 92122 (US).

(25) Filing Language: English

(26) Publication Language: English

(81) Designated States (*national*): CN, JP, KR, SG

(30) Priority Data:
09/705,070 2 November 2000 (02.11.2000) US

Published:
— with international search report

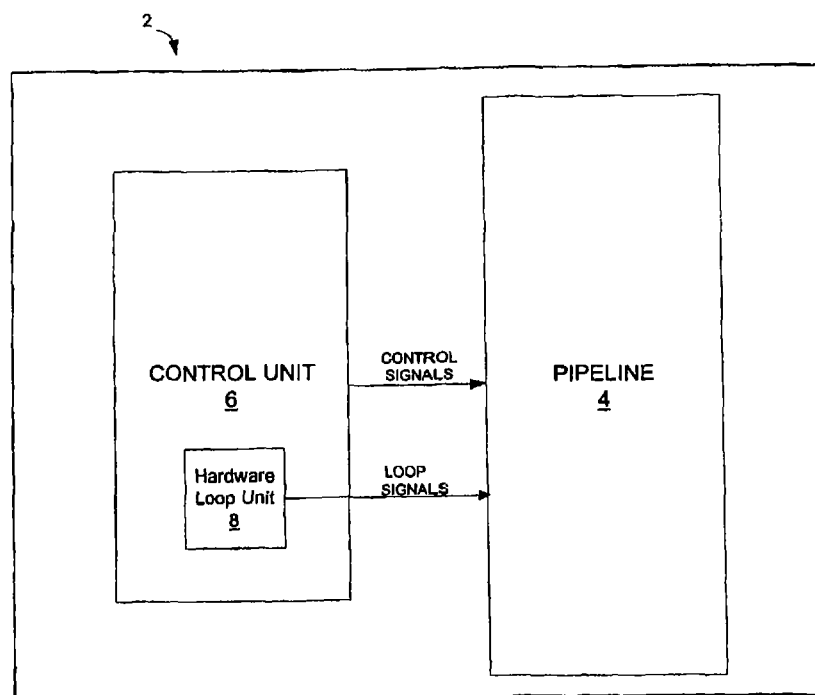
(71) Applicants: **INTEL CORPORATION** [US/US], 2200 Mission College Boulevard, Santa Clara, CA 92122 (US)
ANALOG DEVICES, INC. [US/US], One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106 (US)

(88) Date of publication of the international search report:
17 April 2003

(72) Inventors: **SINGH, Ravi, P.**, 12349 Metric Boulevard, #829, Austin, TX 78758 (US). **ROTH, Charles, P.**, 13305

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette

(54) Title: **HARDWARE LOOPS**



(57) Abstract: In one embodiment, a programmable processor is arranged to include early registers to support hardware loops. In this manner, a system may increase processing speed without significantly increasing power consumption. Loop conditions of a loop may be loaded into a set of early registers. These conditions may then be detected from the early registers before the loop conditions are written to a set of architectural registers.