METHOD FOR FORMING METAL-METAL OXIDE ETCH STOP/ ELECTROMIGRATION BARRIER FOR INTEGRATED CIRCUIT INTERCONNECTS AND DEVICE

FIELD

[0001] An embodiment of the invention relates generally to the field of semiconductor technology and, more specifically, to the formation of interconnects in an integrated circuit.

BACKGROUND

[0002] Conventionally, the formation of metal interconnects within an integrated circuit requires a distinct deposition of an etch-stop layer on top of an ILD/metal interconnect layer before a subsequent level of interconnect is processed. For example, **Figure 1** illustrates a metal interconnect formed according to a conventional technique. Referring to **Figure 1**, an interlayer dielectric (ILD) 102 is deposited on an etch-stop layer 104, typically silicon nitride. A via 106 and trench 107 are patterned into the ILD 102 according to well-known dual damascene techniques. A barrier layer 108 may be formed on the bottom and sidewalls of the via 106 and the trench 107. The via 106 and trench 107 are then filled with an electrically conductive material, such as copper and planarized to the top of the ILD 102, thus forming a copper interconnect 110. An etch-stop layer 112, is deposited over the planarized ILD 102, the planarized barrier layer 108, and the planarized interconnect 110. Consequently, a second ILD 114, second barrier layer 118, and second interconnect 116 may be formed, the second barrier layer 118 and second interconnect 116 connecting to the first

interconnect 110 to provide electrical connection between interconnects 110 and 116. The process may repeat itself for additional ILD/interconnect layers.

[0003] The typical method, however, suffers from problems. For instance, the deposition of the etch-stop layer 112 must be performed before subsequent ILD layers can be formed and patterned. The deposition of the etch-stop layer, however, is time consuming and costly because specialized equipment must be used to deposit a traditional nitride or oxide material. Furthermore, the etch-stop layer 112 is a dielectric material typically formed very thick, usually between 30 to 150 nanometers, which significantly adds to the dielectric value of the circuit. The dielectric value is closely tied to the RC response of the circuit. Therefore, the etch-stop layer 112 significantly increases the overall RC delay of the circuit.

[0004] Additionally, the etch-stop layer 112, typically silicon nitride, does not inhibit interfacial diffusion of metal, such as copper, effectively at the top 120 of the interconnect along the interface between the etch-stop layer 112 and the interconnect material 110. Interfacial diffusion has been identified as the primary cause of premature electromigration failure.

[0005] Some attempts have been made to try and cap the top of the metal interconnect, however these approaches require a very selective process wherein a capping metal can only be deposited onto the metal interconnect, but not onto the ILD. In addition, a separate etch-stop deposition is needed for unlanded via design rules.

BRIEF DESCRIPTION OF THE DRAWINGS

[0 0 0 6] The present invention is illustrated by way of example and should not be limited by the figures of the accompanying drawings in which like references indicate similar elements and in which:

Figure 1 illustrates a typical method of forming interconnects, according to the prior art; and

Figures 2A - 2Q illustrate a method of forming an interconnect, according to one embodiment of the invention.

DETAILED DESCRIPTION

[0 0 0 7] Described herein is a method and apparatus for forming interconnects with a metal-metal oxide electromigration barrier and etch stop. In the following description numerous specific details are set forth. One of ordinary skill in the art, however, will appreciate that these specific details are not necessary to practice embodiments of the invention. While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not restricted to the specific constructions and arrangements shown and described since modifications may occur to those ordinarily skilled in the art. In other instances well-known semiconductor fabrication processes, techniques, materials, equipment, etc., have not been set forth in particular detail in order to not unnecessarily obscure embodiments of the present invention.

[0 0 0 8] A method of forming interconnect layers is described below that does not require a separate etch-stop deposition or selective deposition of a

capping metal. In one embodiment of the invention, a metal layer is deposited with a portion contacting an interlayer dielectric ("ILD") and a portion contacting an electrically conductive interconnect. The portion of the metal layer contacting the ILD reacts with the ILD to form a metal oxide over the ILD. However, the portion of the metal layer contacting the electrically conductive interconnect acts as a metal cap over the electrically conductive interconnect to improve electromigration performance. The metal oxide and metal cap collectively act as an etch-stop layer during the subsequent patterning of an overlying ILD.

[0009] The method begins with an integrated-circuit structure 201, as shown in **Figure 2A**, which includes a substrate 202 supporting a conductor 204 which may be connected to active circuitry and integrated devices within the integrated circuit. The term "substrate" encompasses a semiconductor wafer, such as monocrystalline silicon, as well as structures that have one or more insulative, semi-insulative, conductive, or semiconductive layers and materials. Thus, for example, the term embraces silicon-on-insulator, silicon-on-sapphire, and other advanced structures. The conductor 204 can be a material such as copper, silver, gold, or aluminum, clad in a diffusion barrier 206, such as titanium nitride or tantalum nitride, to prevent the conductor 204 material from diffusing into the substrate 202.

[0010] Atop the integrated-circuit structure 201, as shown in **Figure 2B**, a non-conductive etch-stop layer 208 is deposited, typically from 30 to 150 nanometers thick, comprising a material such as silicon nitride, silicon oxynitride, or nitrogen-doped silicon carbide. The etch-stop layer 208 comprises a material that will work as an effective etch-stop to a subsequent etchant, but in addition may also act as a passivation layer. Upon, the etch-stop layer 208 is formed an

insulative layer 210, sometimes referred to as an interlayer dielectric, or ILD for short. Herein, the insulative layer 208 will therefore be referred to as an ILD. In one embodiment of the invention, the ILD 210 comprises a material having electrically insulative properties but also containing some form of oxygen. Exemplary ILD's containing oxygen include oxide compounds such as silicon dioxide (SiO_2), fluorine-doped silicon oxide (SiOF), or carbon doped oxide (CDO). The presence of oxygen inside the ILD 210 is significant to one embodiment of the invention, as described in further detail in conjunction with **Figure 2I** below.

[0 0 1 1] The ILD 210 may be deposited by any known method for depositing a film of dielectric material, including physical and chemical vapor deposition techniques. The thickness of the ILD 210 may vary depending on the design of the integrated circuit (e.g., 1000 to 15000 Å).

[0 0 1 2] The method may continue, as shown in **Figures 2C- 2D**, with patterning the ILD 210 according to conventional dual-damascene techniques, to etch the ILD 210 to form holes, commonly known as vias. Such techniques may include a typical lithography process, as shown in **Figure 2C**, including depositing a photoresist layer 212 over the ILD 210 then masking, exposing, and developing the photoresist layer 212 to form a pattern 214 in the photoresist layer 212. Then, as shown in **Figure 2D**, the ILD 210 can be etched, according to the pattern 214 in the photoresist layer 212, to first form at least one hole 216, also known as a via, within the ILD 210. The etching may first stop on the etch-stop layer 208. An exemplary method of etching may include reactive ion etching (RIE), or other well-known methods. The photoresist layer 212 can then be removed from atop the ILD 210 and via 217 cleaned.

[0 0 1 3] As shown in **Figure 2E**, a second patterning process may

also be performed, according to conventional dual damascene techniques, to form a trench 220. According to one technique, the second patterning process may include depositing a sacrificial material 218 to fill via 216 completely. The sacrificial material may be a spin-on-polymer (SOP) or spin-on-glass that is deposited by spin coating. The layer may also serve as anti-reflection layer. Another photoresist layer 219 may be deposited on the sacrificial material 218, then the photoresist layer 219 may be masked, exposed, and developed to form another pattern defining a trench formation region. A timed etch, as shown in **Figure 2E**, is then performed until trench 220 is formed to a specified depth according to the designed aspect ratio for the trench 220. The photoresist layer 219 may be subsequently removed, as well as the sacrificial material 218, and the etch-stop layer 208 may then be further etched to connect the via 216 with a portion of the underlying conductor 204. A cleaning process may then be performed to remove any residues.

[0014] A barrier layer 222 may then be deposited on the top of ILD 210 as well as on the sidewalls and bottom of the via 216 and trench 220. In one embodiment of the invention, a seed layer may be deposited on the barrier layer 222 and on the top of the ILD 210. An electroplating process may then be performed to grow a thin layer of an electrically conductive material out of the seed layer in preparation to fill the via 216 and trench 220. The via 216 and trench 220 may then be filled with an electrically conductive material 224, as shown in **Figure 2F**. In one embodiment, the electrically conductive material 224 and the seed layer are copper. The seed layer merges with the electrically conductive material 224. In another embodiment, however, the seed layer may not be present and the electrically conductive material 224 may be deposited

directly onto the barrier layer 222. The barrier layer 222 may be necessary to prevent the electrically conductive material 224 from diffusing into the ILD 210, especially if the ILD 210 is not a material that, itself, prevents diffusion, and especially if the electrically conductive material 224 is highly prone to diffusion. Exemplary materials that may be used for the barrier layer 222 include zirconium, titanium, tantalum, tungsten, titanium nitride, tantalum nitride, tungsten nitride, titanium carbide, tantalum carbide, tungsten carbide, hafnium, or other nitrides, carbides, compounds, or materials that will prevent diffusion of the electrically conductive material 224 into the ILD 210. Exemplary materials for the electrically conductive material 224 include copper, gold, silver, and aluminum. The electrically conductive material 224 should be deposited to a thickness that will completely fill the via 216 and the trench 220.

[0 0 1 5] Next, as shown in **Figure 2G**, a planarization procedure may be performed, such as a chemical mechanical polish, or CMP for short, to planarize the electrically conductive material 224 and the barrier layer 224 with the top of the ILD 210, thus forming an electrically conductive interconnect 224 within the ILD 210, thus completing the formation of the interconnect layer 200.

[0 0 1 6] The planarization procedure exposes upper portions of the ILD 210, the interconnect 224, and the barrier layer 222. In a conventional process, if a second interconnect layer were to be subsequently formed upon the first interconnect layer 200, a conventional etch-stop layer deposition would need to be performed, as was previously performed in the formation of the first interconnect layer 200. However, as shown in **Figure 2H**, to eliminate the need for a conventional etch-stop layer deposition, such as a silicon nitride layer, a metal material 226 is deposited onto the exposed upper portions of the ILD 210,

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the interconnect 224, and the barrier layer 222. The deposition of the metal material 226 is cost effective and time saving since the same machinery used to deposit the barrier/seed layers 222 material can be used to deposit the metal material 224. Additionally, the same machinery can be used at subsequent metallization processes while creating other interconnect layers. Furthermore, since a conventional etch-stop layer is a dielectric material typically formed very thick (e.g., 30 to 150 nanometers), a conventional etch-stop layer typically increases the overall RC delay of an integrated circuit significantly. However, since the need for a conventional etch-stop layer is eliminated according to the embodiment of the invention described, the overall RC delay will decrease significantly due to a thinner metal oxide employed in this invention. Therefore, the method described will also provide an integrated circuit having a decreased RC delay, improving performance of the circuit considerably.

[0 0 1 7] The deposition of the metal material 226 may be done by physical vapor deposition methods (e.g., thermal evaporation, sputtering, etc.), chemical vapor deposition methods (e.g., conventional, plasma enhanced, etc.), or by other known methods of depositing a thin metal film. The metal material 226 should be deposited to a thickness sufficient that the resultant layer, described in further detail below, will act as an effective etch-stop to a subsequent ILD etch. However, the metal material 226 should not be deposited so thick that it will interfere significantly with the dielectric value (K value) of the overall circuit. The K value is directly related to the time constant value (RC value) of the circuit, and consequently, if the metal material 226 is deposited too thickly, it may slow down the circuit's performance. Therefore, in one embodiment of the invention, the metal material 226 is deposited to a thickness above approximately 10Å, with

optimal results between approximately 10 Å to 100Å.

[0 0 1 8] In one embodiment of the invention, the metal material 226 may comprise a material that will automatically react with the exposed upper portion of the ILD 210 as the metal material 226 is being deposited, to form a metal oxide layer 228 over the exposed upper portion of the ILD 210, as shown in **Figure 2I**. If the ILD 210 is an oxide material, or in other words if the ILD 210 has a sufficient amount of oxygen contained therein, when the metal material 226 is deposited onto the ILD 210, the metal material 226 and the oxygen in the ILD 210 will automatically react, thus causing the metal material 226 to oxidize, and form the metal oxide layer 228 on contact. As the metal material 226 and the ILD 210 react, a portion of the ILD 210 may be consumed, thus causing the metal oxide layer 228 to protrude slightly into the ILD 210. Exemplary ILD 210 materials that will react with the metal material 226 upon contact may include oxygen compounds ("oxides"), such as silicon dioxide (SiO_2), fluorine-doped silicon oxide (SiOF), and carbon doped oxide (CDO). Examples of metal materials that may thus react on contact with the exemplary ILD 210 materials include cobalt, aluminum, tantalum, titanium, and chromium. Consequently, the formed metal oxide layer 228 may comprise tantalum oxide, titanium oxide, aluminum oxide, chromium oxide or cobalt oxide.

[0 0 1 9] Additionally, the metal material 226 may comprise a material that will not significantly be oxidized by the exposed upper portion of the interconnect 224 or the barrier layer 222, thus forming a mostly unreacted metal layer 230, or metal cap 230, over the exposed upper portions of the interconnect 224 and the barrier layer 222, also depicted in **Figure 2I**. The metal cap 230 is the same material as the metal material 226. The metal cap 230 and the metal

oxide layer 228 are thus formed simultaneously, and both were formed onto the ILD 210, the interconnect 224 and the barrier layer 222 without a need for selective depositions. It should be noted that either at the interface 231 between the metal layer 230 and the copper interconnect 224, or above the metal cap 230, partial oxidation may also occur due to exposure to the ambient, however such oxidation is minimal and effectively inconsequential to electrical communication between the copper interconnect 224 and subsequently formed interconnects. Care should be taken, however, to ensure that as little oxidation occurs as possible at the interface 231 since the oxidation cannot be removed feasibly after the metal cap 230 has been formed.

[0 0 2 0] The metal cap 230 is configured to provide electrical connection between the first interconnect and subsequent interconnects formed above it. The metal cap 230 will inhibit diffusion of the interconnect 224 material along the metal cap/interconnect interface due to better adhesion strength compared to that in a conventional etch-stop/interconnect interface. In other words, the metal cap 230 causes an increase in the activation energy of electromigration along the interface, thus significantly preventing electromigration at the interface, reducing void formation caused by migrating material, thus improving the overall performance of the circuit.

[0 0 2 1] Additionally, the metal cap 230 is advantageous for unlanded via designs wherein a portion of an overlaying ILD is directly above the interconnect. Hence, the metal cap 230 acts as a diffusion barrier that caps the top of the interconnect 224 material from outward diffusion into the surrounding ILD 210 along the edges 231 of the interface between the metal cap 230 and the metal interconnect 224 and also prevents upward diffusion into a subsequently

formed overlaying ILD. Additionally, as described in further detail below in conjunction with **Figure 2M**, the metal cap 230 and the metal oxide 228 act as an etch-stop layer preventing subsequent etch, ash, and clean processes from damaging the ILD material 210, the metal interconnect 224, or the barrier layer 222.

[0 0 2 2] Furthermore, since the metal cap 230 is configured to provide electrical connection between the first interconnect and subsequent interconnects formed above it, the metal material 226 should not be too electrically resistive a material. If too resistive, the metal cap 230 may not be able to provide good electrical conductivity between the first interconnect 224 and subsequently formed interconnects that may be contacting the metal cap 230. Furthermore, the metal material 226 of the metal cap 230 should not be too prone to diffusion into the interconnect 224 material. If too prone to diffusion into the interconnect 224 material, then in time the metal material 226 would pervade the interconnect 224 producing an undesirable increase in the resistivity of the interconnect 224. An increased resistivity would increase the RC value of the interconnect 224 eventually causing diminished performance of the circuit.

[0 0 2 3] Consequently, the metal cap 230 helps to significantly improve electromigration problems in an integrated circuit, thus improving overall circuit reliability. Plus, because the metal cap 230 was formed at the same time as the oxide layer 228, the method is especially advantageous since the subsequent formation of an additional interconnect layer does not require a etch-stop layer deposition separate from the metal cap 230 deposition.

[0 0 2 4] After the metal material 226 has been deposited, and the ILD 210 has reacted with the metal material 226, a portion 232 of metal material 226

above the ILD 210 may not have fully reacted with the ILD 210. This portion 232 is superfluous and undesirable because it would short out the entire circuit if permitted to remain. Therefore, as shown if **Figure 2J**, an etch-back may be performed to remove the superfluous portion 232 above the metal oxide layer 228. During such an etch-back process, the etchant should have a chemistry that etches the metal material 226 but does not significantly etch the metal oxide 228, the ILD 210, the interconnect 224, or the barrier layer 222. A standard fluorine based plasma etch may be employed for Ta, while A standard chlorine based plasma etch may be employed for Al and Ti. Furthermore, the etch should not be performed too long or else the metal cap 230 may become etched excessively. Consequently, the etch-back process should be timed to be only as long as necessary to etch the superfluous portion 232 down to the top of the metal oxide layer 228. As shown in Figure 2J, the metal cap 230 is substantially planar with the metal oxide layer 228, but does not necessarily need to be planar.

[0 0 2 5] The resultant metal oxide layer 228 and metal cap 230 together define a protective layer 234 that can act as an etch-stop to a subsequent ILD patterning and etch. Consequently, as shown in **Figures 2K-2M**, the method may continue with depositing a second ILD 236 on the protective layer 234, then patterning and etching a via 242 in the second ILD 236, with the protective layer 234 acting as an etch-stop during the via etch.

[0 0 2 6] In one embodiment of the invention, as shown in **Figure 2K**, the second ILD 236 may be deposited by any known method for depositing a film of dielectric material, including physical and chemical vapor deposition techniques. The second ILD 236 thickness may vary depending on the design of the integrated circuit, but in one embodiment is deposited to a thickness of

approximately 6000 Å. The second ILD 236 may comprise the same oxide material as the first ILD 210, such as silicon dioxide (SiO_2), fluorine-doped silicon oxide (SiOF), or carbon doped oxide (CDO), or may be a different material from the first ILD 210. If subsequent ILD are to be formed atop the second ILD 236, however, it may be advantageous for the second ILD 236 to be the same material as the first ILD 210.

[0 0 2 7] Patterning of the via 242 may include a lithography process, as shown in **Figure 2L**, including depositing a photoresist layer 238 over the second ILD 236 then masking, exposing, and developing the photoresist layer 238 to form a pattern 240 in the photoresist layer. Then, as shown in **Figure 2M**, the second ILD 236 can be etched, according to the pattern 240 in the photoresist layer 238. An exemplary method of etching may include reactive ion etching (RIE), or other well-known methods. During the etch, if not for the protective layer 234, the underlying ILD 210, interconnect 224 and barrier layer 222 would be attacked and damaged by the etchant 244. Ashing and cleaning may then be performed to remove the photoresist layer 238 and to clean residues from the inside of the via 242. The protective layer 234 also protects the underlying ILD 210, interconnect and barrier layer 222 during the ashing and cleaning processes.

[0 0 2 8] According to one embodiment of the invention, the via 242 may be formed according to an unlanded design, or in other words may be formed so that part of via 242 may overlay the metal oxide layer 228 and another part may overlay the metal cap 230, such as the embodiment depicted in **Figure 2M**. Therefore, the etchant 244 used during the etching of the second ILD 236 should include a chemistry that etches the material of the second ILD 236 but does not significantly etch the metal oxide layer 228 or the metal cap 230.

[0 0 2 9] The method may then continue, as shown in **Figure 2N**, with performing a second patterning process, according to conventional dual damascene techniques, to form a trench 248. According to one technique, after removing the photoresist layer 238 from atop the second ILD 236, the second patterning process may include depositing a sacrificial material 245, depositing another photoresist layer 246 over the sacrificial material 245, then masking, exposing, and developing the photoresist 246 to form an pattern defining a trench formation region. A timed etch, as shown in **Figure 2N**, is then performed until trench 248 is formed to a specified depth according to the designed aspect ratio for the trench 248. The photoresist layer 246 and any remaining sacrificial material 245, may be subsequently removed via ashing and cleaning processes.

[0 0 3 0] The method may further continue, as shown in **Figures 2O – 2P** with forming a second interconnect 254 in the second ILD 236 to form a second interconnect layer 256. As shown in **Figure 2O**, a barrier layer 250 may be deposited on top of the second ILD 236 and on the sidewalls of the etched via 242 and trench 248 to prevent lateral diffusion of the subsequently formed interconnect into the second ILD 236. A seed layer may be deposited on the barrier layer 250 and an electroplating process may be performed. An electrically conductive material 252, such as copper, is deposited to a thickness sufficient to completely fill the via 242 and trench 248. Then, as shown in **Figure 2P**, a planarization procedure may be performed, such as a CMP, to planarize the electrically conductive material 252 and barrier layer 250 with the top of the second ILD 236, to form a second interconnect 254. Hence, a second interconnect layer 256 is formed above the first interconnect layer 200 utilizing a metal-metal oxide etch-stop layer/electromigration barrier, and thus avoiding a

separate, conventional etch-stop layer deposition. The second ILD 236 is protected from interconnect electromigration by the metal cap 230. Then, as shown in **Figure 2Q**, the method may repeat for the formation a subsequent interconnect layer 258, and so on.

[0031] Several embodiments of the invention have thus been described. However, those skilled in the art will recognize that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims that follow.

CLAIMS

1. A method, comprising:

forming a metal oxide layer over an interconnect layer by depositing a metal layer on an exposed portion of a first interlayer dielectric (ILD) and on an exposed portion of an interconnect formed within the first ILD, the metal oxide layer comprising a reaction product of the first ILD and the deposited metal layer; and
depositing a second ILD on the metal oxide layer.

2. The method of claim 1, wherein the first ILD is a material that includes an amount of oxygen sufficient to react with the metal layer as the metal layer is being deposited to form the metal oxide layer.

3. The method of claim 1, further comprising:
etching a via in the second ILD, the metal oxide layer acting as an etch-stop.

4. The method of claim 3, wherein etching the via includes utilizing an etchant that will etch the second ILD without significantly etching the metal oxide layer.

5. The method of claim 1, wherein depositing the metal layer includes depositing the metal layer to a thickness between approximately 10 Å to 100 Å.

6. The method of claim 1, wherein the first interconnect comprises copper.

7. The method of claim 1, wherein the metal layer comprises a material selected from the group consisting of cobalt, aluminum, tantalum, chromium, and titanium.

8. A method, comprising:
depositing a first ILD over a substrate;
forming a first via and a first trench in the first ILD;
filling the first via and the first trench with an electrically conductive material;
planarizing the electrically conductive material equivalent to a top surface of the first

ILD, thus forming a first interconnect within the first ILD, the interconnect have an exposed top portion and the first ILD having an exposed top portion;
depositing a metal on the exposed top portion of the first ILD and on the exposed top portion of the interconnect, the metal being a material that reacts on contact with the first ILD to form a metal oxide on the first ILD, and the metal being a material that forms an electromigration barrier over the first interconnect; and
depositing a second DLD on the metal oxide and the electromigration barrier.

9. The method of claim 8, wherein the metal oxide and the electromigration barrier together define a protective layer over the first ILD and first interconnect, and further comprising:
etching and cleaning a second via and second trench in the second ILD, the protective layer acting as an etch-stop during etching and cleaning.

10. The method of claim 9, further comprising:
forming a second interconnect within the second via and trench, the electromigration barrier to prevent the first interconnect from diffusing into any one of the first ILD and the second ILD.

11. The method of claim 9, wherein etching the second via includes utilizing an etchant that will etch the second ILD without significantly etching the protective layer.

12. The method of claim 8, wherein the metal does not completely react with the first ILD, thus producing a superfluous metal layer above the metal oxide, and further comprising etching back the superfluous metal layer to the top of the metal oxide.

13. The method of claim 8, wherein depositing the metal includes depositing the metal to a thickness between approximately 10 Å to 100 Å.

14. The method of claim 8, wherein the first interconnect comprises copper.

15. The method of claim 8, wherein the metal comprises a material selected from the group consisting of cobalt, aluminum, tantalum, chromium, and titanium.

16. The method of claim 8, wherein the first ILD comprises a material selected from the group consisting of SiO_2, SiOF, and CDO.

17. A method comprising:
forming a first ILD;
forming a first via and trench in the first ILD;
filling the first via and the trench with an electrically conductive material;
planarizing the electrically conductive material equivalent to a top surface of the first ILD, thus forming an interconnect within the first ILD, the interconnect having an exposed top portion and the first ILD having an exposed top portion;
simultaneously forming a metal oxide layer on the exposed top portion of the first ILD and a metal cap over the exposed top portion of the interconnect;
forming a second ILD on the metal oxide layer and over the metal cap; and
etching the second ILD until at least a portion of the metal cap is exposed.

18. The method of claim 17, wherein etching the second ILD until at least a portion of the metal cap is exposed exposes at least a portion of the metal oxide layer.

19. The method of claim 17, wherein simultaneously forming the metal oxide layer and the metal cap comprises:
depositing a metal on the exposed top portion of the first ILD and the exposed top portion of the interconnect, at least a portion of the metal consuming a part of the first ILD to form the metal oxide layer.

20. The method of claim 19, further comprising, prior to forming the second ILD on the metal oxide layer:
etching superfluous metal on the metal oxide layer to expose the metal oxide layer.