STRUCTURE FOR RADIO-FREQUENCY APPLICATIONS

FIELD OF THE INVENTION

The present invention relates to the field of integrated radiofrequency devices.

TECHNOLOGICAL BACKGROUND OF THE INVENTION

Integrated devices are usually created on substrates in the form of wafers which are used mainly as support for the fabrication thereof. However, the increasing degree of integration and the increasing performance levels expected of these devices is driving an increasingly significant coupling between their performance levels and the characteristics of the substrate on which they are formed. That is particularly the case with radiofrequency (RF) devices, processing signals with a frequency of between approximately 3 kHz and 300 GHz, the applications of which notably fall within the field of telecommunications (cellular telephony, Wi-Fi, Bluetooth, etc.).

As an example of device/substrate coupling, the electromagnetic fields, deriving from the high-frequency signals propagating in the devices, penetrate into the depth of the substrate and interact with any charge carriers located therein. This causes problems of nonlinear distortion (harmonics) of the signal, a pointless consumption of a portion of the energy of the signal by insertion loss and possible influences between components.

Thus, the RF devices have characteristics governed both by their architecture and their creation processes, and by the capacity of the substrate on which they are fabricated to limit the insertion losses, the

crosstalks between neighboring devices, and the nonlinear distortion phenomena generating harmonics.

The radiofrequency devices, such as antenna switches and tuners and power amplifiers, can be created on different types of substrates.

Silicon on sapphire substrates are for example known, commonly called SOS (silicon on sapphire), which give the components, created according to microelectronic technologies in the surface layer of silicon, the benefit of the insulating properties of the sapphire substrate. For example, the antenna switches and power amplifiers fabricated on this type of substrate exhibit very good figures of merit but are primarily used for niche applications because of the overall cost of the solution.

Also known are the substrates based on high-resistivity silicon comprising a support substrate, a trapping layer arranged on the support substrate, a dielectric layer arranged on the trapping layer, and an active semiconductive layer arranged on the dielectric layer. The support substrate usually exhibits a resistivity higher than 1 kohm.cm. The trapping layer can comprise non-doped polycrystalline silicon. The combination of a high-resistivity support substrate and of a trapping layer according to the prior art makes it possible to reduce the abovementioned device/substrate coupling and thus ensure good performance levels in the RF devices. In this respect, a person skilled in the art will find a review of the performance levels of the RF devices fabricated on the high-resistivity semiconductive substrate known from the prior art in "Silicon-on-insulator (SOI) Technology, manufacture and applications", points 10.7 and 10.8, Oleg Kononchuk and Bich-Yen Nguyen, from Woodhead Publishing.

Nevertheless, a trapping layer of polysilicon presents the drawback of undergoing a partial recrystallization in high-temperature heat treatment steps, which contributes to diminishing the trap density in the layer. With the trend in mobile telephony standards dictating increasingly demanding specifications in the RF components, the degradation of the performance of the device linked to this decrease in trap density is prohibitive for some applications.

Moreover, the step of deposition of the polysilicon and of surface preparation in order to produce the stacking of the substrate are sensitive and expensive.

An alternative to this trapping layer of polysilicon is a layer of porous silicon. A deposition of a porous layer, according to the prior art, does not make it possible to obtain a very thin layer thickness, less than 1 μm. Thus, the porous layers of the prior art and their thickness, between 10 μm and 80 μm, do not make it possible to obtain a substrate comprising a porous layer with a mechanical strength that is sufficient to withstand certain steps of fabrication of the devices and be retained in the final functional devices.

OBJECT OF THE INVENTION

An object of the invention is therefore to propose a structure suitable for radiofrequency applications, remedying the drawbacks of the prior art. An object of the invention is notably to propose an integrated structure that meets the increasing demands of the RF applications and that allows for a reduction in fabrication costs.

BRIEF DESCRIPTION OF THE INVENTION

An aspect of the invention relates to a structure for radiofrequency applications comprising:

a support substrate of high-resistivity silicon comprising a non-doped lower part and a p-type doped upper part, the p-typed doped upper part formed to a depth D of less than 1 µm in the support substrate; and

a mesoporous trapping layer of silicon formed in the p-type doped upper part of the support substrate, the mesoporous trapping layer having a porosity rate of between 20% and 60% such that the mesoporous trapping layer traps inversion charges susceptible to be generated in the non-doped lower part and the non-doped lower part retains a high and stable resistivity level.

The porosity rate of the trapping layer thus obtained makes it possible to accurately control its resistivity, at levels that can be high (> 5000 ohm.cm). Thus, the setting of the porosity rate (according to a precise range from 20% to 60%) and of the depth D (less than 1 µm) of the doping of the upper part of the support substrate of silicon in which the trapping layer will be formed, make it possible:

- to ensure a good mechanical strength of the mesoporous layer, allowing it to be retained in the final functional device;
- and to confer properties of resistivity and of insulation on the structure that are appropriate for radiofrequency applications.

Moreover, the fabrication of a very thin mesoporous trapping layer (less than 1 µm) simplifies the step of deposition of the trapping layer on the support substrate, as well as the potential steps of surface preparation necessary for the subsequent process steps to be carried out.

According to advantageous features of the invention, taken alone or in combination:

- the mesoporous trapping layer has pores with a diameter of between 2 nm and 50 nm;
- the mesoporous trapping layer is obtained by a process of electrolysis of the doped upper part of the support substrate;
- the electrolysis process is controlled by a technique of voltage control at the terminals of the electrolysis;
- the resistivity of the lower part of the support substrate is greater than 1000 ohm.cm.

According to other advantageous features of the invention, taken alone or in combination:

- an active layer is arranged on the trapping layer;
- the active layer is transferred onto the trapping layer by direct bonding;
- the active layer is formed from a semiconductive material;
- the active layer is formed from a piezoelectric material;
- the active layer comprises at least one of the materials selected from the following group: silicon, silicon carbide, silicon germanium, lithium niobate, lithium tantalate, quartz, aluminum nitride;
- the thickness of the active layer is between 10 nm and 50 μm;
- a dielectric layer is arranged between the trapping layer and the active layer;
- the dielectric layer is transferred onto the trapping layer by direct bonding;
- the dielectric layer comprises at least one of the materials selected from the following group: silicon dioxide, silicon nitride, aluminum oxide;
- the dielectric layer is between 10 nm and 6 μm;
- a layer of silicon nitride (SiN) is arranged between the trapping layer and the dielectric layer.

According to other advantageous features of the invention, taken alone or in combination, at least one microelectronic device is present on or in the active layer:

- the microelectronic device is a switching circuit or an antenna tuning circuit or a radiofrequency power amplification circuit;
- the microelectronic device comprises a plurality of active components and a plurality of passive components;
- the microelectronic device comprises at least one control element and one MEMS switching element consisting of a microswitch with ohmic contact or of a capacitive microswitch;
- the microelectronic device is a radiofrequency filter operating by bulk or surface acoustic wave propagation.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will emerge from the following detailed description of the invention with reference to the attached figures in which:

- figure 1 represents the dependency of the Young's modulus with the porosity of the silicon;
- figure 2 represents a first embodiment of the invention;
- figures 3a and 3b represent a second embodiment of the invention;
- figure 4 represents another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The structure 1, 1', 11 for radiofrequency applications according to the invention comprises a support

substrate 2 of high-resistivity (HR) silicon. High resistivity should be understood to mean a resistivity higher than 1000 ohm.cm; it is advantageously between 4000 and 10 000 ohm.cm.

The support substrate 2 of HR silicon undergoes a p-type doping on an upper part 3 and to a predetermined depth D, less than 1 μm, in accordance with the invention. This doping can advantageously be performed by ion implantation followed by a bake of RTA type to activate the implanted p-type dopants, or an epitaxy of a p+ layer, or even a doping by "spin on glass" (term describing a deposition of a layer of glass by centrifugation).

Thus doped, the upper layer 3 of the support substrate 2 of HR silicon is subjected to a process of electrolysis, so as to transform the upper part 3 of the support substrate 2 into a porous layer 4, which will form the trapping layer 4. The depth D of the dopants introduced previously into the upper part 3 of the support substrate 2 corresponds substantially to the thickness of the trapping layer 4.

The process of electrolysis can consist for example of an electrochemical anodization, in which at least the upper part 3 of the support substrate 2 is placed in a chamber comprising an electrolyte, such as hydrofluoric acid. An anode and a cathode are then dipped into the electrolyte and powered by a source of electrical current.

There are three types of morphologies for porous silicon:

- macroporous silicon, generally obtained from weakly doped n-type silicon, and having a pore diameter greater than 50 nm;

- mesoporous silicon, generally obtained from strongly doped p-type silicon, and having a pore diameter of between 2 nm and 50 nm;
- nanoporous (also called microporous) silicon, generally obtained from weakly doped p-type silicon, and having a pore diameter of less than 2 nm.

Thus, depending on the level of doping of the substrate 2 and the conditions of the electrolysis process, such as the adjustment of the electrical current density applied by the source of electrical current, the porosity rate will be higher or lower and controlled. To recap, the porosity Po of a layer is defined as the fraction of bulk unoccupied within the layer and is expressed as:

$$Po = (d - d_{Po}) / d$$

where d is the density of the non-porous material and d_{Po} is the density of the porous material.

The trapping layer 4 generated has to have a porosity rate that is sufficient to obtain a high defect density, suitable for trapping the inversion charges generated in the support substrate 2, and a high resistivity level. However, this porosity rate, coupled with the thickness of the porous layer 4, also characterizes the mechanical strength of the trapping layer 4. The dependency of the Young's modulus (denoted E and expressed in GigaPascal) as a function of the porosity rate of the porous layer is represented in figure 1. For a given thickness, the greater the porosity rate, the lower the mechanical properties: the decrease in the Young's modulus as a function of the porosity percentage (Po) reflects this decrease in mechanical strength. Furthermore, for a given porosity rate, the thicker the porous layer, the lower the

mechanical properties. The applicant has identified a process window for which the porous layer exhibits the mechanical strength required to be compatible with subsequent microelectronic steps (deposition, bakes, polishing, etc.), as well as the resistivity properties required for the radiofrequency applications.

The structure 1, 1', 11 according to the invention therefore proposes a trapping layer 4 with a porosity rate that is between 20% and 60% and with a thickness that is less than 1 μm, so as to ensure mechanical and electrical performance levels of the structure 1, 1', 11. The mesoporous morphology, having pores with a diameter of between 2 nm and 50 nm, makes it possible to achieve the requisite porosity levels, over the thickness of 1 μm, with a significant trap density (typically greater than $10^{13}/cm^2$, making it possible to trap the inversion charges) and a high resistivity.

The thickness D of the trapping layer 4 (of mesoporous silicon) depends on the depth of the p-type doping of the upper part 3 of the support substrate 2. The porosity rate depends on the quantity of dopants introduced into the upper part 3 of the support substrate 2 as well as the electrolysis process performance conditions.

In order to ensure that the porosification by electrolysis of the upper part 3 of the support substrate 2 does not exceed the predetermined depth D, a control of the voltage at the terminals of the electrolysis is put in place, making it possible to determine when the porosification begins in the non-doped lower part of the support substrate 2 of HR silicon, and therefore stop the electrolysis process. The porosification of the upper part 3 of the support substrate 2 has to be stopped at the end of the

diffusion tail of the dopants introduced into the upper part 3 of the substrate 2, substantially at the depth D.

The structure 1, 1', 11 for radiofrequency applications according to the invention thus comprises a trapping layer 4 of mesoporous silicon, the porosity of which is between 20 and 60% and the thickness of which is less than 1 μm, arranged on a support substrate 2 of high-resistivity silicon. The trapping layer has a typical resistivity greater than 5000 ohm.cm.

According to a first embodiment of the invention represented in figure 2, the structure 1 for radiofrequency applications can take the form of a wafer of dimensions compatible with microelectronic processes, for example with a diameter of 200 nm or 300 nm, comprising the support substrate 2 and the trapping layer 4 (figure 2c).

The support substrate 2 of HR silicon (figure 2a) advantageously has a resistivity greater than 4000 ohm.cm. It first of all undergoes a boron ion implantation, for example, with a dose of $1^e13/cm^2$ and with an energy of 50 keV, followed by a heat treatment at 1000°C for 5 minutes; a p-doped upper part 3, to a depth of approximately 200 nm, is thus created (figure 2b). The support substrate 2 then undergoes an electrolysis: the current density will for example be between 10 and 20 mA/cm^2 and the electrolysis solution will have an HF concentration of between 10 and 30%. The mesoporous trapping layer 4 of silicon is formed, in the doped upper part 3 of the support substrate 2 (figure 2c). The porosity obtained, dependent on the quantity of dopants and on the current density applied during the electrolysis, is of the order of 50%; the pores have a size of between 2 and 50 nm. This

fabrication process, simple and inexpensive, makes it possible to obtain a structure 1 that exhibits mechanical and electrical properties compatible with the specifications of radiofrequency applications:

- a good mechanical strength making it possible to withstand the various stressful steps of creation of microelectronic components;
- stable insulation properties linked to the high resistivity of the support substrate 2 and to the charge trapping qualities of the mesoporous trapping layer 4, even after application of the high-temperature heat treatments for the creation of microelectronic components.

A second embodiment of the invention is represented in figure 3. According to a first variant of this second embodiment, illustrated in figure 3a, the structure 1' for radiofrequency applications can take the form of a wafer and further comprise an active layer 5, arranged on the trapping layer 4, in and on which RF components will be able to be created. The active layer 5 will advantageously be able to consist of semiconductive materials and/or piezoelectric materials. Advantageously, but without this being limiting, the active layer 5 comprises at least one of the materials out of: silicon, silicon carbide, germanium silicon, lithium niobate, lithium tantalate, quartz, aluminum nitride, etc. The thickness of the active layer 5 can vary from a few nanometers (for example 10 nm) to several tens of microns (for example 50 μm) depending on the components to be fabricated.

By way of example, the active layer 5 is transferred onto the support substrate 2 comprising the trapping layer 4, by one of the thin layer transfer processes well known to those skilled in the art, including:

- The Smart Cut™ process, based on an implantation of

light hydrogen and/or helium ions in a donor substrate and a bonding, for example by molecular adhesion, of this donor substrate directly onto the trapping layer 4, itself arranged on the support substrate 2; a detachment step then makes it possible to separate a thin surface layer from the donor substrate (the active layer), at the level of the embrittlement plane defined by the depth of implantation of the ions. Finishing steps, that can include high-temperature heat treatments, finally confer the crystalline and surface quality required of the active layer 5. The process is particularly suited to the fabrication of thin active layers, with a thickness of between a few nanometers and approximately 1.5 μm for example for layers of silicon.

- The Smart Cut process followed by an epitaxy step, making it possible in particular to obtain thicker active layers, for example from a few tens of nm to 20 μm.
- The direct bonding and mechanical, chemical and/or mechanical-chemical thinning processes; they consist in assembling a donor substrate by molecular adhesion directly on the trapping layer 4, itself arranged on the support substrate 2, then in thinning the donor substrate to the desired thickness of active layer 5, for example by grinding and by polishing (CMP, "chemical mechanical polishing"). These processes are particularly suited to the transfer of thick layers, for example from a few microns to several tens of microns, and up to a few hundreds of microns.

According to another variant of the second embodiment, represented in figure 3b, the structure 1' for radiofrequency applications will also be able to include a dielectric layer 6, arranged between the active layer 5 and the trapping layer 4.

Advantageously, but without this being limiting, the dielectric layer 6 will comprise at least one of the materials out of: silicon dioxide, silicon nitride, aluminum oxide, etc. Its thickness will be able to vary between 10 nm and 3 μm.

The dielectric layer 6 is obtained by thermal oxidation or by LPCVD or PECVD or HDP deposition, on the trapping layer 4 or on the donor substrate prior to the transfer of the active layer 5 onto the trapping layer 4.

As is well known in the field of SOI (silicon on insulator) substrates for radiofrequency applications, such a dielectric layer, for example formed by an oxide of silicon on a support substrate of silicon, comprises positive charges. These charges are compensated by negative charges coming from the support substrate, at the interface with the dielectric layer. These charges generate a conduction layer in the support substrate, under the dielectric layer, with a resistivity that drops around 10-100 ohm.cm. The electrical performance levels sensitive to the resistivity of the support substrate (such as the linearity of the signal, the level of insertion losses, the quality factors of the passive components, etc.) are therefore greatly degraded by the presence of this conduction layer.

The role of the trapping layer 4 is then to trap all the mobile charges generated in the support substrate 2 in order for it to retain a high and stable resistivity level.

Figure 4 presents a third embodiment according to the invention. According to a first variant of this third embodiment, represented in figure 4a, the structure 11 for radiofrequency applications can also comprise or consist of a microelectronic device 7 on or in the

active layer 5, which is arranged on a dielectric layer 6 or directly on the trapping layer 4. The microelectronic device 7 can be a switching circuit (called switch) or an antenna tuning or synchronization circuit (called tuner) or even a power amplification circuit (called power amplifier), created according to silicon microelectronic technologies. The active layer 5 of silicon typically has a thickness of between 50 nm and 180 nm, for example 145 nm, and the underlying dielectric layer 6 has a thickness of between 50 nm and 400 nm, for example 200 nm; the trapping layer 4 is arranged between the dielectric layer 6 and the support substrate 2. The microelectronic device 7 created in and on the active layer 5 comprises a plurality of active components (MOS or bipolar type, or the like) and a plurality of passive components (of capacitor, inductor, resistor, resonator, filter type, or the like).

The fabrication of the microelectronic components entails carrying out several steps including high-temperature heat treatments, typically at 950-1100°C, or even higher. The trapping layer 4 of mesoporous silicon described previously retains its physical and electrical properties after such heat treatments.

According to another variant of this embodiment, represented in figure 4b, the microelectronic device 7 can first of all be created on a substrate of SOI (silicon on insulator) type, then transferred by a layer transfer technique known to those skilled in the art onto a structure 1 according to the invention comprising the trapping layer 4 arranged on the support substrate 2.

In this particular case, the structure 11 comprises, on the one hand, the support substrate 2 on which the

trapping layer 4 is arranged; above the latter, there is the layer of components of the microelectronic device 7: the so-called "back end" part of metal interconnect and dielectric layers is arranged above the trapping layer 4, the so-called "front end" part (silicon), generated partly in the active layer 5, being itself above the "back end" part. Finally, above, there is the active layer 5 and, optionally, a dielectric layer 6'.

In these two particular cases, the electromagnetic fields, deriving from the high-frequency signals intended to be propagated in the devices 7, and which will penetrate into the trapping layer 4 and into the support substrate 2, will undergo only low losses (insertion losses) and disturbances (crosstalk, harmonics), because of the high and stable resistivity of the support substrate 2 and of the trapping layer 4. Advantageously, the structure 11 according to the invention benefits from a process of fabrication of the trapping layer 4 that is simple and economical compared to the prior art; and it offers at least equivalent performance levels.

According to a fourth embodiment, the structure 11 for radiofrequency applications can comprise or consist of a microelectronic device 7 comprising at least one control element and one MEMS (microelectromechanical system) switching element consisting of a microswitch with ohmic contact or of a capacitive microswitch.

The MEMS fabrication can be facilitated by the presence of a dielectric layer under an active layer of silicon. The structure 11 according to the invention will therefore be able to include, by way of example, an active layer 5 of silicon with a thickness of between 20 nm and 2 microns, advantageously 145 nm, and an

underlying dielectric layer 6 with a thickness of between 20 nm and 1 micron, advantageously 400 nm; the trapping layer 4 is arranged between the dielectric layer 6 and the support substrate 2. The fabrication of the MEMS part is then based on surface micromachining techniques, making it possible in particular to free beams or mobile membranes in the active layer of silicon.

Alternatively, the MEMS part can be created directly on the trapping layer 4, by successive deposition of a plurality of layers (including an electrode, a dielectric, a sacrificial layer, an active layer) and by the production of patterns on these different layers.

The microelectronic processes for the fabrication of the control element(s) (CMOS for example), usually performed before the MEMS part, require, as in the preceding embodiment, the application of high-temperature heat treatments. The mechanical strength of the trapping layer 4 to this type of treatment and its capacity to retain its electrical properties (high resistivity and trap density suitable for trapping the mobile charges) are therefore key advantages.

In the same way as for the third embodiment, the high-frequency signals propagated in this device 7 generate electromagnetic fields which penetrate into the trapping layer 4 and into the support substrate 2. The losses (insertion losses), distortions (harmonics) and disturbances (crosstalk, etc.) will be lesser because of the high and stable resistivity of the support substrate 2 provided with the trapping layer 4.

According to a fifth embodiment, the structure 11 for radiofrequency applications can comprise or consist of

a microelectronic device 7 comprising a radiofrequency filter operating by bulk acoustic wave (BAW) propagation.

The fabrication of a BAW filter of FBAR (thin-film bulk acoustic resonator) type necessitates an active layer 5 consisting of a piezoelectric material, in which the acoustic wave will be contained between the two electrodes which surround it. The structure 11 according to the invention will therefore be able to include, by way of example, an active layer 5 of aluminum nitride with a thickness of between 50 nm and 1 μm, advantageously 100 nm, and a dielectric layer 6 (for example of silicon oxide) with a thickness of between 1 and 6 μm; the trapping layer 4 is arranged between the dielectric layer 6 and the support substrate 2. Insulation cavities are formed under the active layers of the filter, that is to say the areas in which the acoustic waves will be required to be propagated.

The fabrication of the BAW filter then entails steps of depositions of electrodes to which the RF signal will be applied.

The structure 11 according to the invention makes it possible on the one hand to limit the depth of the insulation cavities whose insulation function relative to the substrate is made less critical by the high and stable resistivity of the support substrate and of the trapping layer; this is an advantage in terms of simplification, flexibility and robustness in the process of fabrication of these devices. Also, the structure 11 according to the invention makes it possible to obtain better performance levels in the filters, notably in terms of linearity.

According to a variant of this fifth embodiment, the microelectronic device 7 comprises a radiofrequency filter operating by surface acoustic wave (SAW) propagation.

The fabrication of an SAW filter requires an active layer 5 consisting of a piezoelectric material, on the surface of which will be created an electrode comb: the acoustic wave is intended to be propagated between these electrodes. The structure 11 according to the invention will therefore be able to include, by way of example, an active layer 5 of lithium tantalate with a thickness of between 200 nm and 20 μm, advantageously 0.6 μm; the trapping layer 4 is arranged between the active layer 5 and the support substrate 2. A dielectric layer 6 can optionally be added between the active layer 5 and the trapping layer 4.

The structure 11 according to the invention makes it possible to obtain better filter performance levels, notably in terms of insertion losses and of linearity.

The structure 1, 1', 11 for radiofrequency applications according to the invention is not limited to the embodiments cited above. It is suited to any application for which high-frequency signals propagate and are likely to undergo undesirable losses or disturbances in a support substrate, because the physical and electrical characteristics of the trapping layer 4 arranged on the support substrate 2 confer good RF properties on the assembly (limiting the losses, nonlinearities and other disturbances).

CLAIMS

1. A structure for radiofrequency applications comprising:

a support substrate of high-resistivity silicon comprising a non-doped lower part and a p-type doped upper part, the p-typed doped upper part formed to a depth D of less than 1 µm in the support substrate; and

a mesoporous trapping layer of silicon formed in the p-type doped upper part of the support substrate, the mesoporous trapping layer having a porosity rate of between 20% and 60% such that the mesoporous trapping layer traps inversion charges susceptible to be generated in the non-doped lower part and the non-doped lower part retains a high and stable resistivity level.

2. The structure of claim 1, wherein the mesoporous trapping layer has pores with a diameter of between 2 nm and 50 nm.

3. The structure of claim 2, wherein the resistivity of the non-doped lower part of the support substrate is greater than 1000 ohm.cm.

4. The structure of claim 1, wherein an active layer is disposed over the mesoporous trapping layer.

5. The structure of claim 4, wherein the active layer compromises a semiconductive material.

6. The structure of claim 4, wherein the active layer compromises a piezoelectric material.

7. The structure of claim 4, wherein the active layer comprises at least one material selected from the group consisting of:

silicon, silicon carbide, silicon germanium, lithium niobate, lithium tantalate, quartz, and aluminum nitride.

8. The structure of claim 4, wherein the thickness of the active layer is between 10 nm and 50 µm.

9. The structure of claim 4, wherein a dielectric layer is disposed between the mesoporous trapping layer and the active layer.

10. The structure of claim 9, wherein the dielectric layer comprises at least one material selected from the group consisting of: silicon dioxide, silicon nitride, and aluminum oxide.

11. The structure of claim 10, wherein the dielectric layer is between 10 nm and 6 µm.

12. The structure of claim 4, wherein at least one microelectronic device is present on or in the active layer, the microelectronic device being a switching circuit or an antenna tuning circuit or a radiofrequency power amplification circuit.

13. The structure of claim 4, wherein at least one microelectronic device is present on or in the active layer, the microelectronic device comprising a plurality of active components and a plurality of passive components.

14. The structure of claim 4, wherein at least one microelectronic device is present on or in the active layer, the microelectronic device comprising at least one control element and one MEMS switching element comprising a microswitch with ohmic contact or a capacitive micro-switch.

15. The structure of claim 4, wherein at least one microelectronic device is present on or in the active layer, the microelectronic device comprising a radiofrequency filter operating by bulk or surface acoustic wave propagation.

16. The structure of claim 1, wherein the resistivity of the non-doped lower part of the support substrate is greater than 1000 ohm.cm.

17. The structure of claim 1, wherein an active layer is arranged on the mesoporous trapping layer.

18. The structure of claim 9, wherein the dielectric layer is between 10 nm and 6 µm.