ABSTRACT

A METHOD FOR MAKING IMPROVED SHALLOW TRENCH ISOLATION FOR SEMICONDUCTOR INTEGRATED CIRCUITS

A method was achieved for fabricating field oxide regions (shallow trench isolation) having raised portions which are self-aligned and extend over edges of device areas. This results in FETs with improved sub-threshold characteristics and lower sub-threshold leakage currents. The method consists of forming a pad oxide and depositing a doped polysilicon layer and a hard mask layer on a silicon substrate. Shallow trenches are etched through the hard mask, doped polysilicon layer and partially into the silicon substrate. A thermal oxidation is used to form a liner oxide in the trenches and to oxidize, at a higher oxidation rate, the sidewalls of the doped polysilicon layer to form an oxide over the edges of the device areas. A gap-fill oxide is deposited in the trenches and chemical mechanical polished (CMP) back to the polysilicon layer. The remaining polysilicon layer over the device areas is selectively removed to provide a field oxide having raised portions formed over the edges of the device areas. This eliminates the wrap-around corner effect which in the prior art resulted in enhanced corner conduction and increased sub-threshold leakage currents at substrate back bias. This improved method also provides greater processing latitude during the chemical mechanical polish step.

(FIGURE 7 IS SUGGESTED FOR PUBLICATION)