Claims

1. Method for fabricating a semiconductor structure comprising a semiconductor layer (5) and a metallic layer (7), the method comprising the steps of:

   a) providing a semiconductor layer (5) comprising defects and/or dislocations (11a, 11b, 11c),

   b) removing material at one or more locations of the defects and/or dislocations (11a, 11b, 11c) thereby forming pits (13a, 13b, 13c) in the semiconductor layer (5),

   c) passivating the pits (13a, 13b, 13c), and

   d) providing the metallic layer (7) over the semiconductor layer (5).

2. The method according to claim 1, wherein the passivating step c) includes a step of at least partially filing the pits with a dielectric material (15).

3. The method according to claim 1 or 2, wherein the material removal step b) comprises a step of etching the surface of the semiconductor layer (5) preferentially at one or more locations of the defects and/or dislocations (11a, 11b, 11c).

4. The method according to claim 2 or 3, wherein the dielectric material (15) is chosen from any one of silicon oxide, silicon nitride and mixtures thereof.

5. The method according to any one of claims 2 to 4, wherein the dielectric material (15) completely fills the pits (13a, 13b, 13c) formed in step b).

6. The method according to any one of claims 1 to 5, further comprising a step e) of polishing the surface of the semiconductor layer (5) after step c) and before step d).

7. The method according to any one of claims 1 to 6, wherein the metallic layer is provided by any one of physical vapor deposition (PVD), sputtering and chemical vapor deposition.

8. The method according to claim 7, wherein the semiconductor layer (5) is chosen from any one of GaN, Silicon, strained Silicon, Germanium, SiGe or a III-V material, III/N material, binary or ternary or quaternary alloy like GaN, InGaN, AlGaN, AlGaInN and the

likes and the metallic layer is chosen from any one of Al, Au, Pt, chromium, palladium, tungsten, molybdenum or silicides from the same, polycrystalline or amorphous material and alloys or combinations thereof.

9. A semiconductor structure comprising a semiconductor layer (5) and a metallic layer (7) provided over the semiconductor layer (5),

wherein pits at least partially filed with a dielectric material (15) are present in the semiconductor layer (5).

10. The semiconductor structure according to claim 9, wherein the metallic layer (7) is provided on the semiconductor layer (5) and the pits extend up to the interface with the metallic layer (7).

11. The semiconductor structure according to claim 9 or 10, wherein the dielectric material (15) is chosen from any one of silicon oxide, silicon nitride and mixtures thereof.

12. The semiconductor structure according to any one of claims 9 to 11, wherein the pits are completely filed with the dielectric material (15).

13. The semiconductor structure according to any one of claims 9 to 11, wherein the pits filled with dielectric material are arranged on top of dislocations and/or defects in the semiconductor layer.

14. A device using the semiconductor structure of any one of claims 9 to 13, in particular a Schottky diode.

Claims

1. Method for fabricating a semiconductor structure comprising a semiconductor layer (5) and a metallic layer (7), the method comprising the steps of:

   a) providing a semiconductor layer (5) comprising defects and/or dislocations (11a, 11b, 11c),

   b) removing material at one or more locations of the defects and/or dislocations (11a, 11b, 11c) thereby forming pits (13a, 13b, 13c) in the semiconductor layer (5),

   c) passivating the pits (13a, 13b, 13c), and

   d) providing the metallic layer (7) over the semiconductor layer (5).

2. The method according to claim 1, wherein the passivating step c) includes a step of at least partially filing the pits with a dielectric material (15).

3. The method according to claim 1 or 2, wherein the material removal step b) comprises a step of etching the surface of the semiconductor layer (5) preferentially at one or more locations of the defects and/or dislocations (11a, 11b, 11c).

4. The method according to claim 2 or 3, wherein the dielectric material (15) is chosen from any one of silicon oxide, silicon nitride and mixtures thereof.

5. The method according to any one of claims 2 to 4, wherein the dielectric material (15) completely fills the pits (13a, 13b, 13c) formed in step b).

6. The method according to any one of claims 1 to 5, further comprising a step e) of polishing the surface of the semiconductor layer (5) after step c) and before step d).

7. The method according to any one of claims 1 to 6, wherein the metallic layer is provided by any one of physical vapor deposition (PVD), sputtering and chemical vapor deposition.

8. The method according to claim 7, wherein the semiconductor layer (5) is chosen from any one of GaN, Silicon, strained Silicon, Germanium, SiGe or a III-V material, III/N material, binary or ternary or quaternary alloy like GaN, InGaN, AlGaN, AlGaInN and the likes and the metallic layer is chosen from any one of Al, Au, Pt, chromium, palladium,

tungsten, molybdenum or silicides from the same, polycrystalline or amorphous material and alloys or combinations thereof.

9. A semiconductor structure comprising a semiconductor layer (5) and a metallic layer (7) provided over the semiconductor layer (5),

wherein pits at least partially filed with a dielectric material (15) are arranged in the semiconductor layer (5) on top of dislocations and/or defects in the semiconductor layer.

10. The semiconductor structure according to claim 9, wherein the metallic layer (7) is provided on the semiconductor layer (5) and the pits extend up to the interface with the metallic layer (7).

11. The semiconductor structure according to claim 9 or 10, wherein the dielectric material (15) is chosen from any one of silicon oxide, silicon nitride and mixtures thereof.

12. The semiconductor structure according to any one of claims 9 to 11, wherein the pits are completely filed with the dielectric material (15).

13. A device using the semiconductor structure of any one of claims 9 to 12, in particular a Schottky diode.